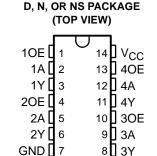
SDFS017B - JANUARY 1989 - REVISED NOVEMBER 2002

- 4.5-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

description/ordering information

The SN74F126 bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.



To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver

ORDERING INFORMATION

TA	PAC	KAGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74F126N	SN74F126N
0°C to 70°C	SOIC - D	Tube	SN74F126D	F126
0°C to 70°C	3010 - D	Tape and reel	SN74F126DR	F120
	SOP – NS	Tape and reel	SN74F126NSR	74F126

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each buffer)

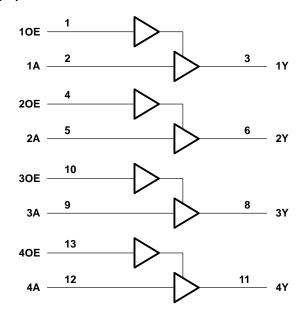
INP	JTS	OUTPUT
OE	Α	Y
Н	Н	Н
Н	L	L
L	Χ	Z



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	0.5 V to 7 V 1.2 V to 7 V
,	-1.2 v to 7 v
	or power-off state
Voltage range applied to any output in the high stat	e –0.5 V to V _{CC}
Current into any output in the low state	128 mÅ
Package thermal impedance, θ_{JA} (see Note 2): D	package 86°C/W
N	backage 80°C/W
NS	package 76°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
lıK	Input clamp current			-18	mA
ІОН	High-level output current			-15	mA
loL	Low-level output current			64	mA
T _A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP†	MAX	UNIT
VIK	I _I = -18 mA	4.5 V			-1.2	V
	$I_{OH} = -3 \text{ mA}$	4.5 V	2.4	3.3		
Voн	$I_{OH} = -15 \text{ mA}$	4.5 V	2	3.1		V
	$I_{OH} = -3 \text{ mA}$	4.75 V	2.7			
V _{OL}	I _{OL} = 64 mA	4.5 V		0.4	0.55	V
lį	V _I = 7 V	0			0.1	mA
l _{IH}	V _I = 2.7 V	5.5 V			20	μΑ
I _{IL}	V _I = 0.5 V	5.5 V			-20	μΑ
lozh	$V_0 = 2.7 \text{ V}$	5.5V			50	μΑ
lozL	V _O = 0.5 V	5.5 V			-50	μΑ
los [‡]	VO = 0	5.5 V	-100		-225	mA
Іссн	Outputs open	5.5 V		20	30	mA
ICCL	Outputs open	5.5 V		32	48	mA
ICCZ	Outputs open	5.5 V		26	39	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

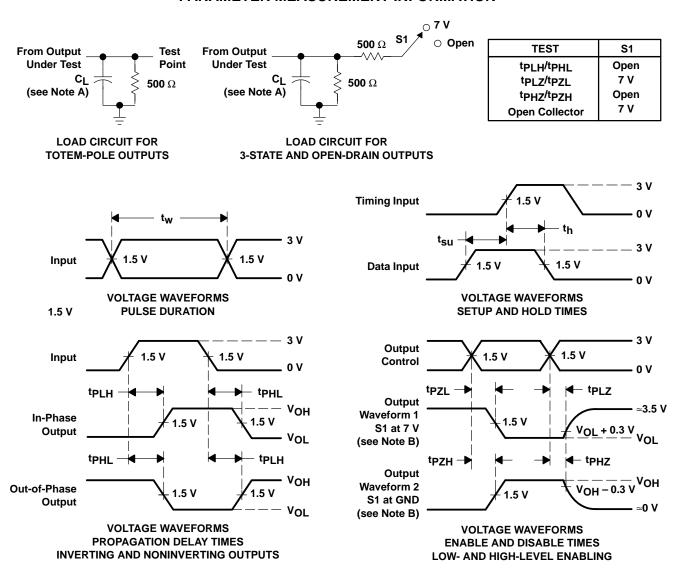
PARAMETER	FROM (INPUT)	TO (OUTPUT)	լ Շլ	CC = 5 V _ = 50 pl _ = 500 C _ = 25°C	F,	V _{CC} = 4.5 V C _L = 50 R _L = 500 T _A = MIN to	0Ω,	UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	Α	>	2	4	6.5	2	7	ns
^t PHL		Y	3	5.5	8	2.8	8.5	115
^t PZH	OE	>	3.8	6	7.5	3.3	8.5	ns
^t PZL	OE	Ť	3.8	6	8	3.5	8.5	115
^t PHZ	OE	>	2	4.5	6.5	2	7.5	ns
^t PLZ	UE	I	3	5.5	7.5	3	8	115

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns, duty cycle = 50%.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	()	.,			(-)	(4)	(5)		(-,
SN74F126D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	F126
SN74F126DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F126
SN74F126DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F126
SN74F126N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F126N
SN74F126N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F126N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Device Package Type F		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74F126DR	SOIC	D	14	2500	353.0	353.0	32.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F126N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74F126N.A	N	PDIP	14	25	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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