SDFS048A - D2932, MARCH 1987 - REVISED OCTOBER 1993

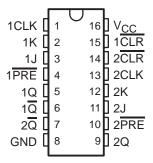
 Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

description

The SN74F112 contains two independent J-K negative-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. The SN74F112 can perform as a toggle flip-flop by tying J and K high.

The SN74F112 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE (TOP VIEW)



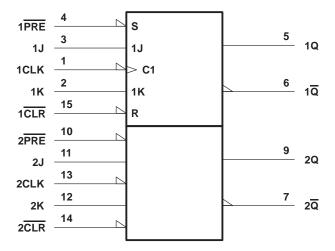
FUNCTION TABLE

		INPUTS			OUTI	PUTS
PRE	CLR	CLK	J	K	Q	Q
L	Н	Х	Χ	Х	Н	L
Н	L	X	Χ	X	L	Н
L	L	X	Χ	X	H [†]	H [†]
Н	Н	\downarrow	L	L	Q_0	\overline{Q}_0
Н	Н	\downarrow	Н	L	Н	L
Н	Н	\downarrow	L	Н	L	Н
Н	Н	\downarrow	Н	Н	Toggle	
Н	Н	Н	Χ	Χ	Q ₀	\overline{Q}_0

[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

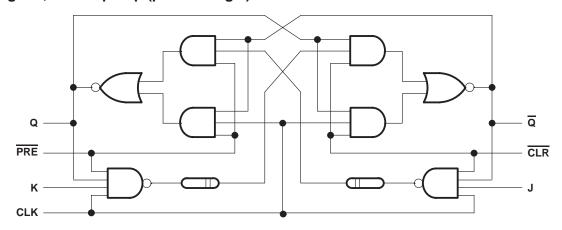
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	1.2 V to 7 V
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the high state	-0.5 V to V _{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.



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recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
lik	Input clamp current			-18	mA
ІОН	High-level output current			- 1	mA
lOL	Low-level output current			20	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TE	ST CONDITIONS	MIN	TYP [†]	MAX	UNIT
٧ıK	·	$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.5	3.4		V
VOH		$V_{CC} = 4.75 V$,	$I_{OH} = -1 \text{ mA}$	2.7			V
VOL		V _{CC} = 4.5 V,	$I_{OL} = 20 \text{ mA}$		0.3	0.5	V
II		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1	mA
lн		$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20	μΑ
	J or K					- 0.6	
Iμ	PRE or CLR	V _{CC} = 5.5 V,	$V_{I} = 0.5 V$			-3	mA
	CLK					- 2.4	
los‡		V _{CC} = 5.5 V,	VO = 0	-60		-150	mA
ICC		V _{CC} = 5.5 V,	See Note 2		12	19	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 2: ICC is measured with all outputs open, the Q and \overline{Q} outputs alternately high and the clock input grounded at the time of measurement.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	= 5 V, 25°C	MIN	MAX	UNIT	
			MIN	MAX				
fclock	Clock frequency		0	110	0	100	MHz	
	Pulse duration	CLK high or low	4.5		5		ns	
t _W	r uise duration	CLR or PRE low	4.5		5	113		
	Saturatima data hafara CLK	High	4		5		no	
t _{su}	Setup time, data before CLK↓	Low	3		3.5		ns	
4.	Hold time data often CLIV	High	0		0			
t _h	Hold time, data after CLK↓	Low	0		0		ns	
t _{su}	Setup time, inactive state, data before CLK↓§	CLR or PRE high	4		5	·	ns	

[§] Inactive-state state setup time is also referred to as recovery time.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN74F112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

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switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R _I	CC = 5 V _ = 50 pl _ = 500 s _ = 25°C	F, Ω,	V _{CC} = 4.5 C _L = 50 pl R _L = 500 C T _A = MIN	UNIT	
			MIN	TYP	MAX	MIN	MAX	
f _{max}			110	130		100		MHz
t _{PLH}	CLK	Q or $\overline{\mathbb{Q}}$	1.2 4.6 6.5		6.5	1.2	7.5	ns
^t PHL	OLK	QOQ	1.2	4.6	6.5	1.2	7.5	115
^t PLH	PRE or CLR	Q or $\overline{\mathbb{Q}}$	1.2	1.2 4.1		1.2	7.5	ns
^t PHL	TINE OF CER	Q 01 Q	1.2	4.1	6.5	1.2	7.5	110

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74F112D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	F112
SN74F112DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F112
SN74F112DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F112
SN74F112N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F112N
SN74F112N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F112N
SN74F112NE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F112N
SN74F112NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F112
SN74F112NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F112

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F112DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74F112NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Type Package Drawing		SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74F112DR	SOIC	D	16	2500	340.5	336.1	32.0	
SN74F112NSR	SOP	NS	16	2000	353.0	353.0	32.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F112N	N	PDIP	16	25	506	13.97	11230	4.32
SN74F112N	N	PDIP	16	25	506	13.97	11230	4.32
SN74F112N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F112N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F112NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74F112NE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOP



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOF



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOF



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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