SCDS062C - JUNE 1998 - REVISED NOVEMBER 2001

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Bus Hold on Data Inputs/Outputs Eliminates the Need for External Pullup/Pulldown Resistors

description

The SN74CBTH16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 12-bit bus switches with separate output-enable (\overline{OE}) inputs. It can be used as two 12-bit bus switches or one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is on, and the A port is connected to the B port. When \overline{OE} is high, the switch is open, and a high-impedance state exists between the two ports.

Active bus-hold circuitry is provided to hold unused or floating A and B ports at a valid logic level

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

NC [1 ₁ ~	56] 1 0E
1A1 [2	55 2OE
1A2 [3	54 🛮 1B1
1A3 [4	53 🛮 1B2
1A4 [5	52 🛮 1B3
1A5 [6	51 🛭 1B4
1A6 [7	50 🛮 1B5
GND [3	49 🛮 GND
1A7 [9	48 🛮 1B6
1A8 [10	47 🛮 1B7
1A9		46 🛮 1B8
1A10	12	45 🛭 1B9
1A11 [13	44 🛮 1B10
1A12	14	43 🛮 1B11
2A1	15	42 1B12
2A2	16	41 🛮 2B1
V _{CC}	17	40 2B2
2A3		39 🛮 2B3
GND [19	38 🛮 GND
2A4	20	37 🛮 2B4
2A5	21	36 🛮 2B5
2A6		35 🛮 2B6
2A7	23	34 🛮 2B7
2A8	24	33 🛮 2B8
2A9 [32 🛮 2B9
2A10	26	31 2B10
2A11	27	30 2B11
2A12 [28	29 2B12

NC - No internal connection

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74CBTH16211DL	CBTH16211
–40°C to 85°C	330F - DL	Tape and reel	SN74CBTH16211DLR	CBIHI0ZII
-40°C 10 85°C	TSSOP – DGG	Tape and reel	SN74CBTH16211DGGR	CBTH16211
	TVSOP – DGV	Tape and reel	SN74CBTH16211DGVR	CYH211

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



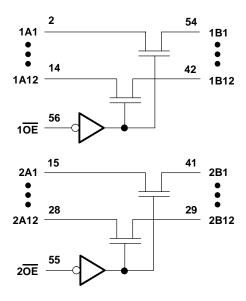
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FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		<i>–</i> 0.5 V	to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V	to 7 V
Continuous channel current		1	28 mA
Input clamp current, I _{IK} (V _I < 0)		–	50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	6	4°C/W
	DGV package	4	8°C/W
	DL package	5	6°C/W
Storage temperature range, T _{stg}		–65°C to	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER		TEST CONDITION	ONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA				-1.2	V
Ī	Control inputs	$V_{CC} = 0 V$,	V _I = 5.5 V				±10	^
I _{BHL} ‡	All inputs	V _{CC} = 5.5 V,	$V_I = 5.5 \text{ V or GND}$				±10	μΑ
I _{BHL} ‡		$V_{CC} = 4.5 V,$	V _I = 0.8 V		100			μΑ
IBHH§		$V_{CC} = 4.5 V,$	V _I = 2 V		-100			μΑ
IBHLO	,¶	$V_{CC} = 5.5 V$,	V _I = 0 to 5.5 V		500			μΑ
Івнно) [#]	$V_{CC} = 5.5 \text{ V},$	V _I = 0 to 5.5 V		-500			μΑ
Icc		$V_{CC} = 5.5 V$,	$I_{O} = 0$,	$V_I = V_{CC}$ or GND			3	μΑ
ΔICC	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _I = 15 mA		14	20	
r _{on} *			\/. 0	I _I = 64 mA		5	7	Ω
"'		V _{CC} = 4.5 V	V _I = 0	I _I = 30 mA		5	7	
			V _I = 2.4 V,	I _I = 15 mA		8	12	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V	V _{CC} =	UNIT	
	(1141 01)	(0011 01)	MIN MAX	MIN	MAX	
$^{t}pd^{\square}$	A or B	B or A	0.35		0.25	ns
t _{en}	<u>OE</u>	A or B	9.9	1	9.6	ns
^t dis	ŌE	A or B	9.5	1	8.3	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



[‡] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[§] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

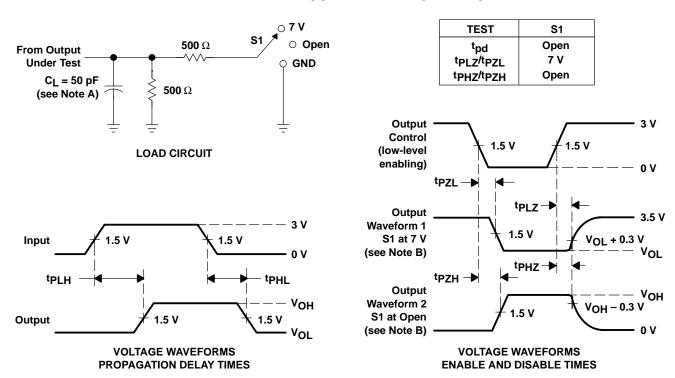
[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

^{*}Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_r \leq 2.5 ns, t_r \leq 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpH7 are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74CBTH16211DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTH16211
SN74CBTH16211DGGR.A	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTH16211

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTH16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTH16211DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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