- Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on})
 Characteristics (r_{on} = 3 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C_{io(OFF)} = 5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 3 μA Max)
- V_{CC} Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DB, DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)

1OE [1B1 [1 2	24 23	V _{CC}
1A1 [3	22	2A5
1A2[4	21	2A4
1B2[5	20	2B4
1B3[6	19	2B3
1A3[7	18	2A3
1A4 [8	17	2A2
1B4 [9	16	2B2
1B5 [10	15	2B1
1A5 [11	14	2A1
GND[12	13	20E

description/ordering information

The SN74CBT3384C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3384C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3384C is organized as two 5-bit bus switches with separate \overline{OE} output-enable (\overline{IOE} , \overline{IOE}) inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When \overline{OE} is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 5-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGI	<u></u> =†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	0010 014	Tube	SN74CBT3384CDW	ODT00040	
	SOIC - DW	Tape and reel	SN74CBT3384CDWR	CBT3384C	
	CCOD DD	Tube	SN74CBT3384CDB	CBT3384C	
-40°C to 85°C	SSOP – DB	Tape and reel	SN74CBT3384CDBR	CB13384C	
-40 C to 65 C	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3384CDBQR	CBT3384C	
	TOCOD DW	Tube	SN74CBT3384CPW	CU384C	
	TSSOP – PW	Tape and reel	SN74CBT3384CPWR		
	TVSOP – DGV	Tape and reel	SN74CBT3384CDGVR	CU384C	

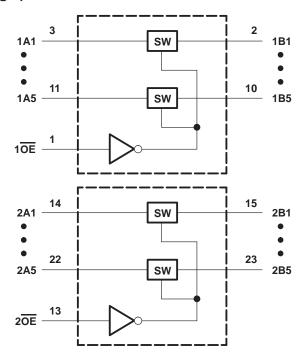
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 5-bit bus switch)

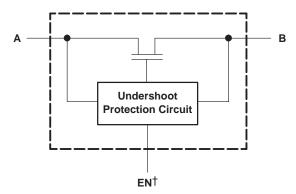
INPUT OE	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect



logic diagram (positive logic)



simplified schematic, each FET switch (SW)



†EN is the internal enable signal applied to the switch.

SN74CBT3384C 10-BIT FET BUS SWITCH 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS132A - SEPTEMBER 2003 - REVISED OCTOBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 7 V
Control input voltage range, V _{IN} (see Notes 1 ar	nd 2)	0.5 V to 7 V
Switch I/O voltage range, V _{I/O} (see Notes 1, 2, a	and 3)	0.5 V to 7 V
Control input clamp current, I _{IK} (V _{IN} < 0)		
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		
ON-state switch current, I _{I/O} (see Note 4)		±128 mA
Continuous current through V _{CC} or GND termin	nals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5):	DB package	63°C/W
	DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
 - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 3. V_I and V_O are used to denote specific conditions for V_{I/O}.
 - 4. II and IO are used to denote specific conditions for II/O.
 - 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
٧ _{IH}	High-level control input voltage	2	5.5	V
VIL	Low-level control input voltage	0	8.0	V
V _{I/O}	Data input/output voltage	0	5.5	V
TA	Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER		TEST CONDITIO	NS	MIN	TYP†	MAX	UNIT
VIK	Control inputs	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$				-1.8	V
VIKU	Data inputs	V _{CC} = 5 V,	0 mA > $I_I \ge -50$ mA, $V_{IN} = V_{CC}$ or GND, Switch OFF				-2	V
I _{IN}	Control inputs	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = V_{CC}$ or GND				±1	μΑ
I _{OZ} ‡		V _{CC} = 5.5 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, V _{IN} = V _{CC} or GND			±10	μΑ
I _{off}		$V_{CC} = 0$,	$V_0 = 0 \text{ to } 5.5 \text{ V},$	V _I = 0			10	μΑ
ICC		V _{CC} = 5.5 V,	$I_{I/O} = 0,$ $V_{IN} = V_{CC} \text{ or GND},$	Switch ON or OFF			3	μΑ
∆ICC§	Control inputs	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
C _{in}	Control inputs	$V_{IN} = 3 V \text{ or } 0$				3.5		pF
C _{io(OFF)})	$V_{I/O} = 3 \text{ V or } 0,$	Switch OFF,	$V_{IN} = V_{CC}$ or GND		5		pF
C _{io(ON)}		$V_{I/O} = 3 \text{ V or } 0,$	Switch ON,	$V_{IN} = V_{CC}$ or GND		12.5		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _O = -15 mA		8	12	
$r_{on}\P$			V 0	I _O = 64 mA		3	6	Ω
0		V _{CC} = 4.5 V	V _I = 0	I _O = 30 mA		3	6	
			V _I = 2.4 V,	$I_O = -15 \text{ mA}$		5	10	

 $V_{\mbox{\footnotesize{IN}}}$ and $I_{\mbox{\footnotesize{IN}}}$ refer to control inputs. $V_{\mbox{\footnotesize{I}}},\,V_{\mbox{\footnotesize{O}}},\,I_{\mbox{\footnotesize{I}}},$ and $I_{\mbox{\footnotesize{O}}}$ refer to data pins.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V	V _{CC} =	= 5 V 5 V	UNIT
	(INPOT)	(001701)	MIN MAX	MIN	MAX	
tpd#	A or B	B or A	0.24		0.15	ns
t _{en}	ŌE	A or B	5	1.5	4.2	ns
^t dis	ŌĒ	A or B	5	1.5	4.5	ns

[#]The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



[†] All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^{\circ}C$.

 $[\]ddagger$ For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

undershoot characteristics (see Figures 1 and 2)

	PARAMETER		TEST CONDI	TIONS	MIN	TYP†	MAX	UNIT
ſ	Vоити	$V_{CC} = 5.5 \text{ V},$	Switch OFF,	$V_{IN} = V_{CC}$ or GND	2 '	V _{OH} -0.3		V

 $[\]overline{\dagger}$ All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25$ °C.

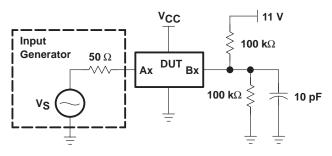


Figure 1. Device Test Setup

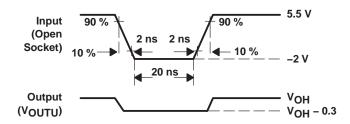
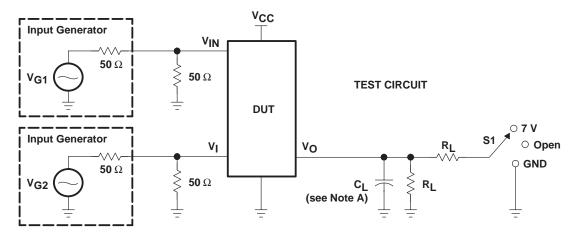


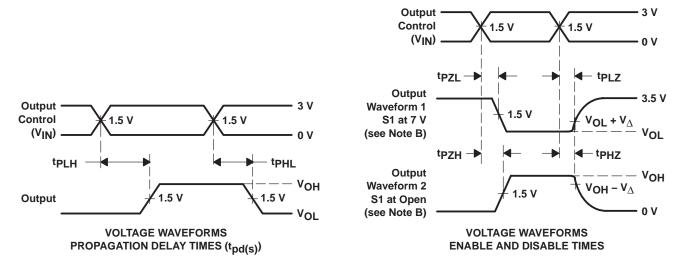
Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)



PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	$v_{\!\scriptscriptstyle\Delta}$
tpd(s)	$\begin{array}{c} \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{4 V} \end{array}$	Open Open	500 Ω 500 Ω	V _{CC} or GND V _{CC} or GND	50 pF 50 pF	
tPLZ/tPZL	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t _{PHZ} /t _{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V _{CC}	50 pF 50 pF	0.3 V 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms



www.ti.com

7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	•		MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74CBT3384CDBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3384C
SN74CBT3384CDBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3384C
SN74CBT3384CDBQRG4	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3384C
SN74CBT3384CDBQRG4.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3384C
SN74CBT3384CDGVR	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU384C
SN74CBT3384CDGVR.B	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU384C
SN74CBT3384CDWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3384C
SN74CBT3384CDWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3384C
SN74CBT3384CPW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU384C
SN74CBT3384CPW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU384C
SN74CBT3384CPWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU384C
SN74CBT3384CPWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU384C

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 7-Oct-2025

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 9-Oct-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3384CDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3384CDBQRG4	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3384CDGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3384CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT3384CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1



www.ti.com 9-Oct-2025



*All dimensions are nominal

7 th difference and from the												
Device	Package Type	Package Drawing	ing Pins SPQ Length (m		Length (mm)	Width (mm)	Height (mm)					
SN74CBT3384CDBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0					
SN74CBT3384CDBQRG4	SSOP	DBQ	24	2500	353.0	353.0	32.0					
SN74CBT3384CDGVR	TVSOP	DGV	24	2000	353.0	353.0	32.0					
SN74CBT3384CDWR	SOIC	DW	24	2000	350.0	350.0	43.0					
SN74CBT3384CPWR	TSSOP	PW	24	2000	353.0	353.0	32.0					

PACKAGE MATERIALS INFORMATION

www.ti.com 9-Oct-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3384CPW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74CBT3384CPW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated