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- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
 - 5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V-Tolerant I/Os With Device Powered-Up or Powered-Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on})
 Characteristics (r_{on} = 5 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading (C_{io(OFF)} = 5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 40 μA Max)

- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0 to 5-V Signaling Levels (For Example: 0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V/2.5-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, Memory Interleaving, Bus Isolation
- Ideal for Low-Power Portable Equipment

DBQ, DGV, DW, OR PW PACKAGE (TOP VIEW)

10E	1	\bigcup_{24}	v _{cc}
1B1 [2	23	2B5
1A1 [3	22	2A5
1A2 [4	21	2A4
1B2[5	20] 2B4
1B3[6	19	2B3
1A3[7	18	2A3
1A4 [8	17	2A2
1B4 [9	16	2B2
1B5 [10	15	2B1
1A5 [11	14	2A1
GND [12	13	2 <u>OE</u>

description/ordering information

ORDERING INFORMATION

TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	
	0010 PW	Tube	SN74CB3T3384DW	ODOTO004
	SOIC – DW	Tape and reel	SN74CB3T3384DWR	CB3T3384
-40°C to 85°C	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3T3384DBQR	CB3T3384
-40°C to 85°C	T000D BW	Tube	SN74CB3T3384PW	140004
	TSSOP – PW	Tape and reel	SN74CB3T3384PWR	KS384
	TVSOP – DGV	Tape and reel	SN74CB3T3384DGVRGE	PREVIEW

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



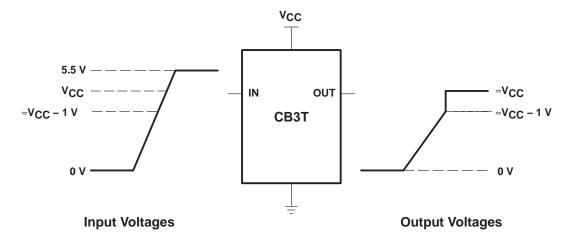
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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description/ordering information (continued)

The SN74CB3T3384 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3384 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1$ V, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC-Voltage-Translation Characteristics

The SN74CB3T3384 is organized as two 5-bit bus switches with separate ouput-enable $(1\overline{OE}, 2\overline{OE})$ inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When \overline{OE} is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 5-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

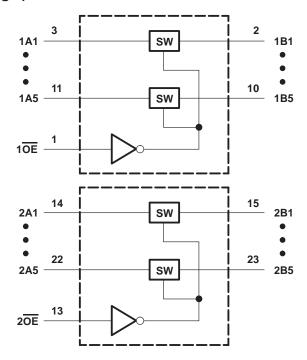
FUNCTION TABLE (each 5-bit bus switch)

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	В	A port = B port
Н	Z	Disconnect

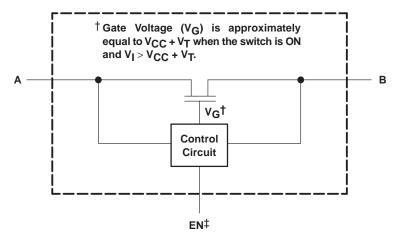


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logic diagram (positive logic)



simplified schematic, each FET switch (SW)



‡EN is the internal enable signal applied to the switch.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} (see Note 1)		0.5 V to 7 V
Control input voltage range, V _{IN} (see Notes 1 a	and 2)	0.5 V to 7 V
Switch I/O voltage range, V _{I/O} (see Notes 1, 2,	and 3)	0.5 V to 7 V
Control input clamp current, I _{IK} (V _{IN} < 0)		–50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)		–50 mA
ON-state switch current, I _{I/O} (see Note 4)		±128 mA
Continuous current through V _{CC} or GND termin	nals	±100 mA
Package thermal impedance, θ _{JA} (see Note 5):	: DBQ package	61°C/W
	DGV package	86°C/W
	DW package	46°C/W
	PW package	88°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
 - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 3. V_I and V_O are used to denote specific conditions for V_{I/O}.
 - 4. II and IO are used to denote specific conditions for II/O.
 - 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
.,	High lavel control in the others	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	
VIH	High-level control input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		5.5	V
.,	Law book and all Constructions	V _{CC} = 2.3 V to 2.7 V		0.7	
VIL	Low-level control input voltage	V _{CC} = 2.7 V to 3.6 V	0	0.8	V
V _{I/O}	Data input/output voltage		0	5.5	V
TA	Operating free-air temperature		-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER SCDS159B - OCTOBER 2003 - REVISED MARCH 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIO	NS	MIN	TYP [†]	MAX	UNIT	
VIK		V _{CC} = 3 V, I _I = -18 mA			-1.2	V		
Vон		See Figures 3 and 4						
I _{IN}	Control inputs	V _{CC} = 3.6 V, V _{IN} = 3.6 V to 5.5 V or GND				±10	μΑ	
		V _{CC} = 3.6 V,	$V_I = V_{CC} - 0.7 \text{ V to } 5.5 \text{ V}$			±20		
Ц		Switch ON,	$V_{I} = 0.7 \text{ V to } V_{CC} - 0.7 \text{ V}$			-40	μΑ	
		V _{IN} = GND	$V_{I} = 0 \text{ to } 0.7 \text{ V}$			±5		
loz [‡]		$\begin{split} &V_{CC}=3.6 \text{ V,} \\ &V_{O}=0 \text{ to } 5.5 \text{ V,} \\ &V_{I}=0, \\ &\text{Switch OFF,} \\ &V_{IN}=V_{CC} \end{split}$				±10	μΑ	
l _{off}		$V_{CC} = 0,$ $V_{O} = 0 \text{ to } 5.5 \text{ V},$ $V_{I} = 0$				10	μΑ	
1		$V_{CC} = 3.6 \text{ V},$ $I_{I/O} = 0,$	$V_I = V_{CC}$ or GND			40	^	
ICC		Switch ON or OFF, V _{IN} = V _{CC} or GND	V _I = 5.5 V			40	μА	
ΔlCC§	Control inputs	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} - 0.6 \text{ V},$ Other inputs at V_{CC} or GND				300	μΑ	
C _{in}	Control inputs	V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND			3		pF	
C _{io(OFF)}		$V_{CC} = 3.3 \text{ V},$ $V_{I/O} = 5.5 \text{ V}, 3.3 \text{ V}, \text{ or GND},$ Switch OFF, $V_{IN} = V_{CC}$			5		pF	
C _{io(ON)}		V _{CC} = 3.3 V, Switch ON,	V _{I/O} = 5.5 V or 3.3 V		4		pF	
SIO(ON)		V _{IN} = GND	$V_{I/O} = GND$		12		Ρı	
		V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V,	I _O = 24 mA		5	8		
$_{ron}\P$		V _I = 0	$I_O = 16 \text{ mA}$		5	8	Ω	
J11		V _{CC} = 3 V,	I _O = 64 mA		5	7		
		V _I = 0	$I_O = 32 \text{ mA}$		5	7		

 V_{IN} and I_{IN} refer to control inputs. V_{I} , V_{O} , I_{I} , and I_{O} refer to data pins.

[†] All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.

[¶] Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN74CB3T3384 10-BIT FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS159B - OCTOBER 2003 - REVISED MARCH 2004

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

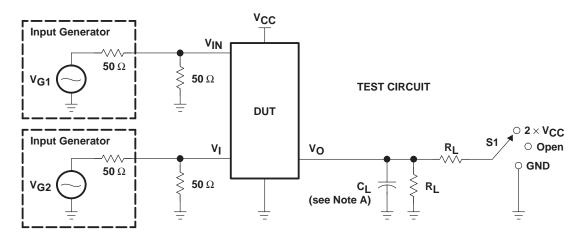
PARAMETER	FROM	TO	V _{CC} =		V _{CC} =	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		0.15		0.25	ns
^t en	ŌĒ	A or B	1	10.5	1	7.5	ns
^t dis	ŌĒ	A or B	1	6.5	1	8	ns

[†]The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

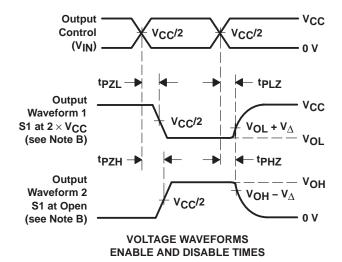


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PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	$v_{\!\scriptscriptstyle\Delta}$
tPLZ/tPZL	$\begin{array}{c} \textbf{2.5 V} \pm \textbf{0.2 V} \\ \textbf{3.3 V} \pm \textbf{0.3 V} \end{array}$	2×V _{CC} 2×V _{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
tPHZ/tPZH	$\begin{array}{c} \textbf{2.5 V} \pm \textbf{0.2 V} \\ \textbf{3.3 V} \pm \textbf{0.3 V} \end{array}$	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. tpzL and tpzH are the same as ten.

Figure 2. Test Circuit and Voltage Waveforms



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TYPICAL CHARACTERISTICS

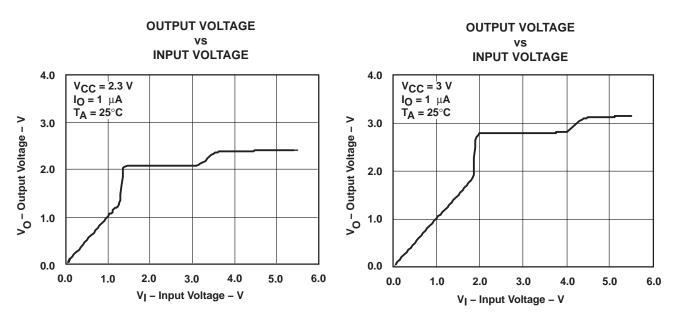
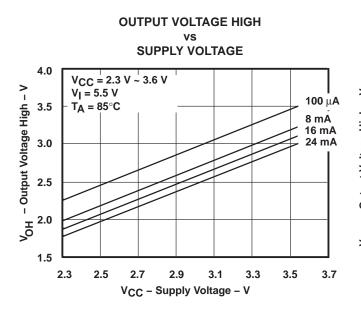
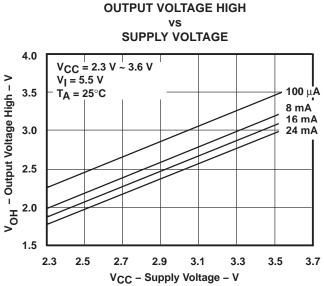


Figure 3. Data Output Voltage vs Data Input Voltage



TYPICAL CHARACTERISTICS (continued)





OUTPUT VOLTAGE HIGH

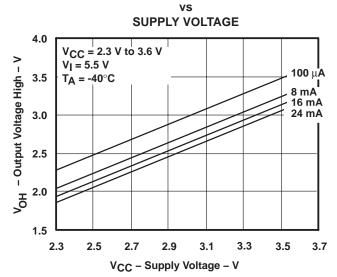


Figure 4. V_{OH} Values

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74CB3T3384DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3384
SN74CB3T3384DBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3384
SN74CB3T3384DBQRG4	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3384
SN74CB3T3384DBQRG4.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3384
SN74CB3T3384DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3384
SN74CB3T3384DW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3384
SN74CB3T3384DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3384
SN74CB3T3384DWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3384
SN74CB3T3384PW	Obsolete	Production	TSSOP (PW) 24	-	-	Call TI	Call TI	-40 to 85	KS384
SN74CB3T3384PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS384
SN74CB3T3384PWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS384

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3384DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3384DBQRG4	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3384DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CB3T3384PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3384DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CB3T3384DBQRG4	SSOP	DBQ	24	2500	353.0	353.0	32.0
SN74CB3T3384DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CB3T3384PWR	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3T3384DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74CB3T3384DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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