

24-BIT FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

Check for Samples: [SN74CB3T16211](#)

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
 - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 5\ \Omega$ Typ)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)} = 5\text{ pF}$ Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 70\ \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, PCI Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

NC	1	56	$\overline{1OE}$
1A1	2	55	$\overline{2OE}$
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
V_{CC}	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

NC - No internal connection



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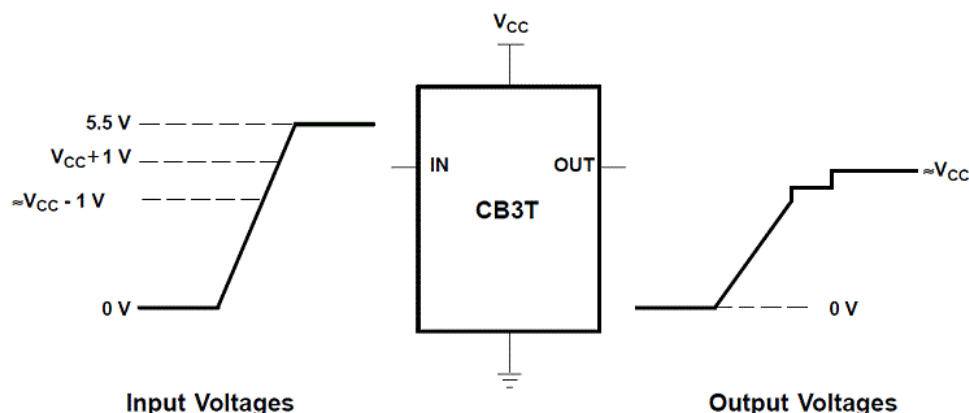
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION/ORDERING INFORMATION

The SN74CB3T16211 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T16211 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

DESCRIPTION/ORDERING INFORMATION (CONTINUED)



If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} + 1V$, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The I/O port of this device has a pullup current source that maintains the output voltage at V_{CC} when the device is ON, and the input is greater than or equal to $V_{CC} - 1$. Because of the pullup current source, the output voltage level may be less than V_{CC} when the operating frequency is low and the I/O port is connected to a pulldown resistor. In order to maintain the output voltage at V_{CC} , a pullup resistor must be connected to V_{CC} instead of a pulldown resistor to ground.

The SN74CB3T16211 is organized as two 12-bit bus switches with separate output-enable ($\overline{1OE}$, $\overline{2OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CB3T16211DL	CB3T16211
		Tape and reel	SN74CB3T16211DLR	
	TSSOP – DGG	Tube	SN74CB3T16211DGG	CB3T16211
		Tape and reel	SN74CB3T16211DGGR	
	TVSOP – DGV	Tape and reel	SN74CB3T16211DGVR	KR211
	VFBGA – GQL (Pb-free)	Tape and reel	SN74CB3T16211GQLR	KR211
	VFBGA – ZQL (Pb-free)	Tape and reel	SN74CB3T16211ZQLR	KR211

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

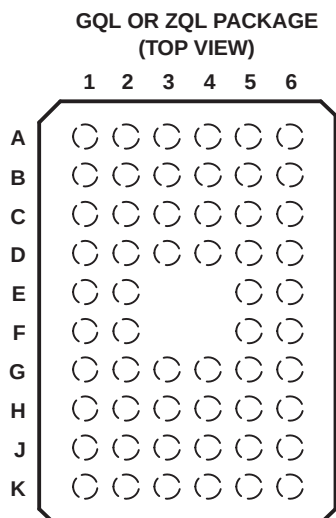


Table 2. TERMINAL ASSIGNMENTS

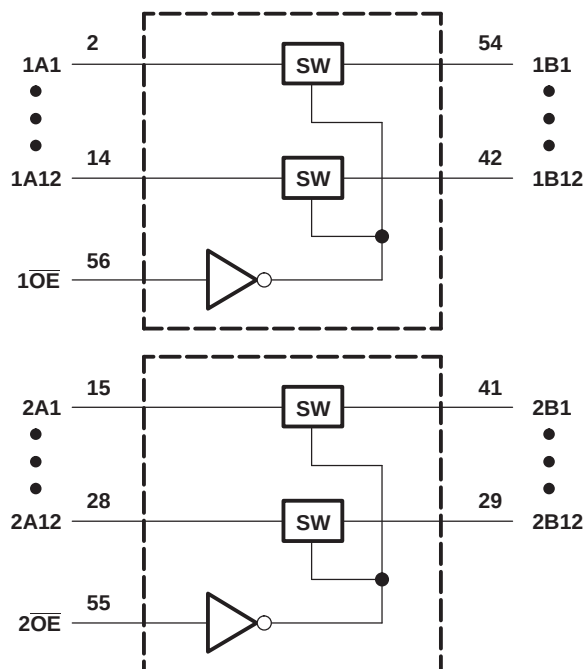
	1	2	3	4	5	6
A	1A2	1A1	NC ⁽¹⁾	1 $\overline{OE}$	2 $\overline{OE}$	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	V _{CC}	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

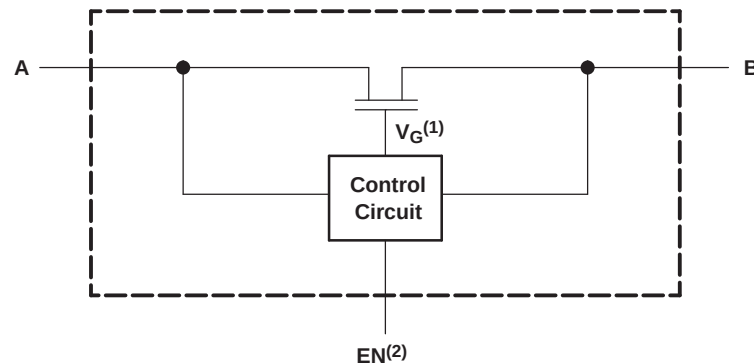
(1) NC – No internal connection

**Table 3. FUNCTION TABLE
(EACH 12-BIT BUS SWITCH)**

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)

- (1) Gate voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
 (2) Internal enable signal applied to the switch

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.5	7	V
V _{IN}	Control input voltage range ⁽²⁾ ⁽³⁾		−0.5	7	V
V _{I/O}	Switch I/O voltage range ⁽²⁾ ⁽³⁾ ⁽⁴⁾		−0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		−50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		−50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±128	mA
	Continuous current through V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
		GQL/ZQL package		42	
T _{std}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 (2) All voltages are with respect to ground, unless otherwise specified.
 (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V _{CC} = 2.7 V to 3.6 V	2	5.5	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0	0.8	
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperature		−40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}		See Figure 3 and Figure 4				
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_{IN} = 3.6\text{ V}$ to 5.5 V or GND			±10	μA
I_I		$V_{CC} = 3.6\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7\text{ V}$ to 5.5 V		±20	μA
			$V_I = 0.7\text{ V}$ to $V_{CC} - 0.7\text{ V}$		-40	
			$V_I = 0$ to 0.7 V		±5	
I_{OZ} ⁽³⁾		$V_{CC} = 3.6\text{ V}$, $V_O = 0$ to 5.5 V , $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND			±10	μA
I_{off}		$V_{CC} = 0$, $V_O = 0$ to 5.5 V , $V_I = 0$			10	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND		70	μA
			$V_I = 5.5\text{ V}$		70	
ΔI_{CC} ⁽⁴⁾	Control inputs	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND			300	μA
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$, $V_{IN} = V_{CC}$ or GND		4		pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$, $V_{I/O} = 5.5\text{ V}$, 3.3 V , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND		5		pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5\text{ V}$ or 3.3 V		5	pF
			$V_{I/O} = \text{GND}$		13	
r_{on} ⁽⁵⁾		$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$, $V_I = 0$	$I_O = 24\text{ mA}$		5	Ω
			$I_O = 16\text{ mA}$		5	
		$V_{CC} = 3\text{ V}$, $V_I = 0$	$I_O = 64\text{ mA}$		5	
			$I_O = 32\text{ mA}$		5	

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

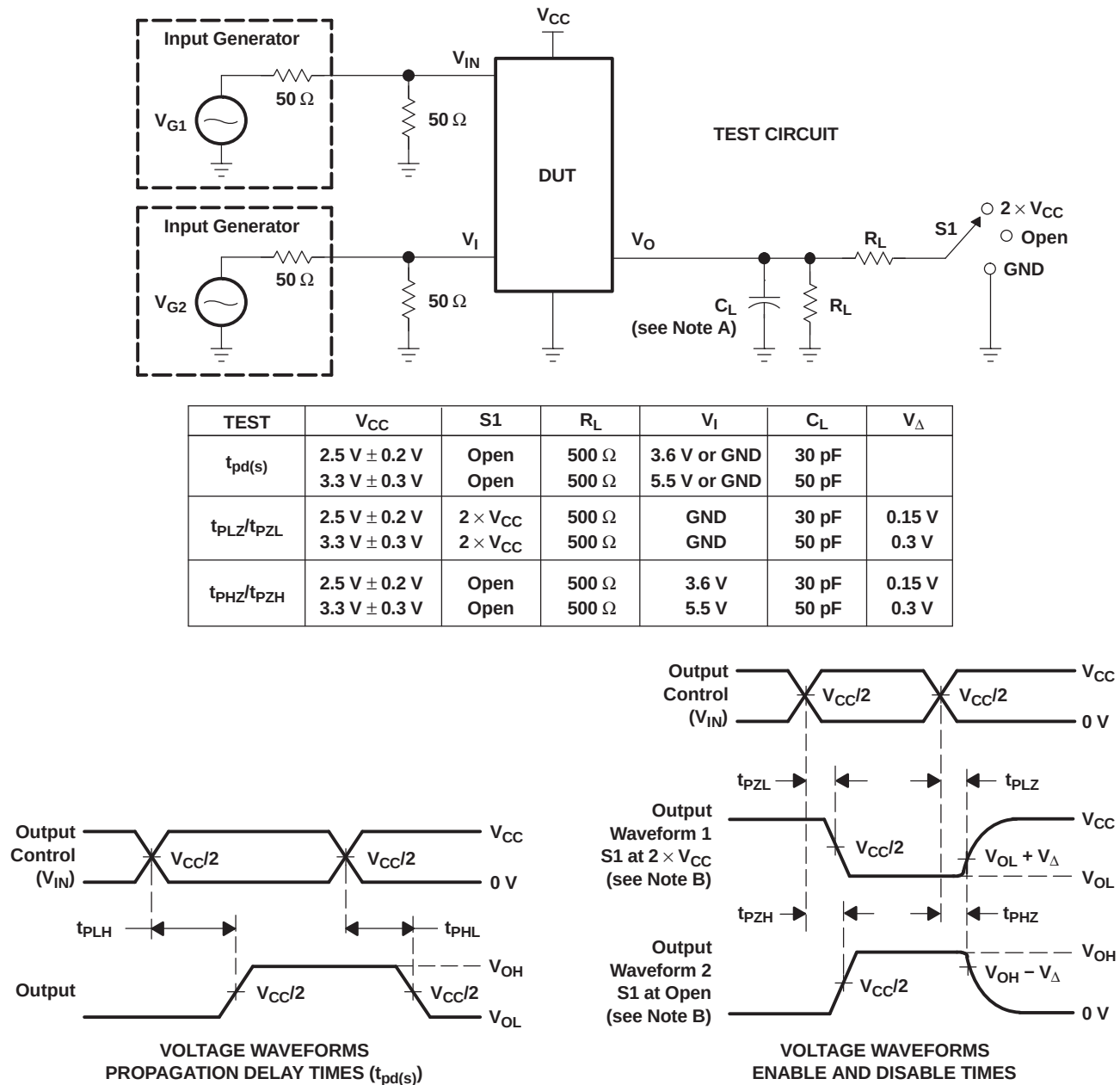
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} ⁽¹⁾	A or B	B or A	0.15		0.25		ns
t_{en}	$\overline{OE}$	A or B	1	12	1	10	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	8.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

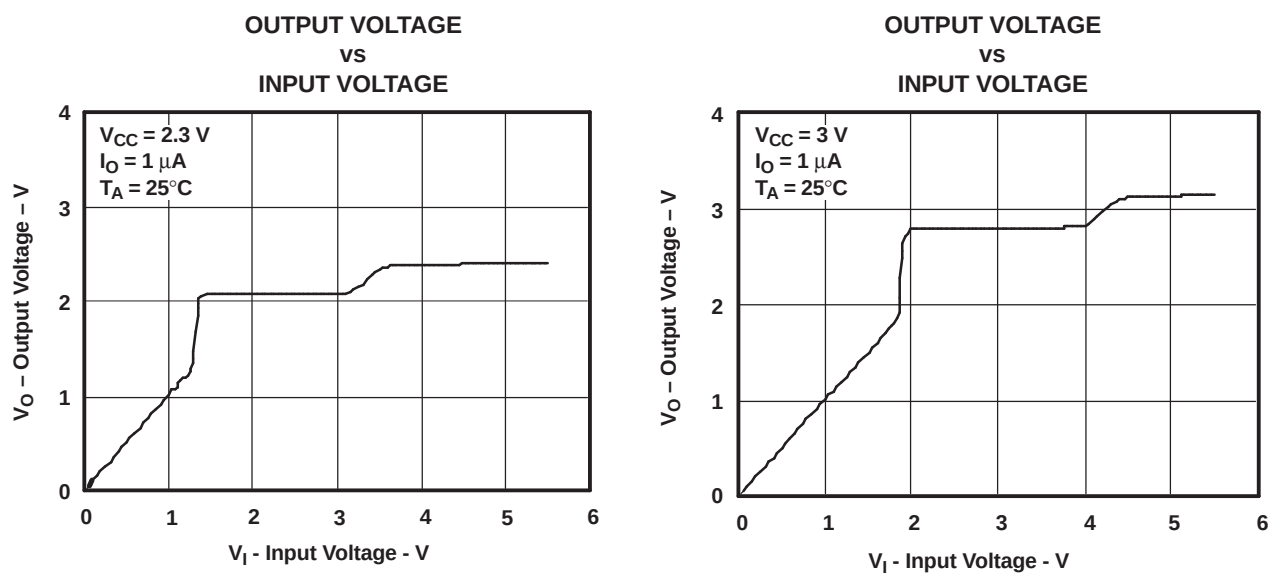
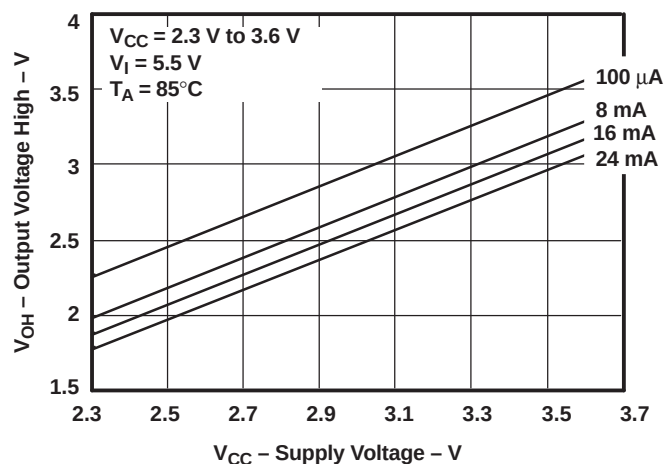
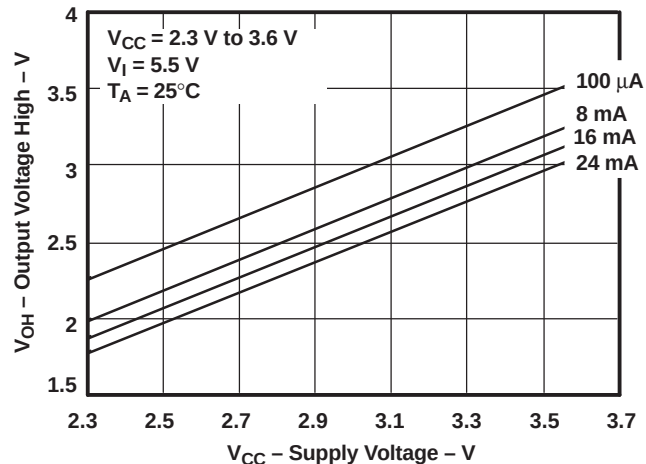
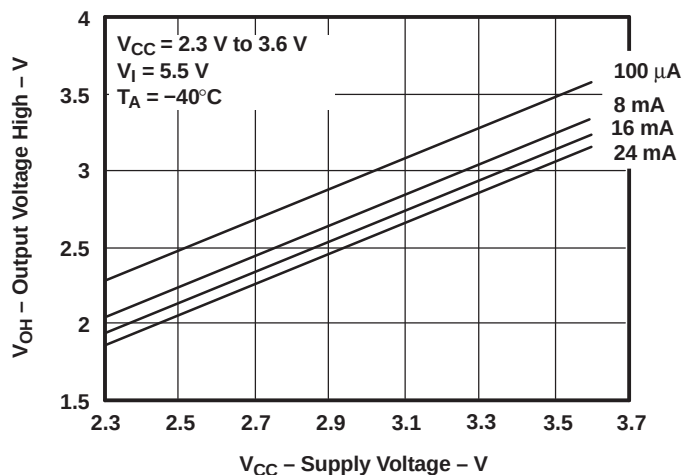


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)**OUTPUT VOLTAGE HIGH****VS****SUPPLY VOLTAGE****OUTPUT VOLTAGE HIGH****VS****SUPPLY VOLTAGE****OUTPUT VOLTAGE HIGH****VS****SUPPLY VOLTAGE****Figure 4. V_{OH} Values**

REVISION HISTORY

Changes from Revision B (January 2006) to Revision C	Page
• Updated graphic and note in figure 1.	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74CB3T16211DGVRG4	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KR211
74CB3T16211DGVRG4.B	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KR211
SN74CB3T16211DGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16211
SN74CB3T16211DGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16211
SN74CB3T16211DGVR	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KR211
SN74CB3T16211DGVR.B	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KR211
SN74CB3T16211DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16211
SN74CB3T16211DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16211
SN74CB3T16211DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16211
SN74CB3T16211DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T16211

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

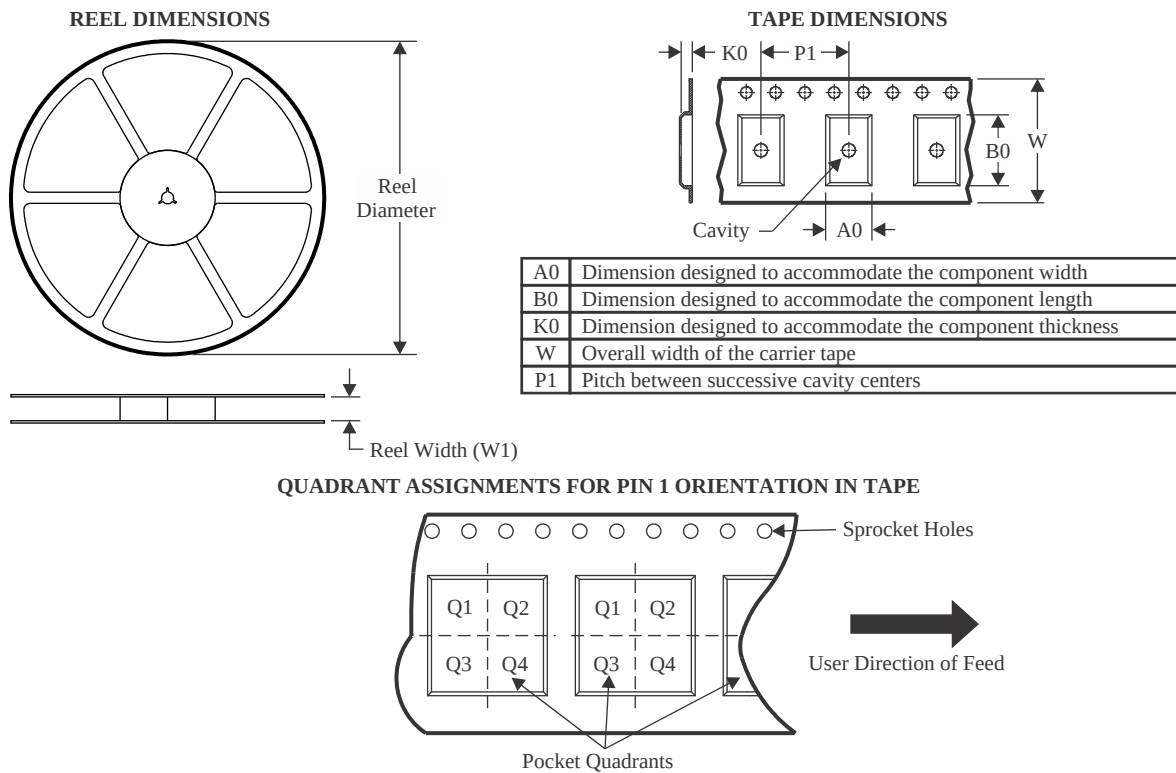
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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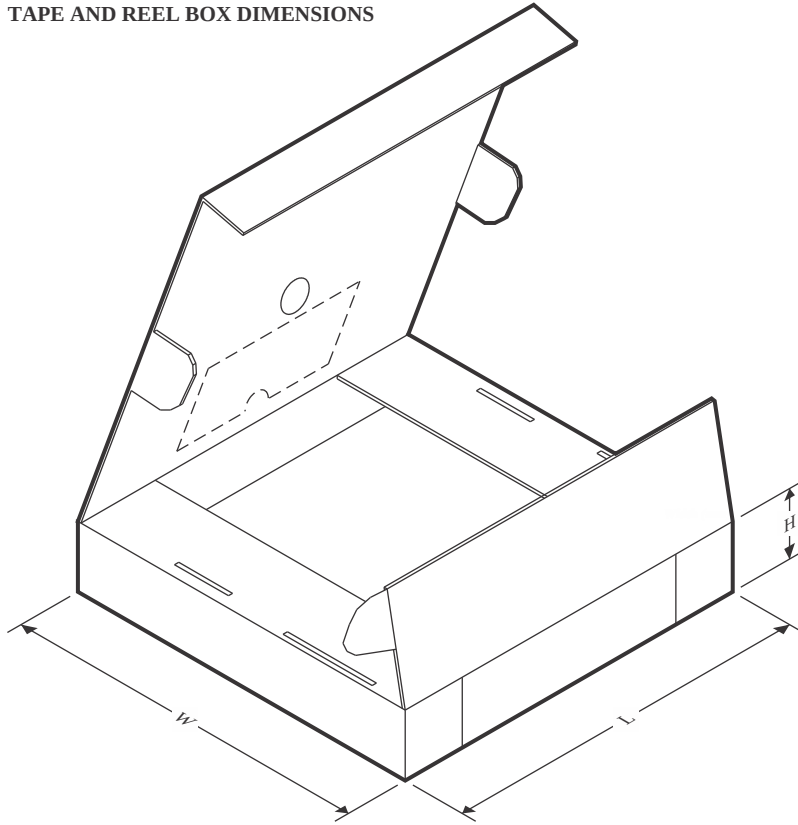
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T16211DLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CB3T16211DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74CB3T16211DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87



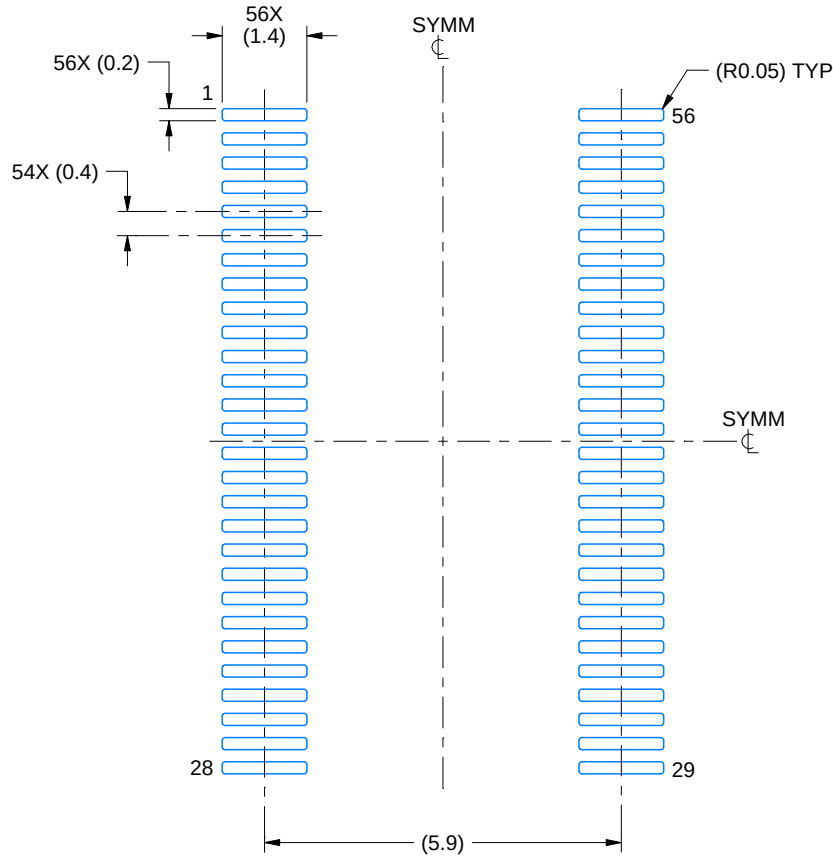
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

EXAMPLE BOARD LAYOUT

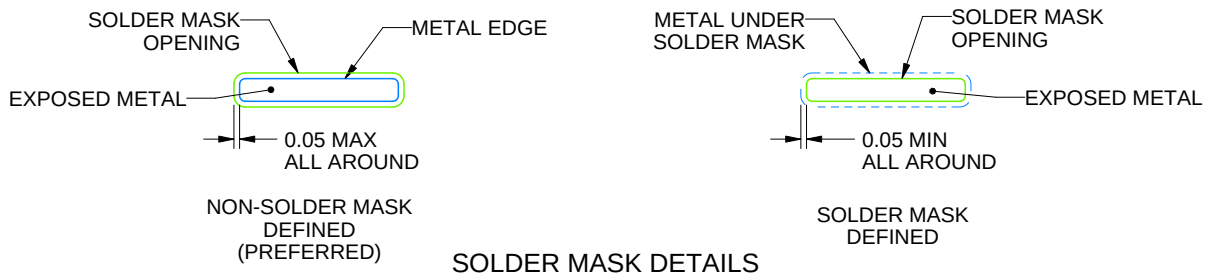
DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



4220240/B 12/2020

NOTES: (continued)

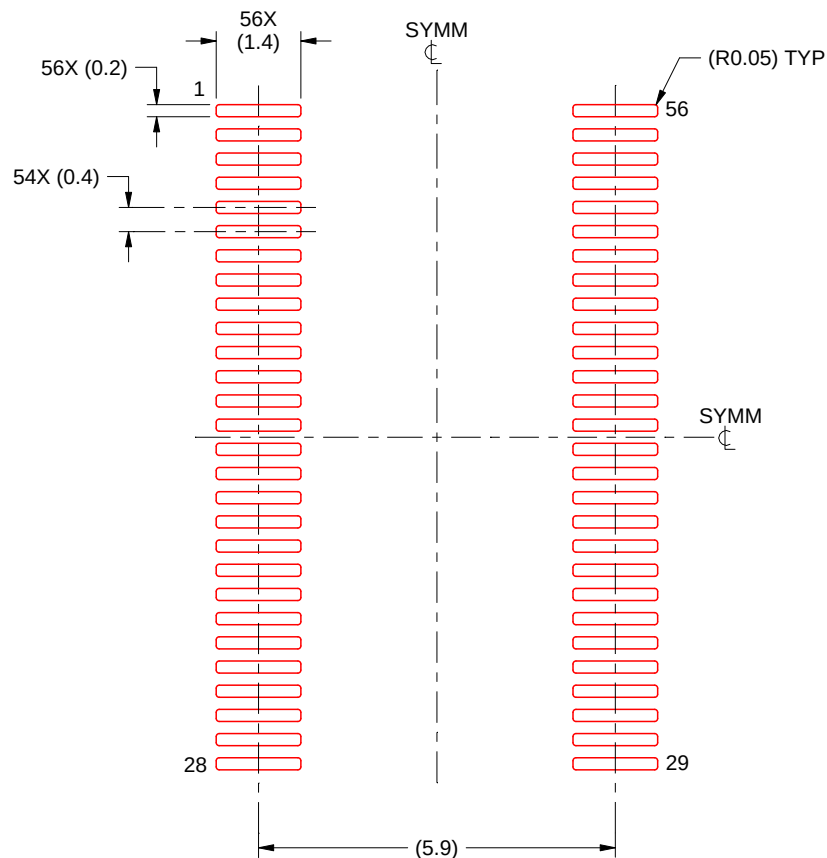
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

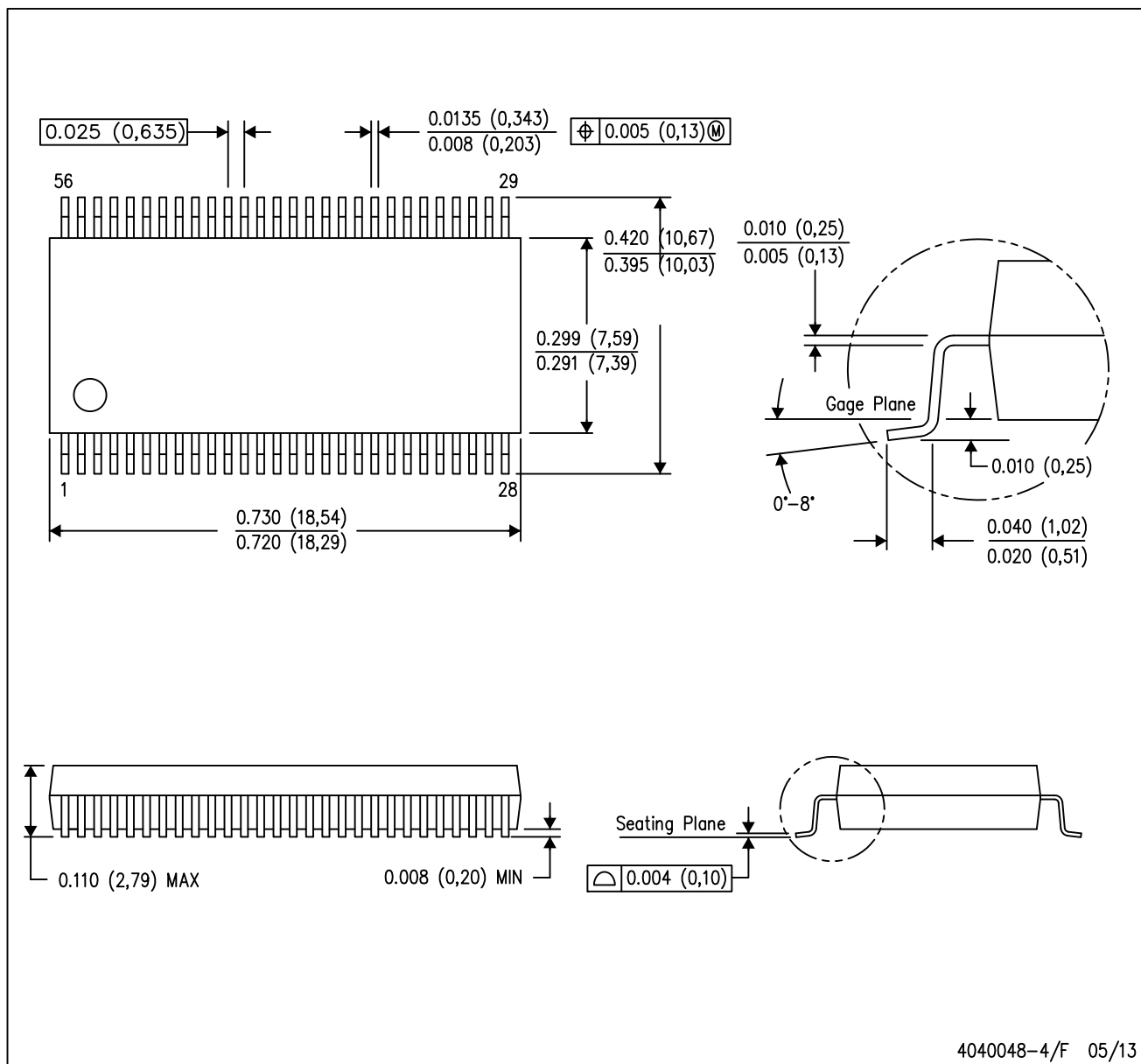
4220240/B 12/2020

NOTES: (continued)

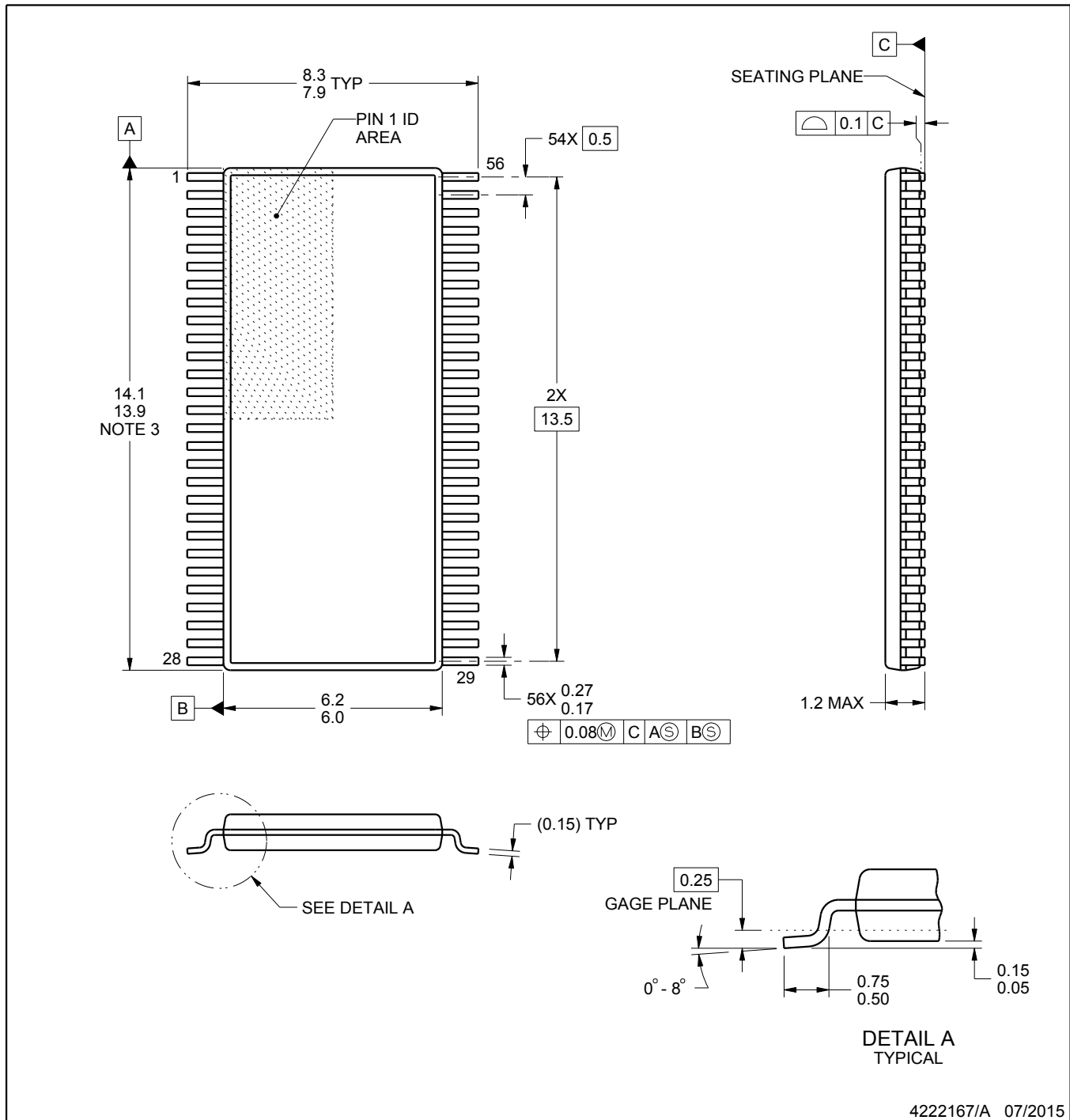
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

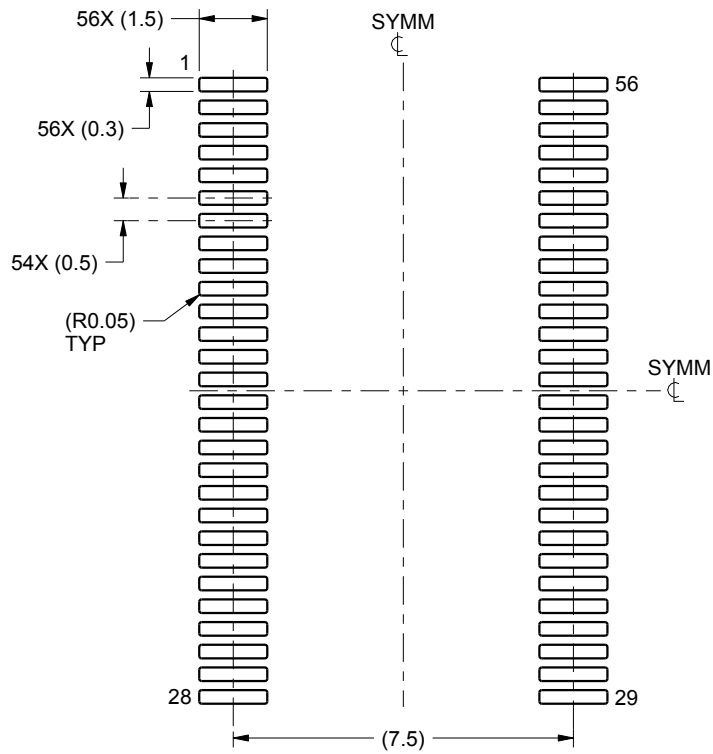
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

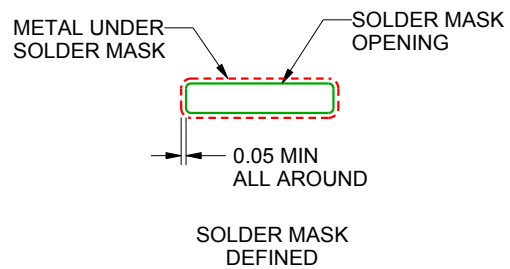
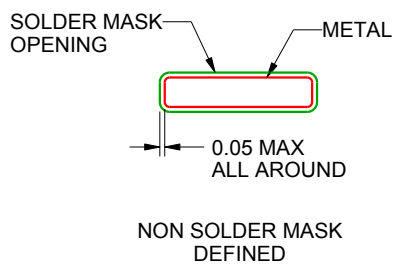
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

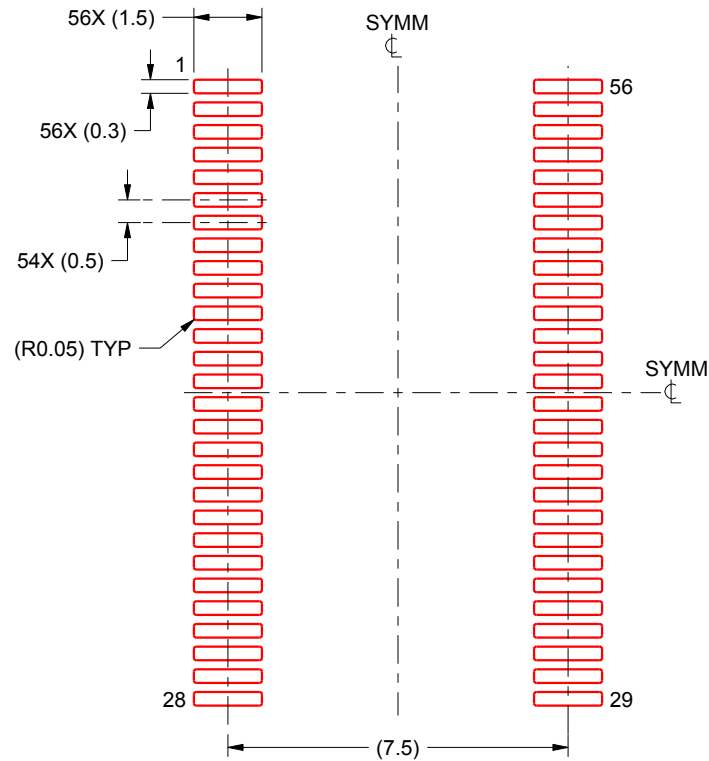
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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