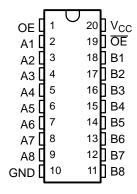
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SCDS144B-OCTOBER 2003-REVISED MARCH 2005

FEATURES

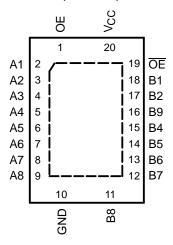
- High-Bandwidth Data Path (up to 500 MHz ⁽¹⁾)
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range $(r_{on} = 4 \Omega \text{ Typ})$
- Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion (C_{io(OFF)} = 4 pF Typ)
- Fast Switching Frequency (f_{OE} = 20 MHz Max)
- For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, CBT-C, CB3T, and CB3Q Signal-Switch Families, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE (TOP VIEW)



- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 0.7 mA Typ)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

RGY PACKAGE (TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3345 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}) . The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3345 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3384A is organized as an 8-bit bus switch with two output-enable (OE, $\overline{\text{OE}}$) inputs. When OE is high or $\overline{\text{OE}}$ is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low and $\overline{\text{OE}}$ is high, the bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

ORDERING INFORMATION

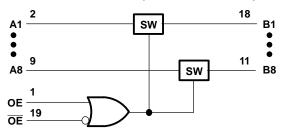
T _A	PACKA	GE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Tape and reel	SN74CB3Q3345RGYR	BU345
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3Q3345DBQR	CB3Q3345
-40°C to 85°C	TSSOP – PW	Tube	SN74CB3Q3345PW	BU345
	1330P - PW	Tape and reel	SN74CB3Q3345PWR	BU343
	TVSOP – DGV	Tape and reel	SN74CB3Q3345DGVR	BU345

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INP	JTS	INPUT/OUTPUT	FUNCTION
OE	ŌĒ	Α	FUNCTION
Н	Х	В	A port = B port
Х	L	В	A port = B port
L	Н	Z	Disconnect

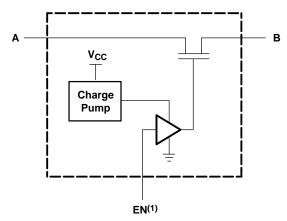
LOGIC DIAGRAM (POSITIVE LOGIC)





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SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	·	·	MIN	MAX	UNIT	
V _{CC}	Supply voltage range		-0.5	4.6	V	
V _{IN}	Control input voltage range ⁽²⁾⁽³⁾		-0.5	7	V	
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾		-0.5	7	V	
I _{I/K}	Control input clamp current	V _{IN} < 0		-50	mA	
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		-50	mA	
I _{IO}	ON-state switch current ⁽⁵⁾	·		±64	mA	
	Continuous current through V _{CC} or GND			±100	mA	
		DBQ package ⁽⁶⁾		68		
0	Dealer as the same of insured and a	DGV package ⁽⁶⁾		92	00.444	
θ_{JA}	Package thermal impedance	PW package ⁽⁶⁾		83	°C/W	
		RGY package ⁽⁷⁾		37		
T _{stg}	Storage temperature range		-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to ground, unless otherwise specified.
- The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- V_I and V_O are used to denote specific conditions for V_{I/O}.
- I_I and I_O are used to denote specific conditions for $I_{I/O}$. The package thermal impedance is calculated in accordance with JESD 51-7.
- The package thermal impedance is calculated in accordance with JESD 51-5.

SN74CB3Q3345 8-BIT FET BUS SWITCH 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH



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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V	High level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	V
V _{IH}	High-level control input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		5.5	V
.,	Lavidaval appetual institutiona	V _{CC} = 2.3 V to 2.7 V	0	0.7	
V _{IL}	Low-level control input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8	V
V _{I/O}	Data input/output voltage	·	0	5.5	V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIO	NS	MIN TYP(2)	MAX	UNIT
V _{IK}		$V_{CC} = 3.6 \text{ V},$	I _I = -18 mA			-1.8	V
I _{IN}	Control inputs	V _{CC} = 3.6 V,	V _{IN} = 0 to 5.5 V			±1	μΑ
I _{OZ} ⁽³⁾		V _{CC} = 3.6 V,	$V_O = 0 \text{ to } 5.5 \text{ V},$ $V_I = 0,$	Switch OFF, $V_{IN} = V_{CC}$ or GND		±1	μΑ
I _{off}		V _{CC} = 0,	$V_{O} = 0 \text{ to } 5.5 \text{ V},$	V _I = 0		1	μΑ
I _{CC}		V _{CC} = 3.6 V,	$I_{I/O} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}$ or GND	0.7	2	mA
$\Delta I_{CC}^{(4)}$	Control inputs	$V_{CC} = 3.6 \text{ V},$	One input at 3 V,	Other inputs at V _{CC} or GND		30	μΑ
ı (5)	Per control	V _{CC} = 3.6 V,	A and B ports open,		0.13	0.14	mA/
I _{CCD} ⁽⁵⁾	input	Control input switching	at 50% duty cycle		0.13	0.14	MHz
C _{in}	Control inputs	V _{CC} = 3.3 V,	$V_{IN} = 5.5 \text{ V}, 3.3 \text{ V}, \text{ or}$	0	2.5	3.5	рF
C _{io(OFF)}		V _{CC} = 3.3 V,	Switch OFF, $V_{IN} = V_{CC}$ or GND,	$V_{I/O} = 5.5 \text{ V}, 3.3 \text{ V}, \text{ or } 0$	3.5	5	pF
C _{io(ON)}		V _{CC} = 3.3 V,	Switch ON, $V_{IN} = V_{CC}$ or GND,	$V_{I/O} = 5.5 \text{ V}, 3.3 \text{ V}, \text{ or } 0$	9	11.5	pF
		V _{CC} = 2.3 V,	$V_I = 0$,	$I_O = 30 \text{ mA}$	4	8	
r _{on} (6)		TYP at $V_{CC} = 2.5 \text{ V}$	V _I = 1.7 V,	I _O = -15 mA	4.5	9	0
		V - 2 V	$V_I = 0$,	I _O = 30 mA	4	6	Ω
		$V_{CC} = 3 V$	$V_1 = 2.4 V,$	I _O = -15 mA	4.5	8	

- V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins. All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25$ °C. For I/O ports, the parameter I_{OZ} includes the input leakage current. This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND. This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see
- Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.2	2.5 V 2 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOI)	(001F01)	MIN	MAX	MIN	MAX	
f _{OE} or f _{OE} ⁽¹⁾	OE or OE	A or B		10		20	MHz
t _{pd} (2)	A or B	B or A		0.12		0.2	ns
t _{en}	OE or OE	A or B	1.5	7.7	1.5	6.5	ns
t _{dis}	OE or OE	A or B	1	6.9	1	6.8	ns

Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5$ V, $R_L \ge 1$ M Ω , $C_L = 0$) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

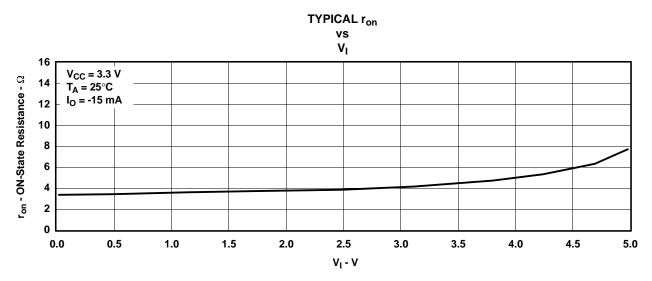


Figure 1. Typical ron vs VI

TYPICAL I_{CC}

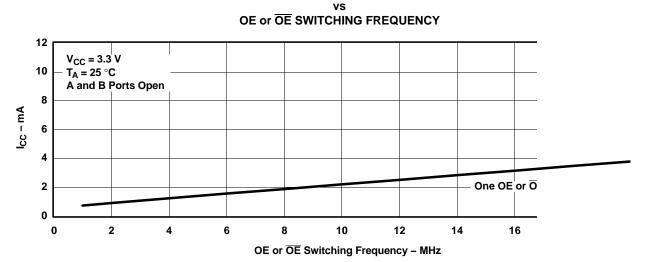
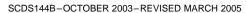
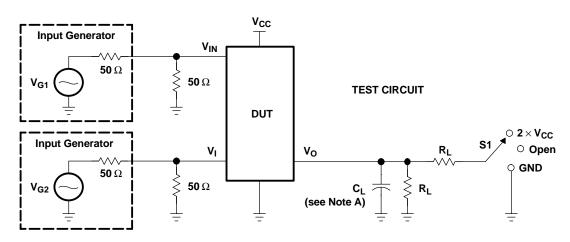


Figure 2. Typical I_{CC} vs OE or OE Switching Frequency

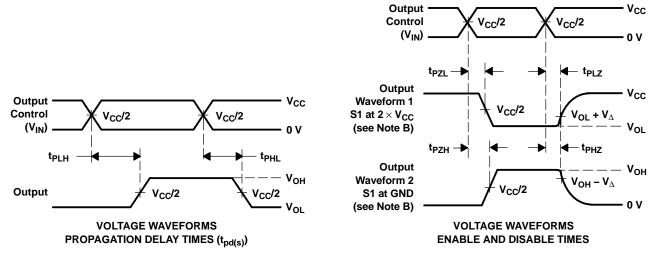




PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	VI	CL	V_{Δ}
t _{pd(s)}	2.5 V \pm 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
-pu(s)	3.3 V \pm 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2×V _{CC}	500 Ω	GND	30 pF	0.15 V
TPLZ/TPZL	3.3 V \pm 0.3 V	2×V _{CC}	500 Ω	GND	50 pF	0.3 V
4 /4	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
t _{PHZ} /t _{PZH}	3.3 V \pm 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74CB3Q3345DBQR	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3Q3345
SN74CB3Q3345DBQR.B	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3Q3345
SN74CB3Q3345DGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345DGVR.B	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	BU345
SN74CB3Q3345PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345PWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345PWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345PWRG4.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU345
SN74CB3Q3345RGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU345
SN74CB3Q3345RGYR.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU345
SN74CB3Q3345RGYR.B	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU345
SN74CB3Q3345RGYRG4	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU345
SN74CB3Q3345RGYRG4.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU345
SN74CB3Q3345RGYRG4.B	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU345

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3345DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3Q3345DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3345PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CB3Q3345PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CB3Q3345RGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74CB3Q3345RGYRG4	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3345DBQR	SSOP	DBQ	20	2500	353.0	353.0	32.0
SN74CB3Q3345DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74CB3Q3345PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74CB3Q3345PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74CB3Q3345RGYR	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74CB3Q3345RGYRG4	VQFN	RGY	20	3000	353.0	353.0	32.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AD.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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