

SN74CB3Q3257 4-Bit 1-of-2 FET Multiplexer and Demultiplexer 2.5V and 3.3V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-bandwidth data path (up to 500MHz)
- 5V Tolerant I/Os with device powered up or powered down
- Low and flat on-state resistance (r_{on}) characteristics over operating range (r_{on} = 4 Ω typical)
- Rail-to-rail switching on data I/O ports
 - 0- to 5V Switching with 3.3V V_{CC}
 - 0- to 3.3V Switching with 2.5V V_{CC}
- Bidirectional data flow with near-zero propagation
- Low input and output capacitance minimizes loading and signal distortion (C_{io(OFF)} = 3.5pF
- Fast switching frequency (f \overline{OE} = 20MHz maximum)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption ($I_{CC} = 0.7$ mA typical)
- V_{CC} Operating range from 2.3V to 3.6V
- Data I/Os support 0- to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control inputs can be driven by TTL or 5V and 3.3V CMOS outputs
- I_{off} Supports partial-power-down mode operation
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD Performance tested per JESD 22
 - 2000V Human body model (A114-B, class II)
 - 1000V Charged-device model (C101)
- Supports both digital and analog applications: USB interface, differential signal interface, bus isolation, low-distortion signal gating ¹

2 Applications

- IP Phones: wired and wireless
- Optical modules
- Optical networking: video over fiber and EPON
- Private branch exchange (PBX)
- WiMAX and wreless infrastructure equipment

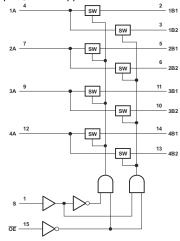
3 Description

The SN74CB3Q3257 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}).

Package Information

<u></u>						
PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾					
TVSOP (DGV, 16)	3.6mm × 6.4mm					
SSOP (DBQ, 16)	4.9mm × 6mm					
TSSOP (PW, 16)	5mm × 6.4mm					
VQFN (RGV, 16)	4mm × 3.5mm					
	TVSOP (DGV, 16) SSOP (DBQ, 16) TSSOP (PW, 16)					

- For more information, see Section 9.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

¹ For additional information regarding the performance characteristics of the CB3Q family, refer to the TI CB7-C, CB3T, and CB3Q Signal-Switch Families application report.



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4 Pin Configuration and Functions

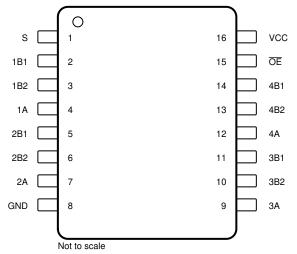


Figure 4-1. D, DB, DGV, DBQ, or PW Package 16-Pin SOIC, SSOP TVSOP, or TSSOP (Top View)

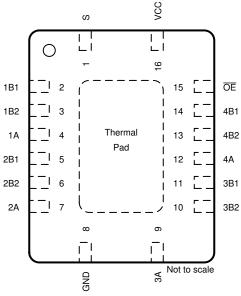


Figure 4-2. RGY Package, 16-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION		
NAME	NO.	ITPE	DESCRIPTION		
S	1	I	Select Pin		
1B1	2	I/O	Channel 1 I/O 1		
1B2	3	I/O	Channel 1 I/O 2		
1A	4	I/O	Channel 1 common		
2B1	5	I/O	Channel 2 I/O 1		
2B2	6	I/O	Channel 2 I/O 2		
2A	7	I/O	Channel 2 common		
GND	8	_	Ground		
3A	9	I/O	Channel 3 common		
3B2	10	I/O	Channel 3 I/O 2		
3B1	11	I/O	Channel 3 I/O 1		
4A	12	I/O	Channel 4 common		
4B2	13	I/O	Channel 4 I/O 2		
4B1	14	I/O	Channel 4 I/O 1		
ŌĒ	15	I	Output Enable (Active Low)		
V _{CC}	16	_	Power		

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V _{CC}	Supply voltage			-0.5	4.6	V
V _{IN}	Control input voltage ^{(2) (3)}			-0.5	7	V
V _{I/O}	Switch I/O voltage ^{(2) (3) (4)}			-0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0			-50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0			-50	mA
I _{IO}	ON-state switch current				±64	mA
	Continuous current through V _{CC} or GND				±100	mA
T _{stg}	Storage temperature			-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V High level control in out valte as		V _{CC} = 2.3V to 2.7V	1.7	5.5	V
V _{IH} High-level control in	High-level control input voltage	V _{CC} = 2.7V to 3.6V	2	5.5	
.,		V _{CC} = 2.3V to 2.7V	0	0.7	V
V _{IL}	Low-level control input voltage	$V_{CC} = 2.7V \text{ to } 3.6V$	0	0.8	
V _{I/O}	Data input/output voltage	·	0	5.5	V
T _A	Operating free-air temperature		-40	105	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Product Folder Links: SN74CB3Q3257

⁽²⁾ All voltages are with respect to ground, unless otherwise specified.

³⁾ The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽⁴⁾ V_I and V_O are used to denote specific conditions for $V_{I/O}$.

²⁾ JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



5.4 Thermal Information

			SN74CB3Q3257				
THERMAL METRIC ⁽¹⁾		DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	UNIT	
		16 PINS	16 PINS	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	114.3	126.0	112.7	49.1		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	65.4	51.3	47.5	61.2		
R _{θJB}	Junction-to-board thermal resistance	56.8	57.8	57.8	25.9	°C/W	
ΨЈТ	Junction-to-top characterization parameter	18.3	5.9	6.0	2.3	- C/W	
Ψ_{JB}	Junction-to-board characterization parameter	56.4	57.3	57.3	26.0		
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	-	-	-	11.4		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

 $T_A = -40$ °C to 105°C. Typical values stated are over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

F	PARAMETER	TEST CONDITIONS			TYP ⁽²⁾	MAX	UNIT
V _{IK}		V _{CC} = 3.6 V, I _I = -18 mA				-1.8	V
I _{IN}	Control inputs	$V_{CC} = 3.6 \text{ V}, V_{IN} = 0 \text{ to } 5$.5 V			±1	μA
I _{OZ} (3)		V_{CC} = 3.6 V, V_{O} = 0 to 5. V_{I} = 0, Switch OFF V_{IN} =				±1	μA
I _{off}		$V_{CC} = 0$, $V_{O} = 0$ to 5.5 V,	V _I = 0			1	μA
I _{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} =	· V _{CC} or GND		0.7	1.5	mA
ΔI _{CC} (4)	Control inputs	V _{CC} = 3.6 V, One input a	t 3 V, Other inputs at V _{CC} or GND			30	μA
I _{CCD} (5)	Per control input	V _{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle			0.3	0.35	mA/MHz
C _{in}	Control inputs	V _{CC} = 3.3 V, V _{IN} = 5.5 V,	V _{CC} = 3.3 V, V _{IN} = 5.5 V, 3.3 V, or 0		2.5	3.5	pF
	A port		V _{CC} = 3.3 V, Switch OFF, V _{IN} = V _{CC} or GND, V _{I/O} = 5.5 V, 3.3 V, or 0		5.5	7	pF
C _{io(OFF)}	B port	V_{CC} = 3.3 V, Switch OFF V_{IN} = V_{CC} or GND, $V_{I/O}$ =			3.5	5	pF
	A port	V _{CC} = 3.3 V, Switch ON,			10.5	13	_
C _{io(ON)}	B port	$V_{IN} = V_{CC}$ or GND, $V_{I/O} = 5.5 \text{ V}$, 3.3 V, or 0			10.5	13	pF
	$V_{CC} = 2.3 \text{ V},$ $V_{I} = 0, I_{O} = 30 \text{ mA}$		V _I = 0, I _O = 30 mA		4	8	
r _{on} ⁽⁶⁾		TYP at $V_{CC} = 2.5 \text{ V}$ $V_{I} = 1.7 \text{ V}, I_{O} = -15 \text{ mA}$ $V_{I} = 0, I_{O} = 30 \text{ mA}$ $V_{I} = 2.4 \text{ V}, I_{O} = -15 \text{ mA}$			4	9	0
					4	6	Ω
					4	8	

- (1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data terminals.
- (2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
- (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
- (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- (5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 5-2).
- (6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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5.6 Switching Characteristics, V_{CC} = 2.5V

Typical values stated are over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

	FROM	ТО	V _{CC} =	= 2.5V ± 0.2V		
PARAMETER	(INPUT)	(OUTPUT)		MAX (85°C)	MAX (105°C)	UNIT
f _{OE} or f _S ⁽¹⁾	OE or S	A or B		10	10	MHz
t _{pd} (2)	A or B	B or A		0.12	0.21	ns
t _{pd(s)}	S	A	1.5	6.5	7.5	ns
+	S	В	1.5	6.5	7.5	no
^L en	ŌĒ	A or B	1.5	6.5	7.5	ns
+	S	В	1	6	7	no
t _{dis}	ŌĒ	A or B	1	6	7	ns

⁽¹⁾ Maximum switching frequency for control inputs $(V_O > V_{CC}, V_I = 5V, R_L \ge 1M\Omega, C_L = 0)$.

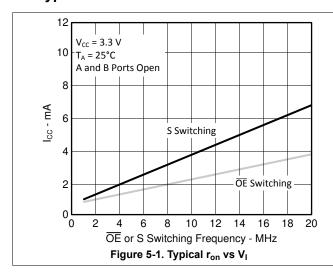
5.7 Switching Characteristics, $V_{CC} = 3.3V$

Typical values stated are over operating free-air temperature range (unless otherwise noted)

71	FROM	EDOM TO					
PARAMETER	PARAMETER FROM TO (OUTPUT)		MIN	TYP ⁽¹⁾	MAX (85°C)	MAX (105°C)	UNIT
f _{OE} or f _S ⁽¹⁾	OE or S	A or B			20	20	MHz
t _{pd} (2)	A or B	B or A			0.2	0.32	ns
t _{pd(s)}	S	A	1.5	4.1	5.5	6.5	ns
	S	В	1.5	4.6	5.5	6.5	no
Len	ŌĒ	A or B	1.5	4.7	5.5	6.5	ns
+	S	В	1	3.3	6	7	ne
t _{dis}	ŌĒ	A or B	1	3.1	6	7	ns

(1) TYP taken from average in 105°C

5.8 Typical Characteristics



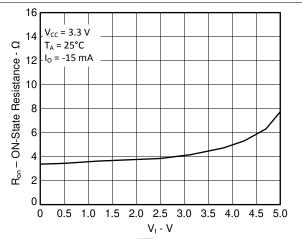


Figure 5-2. Typical I_{CC} vs \overline{OE} or S Switching Frequency

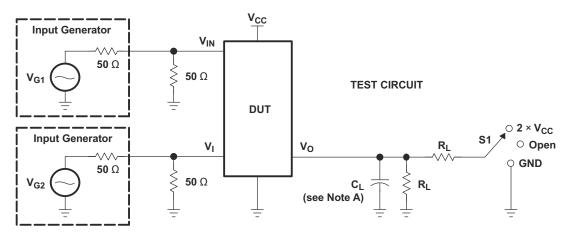
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⁽²⁾ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

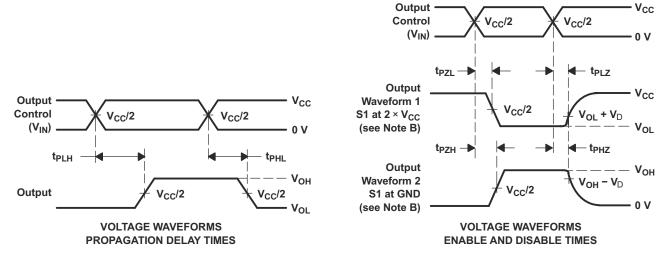


Parameter Measurement Information



TEST	V _{CC}	S1	R _L	VI	CL	V_{Δ}
t _{pd(s)}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V _{CC} or GND V _{CC} or GND	30 pF 50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V _{CC} 2 × V _{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V _{CC}	30 pF 50 pF	0.15 V 0.3 V

Output



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 W, $t_{f} \leq$ 2.5 ns. $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
- F. t_{PZL} and t_{PZH} are the same as t_{en}
- G. tpLH and tpHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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6 Detailed Description

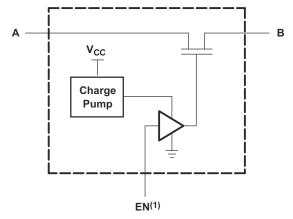
6.1 Overview

The SN74CB3Q3257 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3257 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3257 device is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable $(1\ \overline{OE},\ 2\ \overline{OE})$ inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When \overline{OE} is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



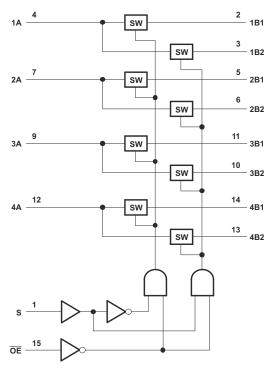
(1) EN is the internal enable signal applied to the switch.

Figure 6-1. Simplified Schematic, Each FET Switch (SW)

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6.2 Functional Block Diagram



6.3 Feature Description

The SN74CB3Q3257 device has a high-bandwidth data path (up to 500 MHz) and has 5V tolerant I/Os with the device powered up or powered down. It also has low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 4 Ω Typical).

This device also has rail-to-rail switching on data I/O ports for 0- to 5V switching with 3.3-V V_{CC} and 0- to 3.3V switching with 2.5V V_{CC} as well as bidirectional data flow with near-zero propagation delay and low input/output capacitance that minimizes loading and signal distortion ($C_{io(OFF)} = 3.5pF$ Typical).

The SN74CB3Q3257 also provides a fast switching frequency ($f_{\overline{OE}}$ = 20MHz Max) with data and control inputs that provide undershoot clamp diodes as well as low power consumption (I_{CC} = 0.6mA Typical).

The V_{CC} operating range is from 2.3V to 3.6V and the data I/Os support 0 to 5V signal levels of (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V).

The control inputs can be driven by TTL or 5V / 3.3V CMOS outputs as well as I_{off} Supports Partial-Power-Down Mode Operation.

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the SN74CB3Q3257.

Table 6-1. Function Table

INP	UTS	INPUT/OUTPUT	FUNCTION
ŌĒ	S	Α	FONCTION
L	L	B1	A port = B1 port
L	Н	B2	A port = B2 port
Н	Х	Z	Disconnect

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Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The SN74CB3Q3257 can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus being multiplexed between two devices, the OE and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

2 Typical Application

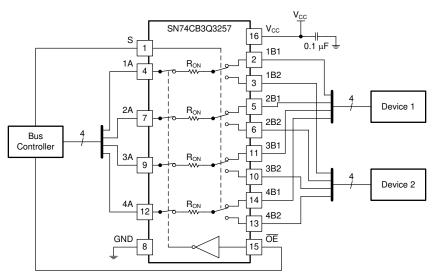


Figure 7-1. Typical Application of the SN74CB3Q3257

2.1 Design Requirements

- 1. Recommended Input Conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in Section 5.3.
 - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
- 2. Recommended Output Conditions:
 - Load currents should not exceed ±128mA per channel.
- 3. Frequency Selection Criterion:
 - Maximum frequency tested is 500MHz.
 - Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in Section 7.3.

2.2 Detailed Design Procedure

The 0.1µF capacitor should be place as close as possible to the device.

Product Folder Links: SN74CB3Q3257

2.3 Application Curve

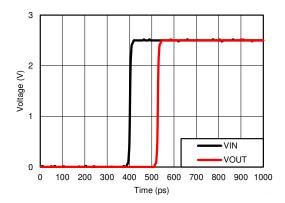


Figure 7-2. Propagation Delay (t_{pd}) Simulation Result at V_{CC} = 2.5V.

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the Section 5.1 table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a $0.1\mu F$ bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a $0.01\mu F$ or $0.022\mu F$ capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a $0.1\mu F$ bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of $0.1\mu F$ and $1\mu F$ are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

3 Layout

3.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 7-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

3.2 Layout Example

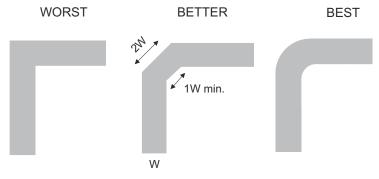


Figure 7-3. Trace Example



7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Implications of Slow or Floating CMOS Inputs
- Texas Instruments, Selecting the Right Texas Instruments Signal Switch

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

Changes from Revision D (July 2018) to Revision E (December 2024)	Page
Changed the Device Information table to the Package Information table	1
Changed the T _A MAX value from 85°C to 105°C in the Recommended Operating Conditions	
Changes from Revision C (April 2017) to Revision D (July 2018)	Page
Changed the pinout images appearance	3
Added Thermal Information table values	
Changes from Revision B (June 2015) to Revision C (April 2017)	Page
Added MAX values for T _A = -40°C to 105°C to the <i>Electrical Characteristics</i> table	5
• Added MAX values for $T_A = -40$ °C to 105°C to the Switching Characteristics, $V_{CC} = 2.5 \text{ V}$ table.	5
• Added separate Switching Characteristics, $V_{CC} = 3.3V$ for $V_{CC} = 3.3V \pm 0.3V$. Added TYP values	and MAX
values for T _A = –40°C to 105°C	

Product Folder Links: SN74CB3Q3257

Changes from Revision A (November 2003) to Revision B (June 2015)

Page

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(0)	(4)	(5)		(0)
SN74CB3Q3257DBQR	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DBQR.A	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DBQR.B	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257DGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257DGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257DGVR.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	BU257
SN74CB3Q3257PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257PWRG4.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU257
SN74CB3Q3257RGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257RGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257
SN74CB3Q3257RGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU257

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1



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*All dimensions are nominal

7 111 01111011010110 0110 11011111101							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3257DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CB3Q3257DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CB3Q3257PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74CB3Q3257PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CB3Q3257RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SHRINK SMALL-OUTLINE PACKAGE



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- 4. This dimension does not include interlead flash.5. Reference JEDEC registration MO-137, variation AB.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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