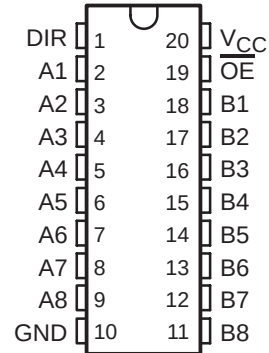


SN54BCT640, SN74BCT640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design
Substantially Reduces Standby Current
- Outputs Have Undershoot-Protection
Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC
Loading Effects
- ESD Protection Exceeds 2000 V
Per MIL-STD-883C, Method 3015
- Package Options Include Plastic
Small-Outline (DW) Packages, Ceramic
Chip Carriers (FK) and Flatpacks (W), and
Plastic and Ceramic 300-mil DIPs (J, N)

SN54BCT640 . . . J OR W PACKAGE
SN74BCT640 . . . DW OR N PACKAGE
(TOP VIEW)

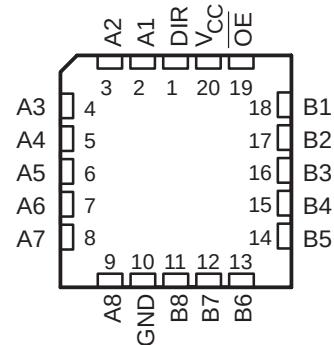


description

The 'BCT640 bus transceiver is designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{\text{OE}}$) input can be used to disable the device so that the buses are effectively isolated.

The SN54BCT640 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT640 is characterized for operation from 0°C to 70°C .

SN54BCT640 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	$\overline{\text{B}}$ data to A bus
L	H	$\overline{\text{A}}$ data to B bus
H	X	Isolation

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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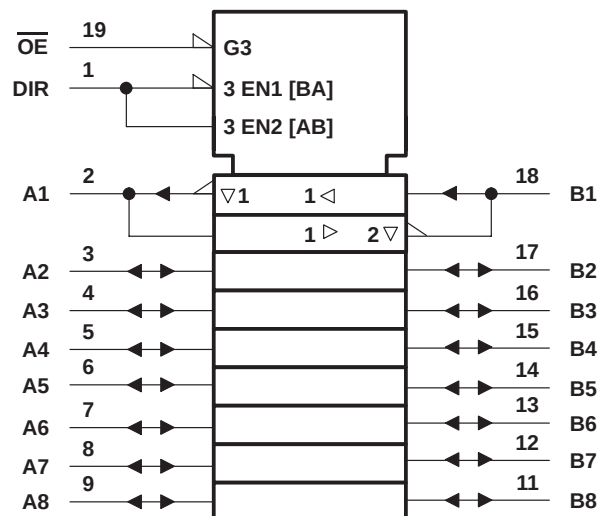
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SN54BCT640, SN74BCT640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

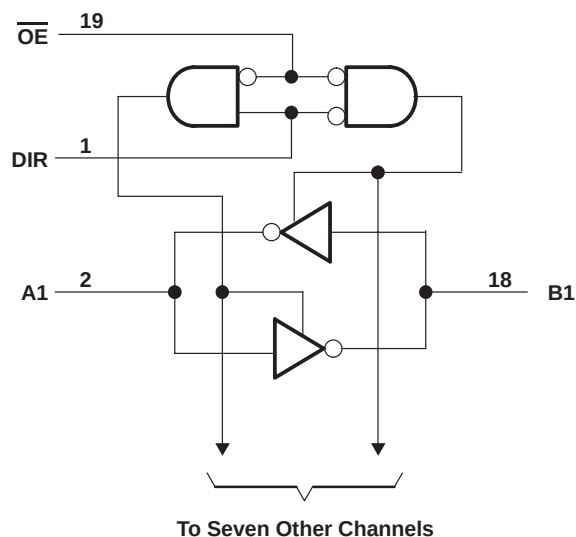
SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	– 0.5 V to 7 V
I/O ports (see Note 1)	– 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	– 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	– 0.5 V to V_{CC}
Input clamp current, I_{IK}	–30 mA
Current into any output in the low state: SN54BCT640	96 mA
SN74BCT640	128 mA
Operating free-air temperature range: SN54BCT640	– 55°C to 125°C
SN74BCT640	0°C to 70°C
Storage temperature range	– 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

SN54BCT640, SN74BCT640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

recommended operating conditions

			SN54BCT640			SN74BCT640			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{IK}	Input clamp current		−18			−18			mA
I _{OH}	High-level output current	A port	−3			−3			mA
		B port	−12			−15			
I _{OL}	Low-level output current	A port	20			24			mA
		B port	48			64			
T _A	Operating free-air temperature		−55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT640			SN74BCT640			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				-1.2			-1.2	V
V_{OH}	A port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		V
			$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		
	B port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		
			$I_{OH} = -12\text{ mA}$	2	3.2					
			$I_{OH} = -15\text{ mA}$				2	3.1		
V_{OL}	A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$		0.3	0.5				V
			$I_{OL} = 24\text{ mA}$					0.35	0.5	
	B port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.38	0.55				
			$I_{OL} = 64\text{ mA}$					0.42	0.55	
I_I	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$				1			1	mA
	Control inputs					0.1			0.1	
$I_{IH}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				70			70	μA
	Control inputs					20			20	
$I_{IL}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 0.5\text{ V}$				-0.6			-0.6	mA
	Control inputs					-0.65			-0.65	
$I_{OS}^\S$	A port	$V_{CC} = 5.5\text{ V}$, $V_O = 0$		-60		-150	-60		-150	mA
	B port			-100		-225	-100		-225	
I_{CCL}	A to B	$V_{CC} = 5.5\text{ V}$			53	84		53	94	mA
I_{CCH}	A to B	$V_{CC} = 5.5\text{ V}$			23	37		23	41	mA
I_{CCZ}		$V_{CC} = 5.5\text{ V}$			4	10		4	11	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



SN54BCT640, SN74BCT640

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS025C – SEPTEMBER 1988 – REVISED APRIL 1994

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†				UNIT
			'BCT640			SN54BCT640		SN74BCT640		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	0.5	3.6	5.6	0.5	7	0.5	6.5	ns
t _{PHL}			0.5	1.9	3.4	0.5	3.8	0.5	3.7	
t _{PZH}	$\overline{\text{OE}}$	A or B	3.1	6.4	8.9	2.6	10.5	2.6	10.2	ns
t _{PZL}			4.1	6.9	9.5	3.5	12.3	3.5	10.7	
t _{PHZ}	$\overline{\text{OE}}$	A or B	1.9	5	7.9	1.4	12.2	1.4	10.2	ns
t _{PLZ}			1.8	4.3	6.8	1.5	8.3	1.5	7.8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9075201M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9075201M2A SNJ54BCT 640FK
5962-9075201MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9075201MR A SNJ54BCT640J
5962-9075201MSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9075201MS A SNJ54BCT640W
SN74BCT640DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT640
SN74BCT640DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT640
SN74BCT640N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT640N
SN74BCT640N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT640N
SN74BCT640NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT640
SN74BCT640NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT640
SNJ54BCT640FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9075201M2A SNJ54BCT 640FK
SNJ54BCT640FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9075201M2A SNJ54BCT 640FK
SNJ54BCT640J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9075201MR A SNJ54BCT640J
SNJ54BCT640J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9075201MR A SNJ54BCT640J
SNJ54BCT640W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9075201MS A SNJ54BCT640W

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54BCT640W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9075201MS A SNJ54BCT640W

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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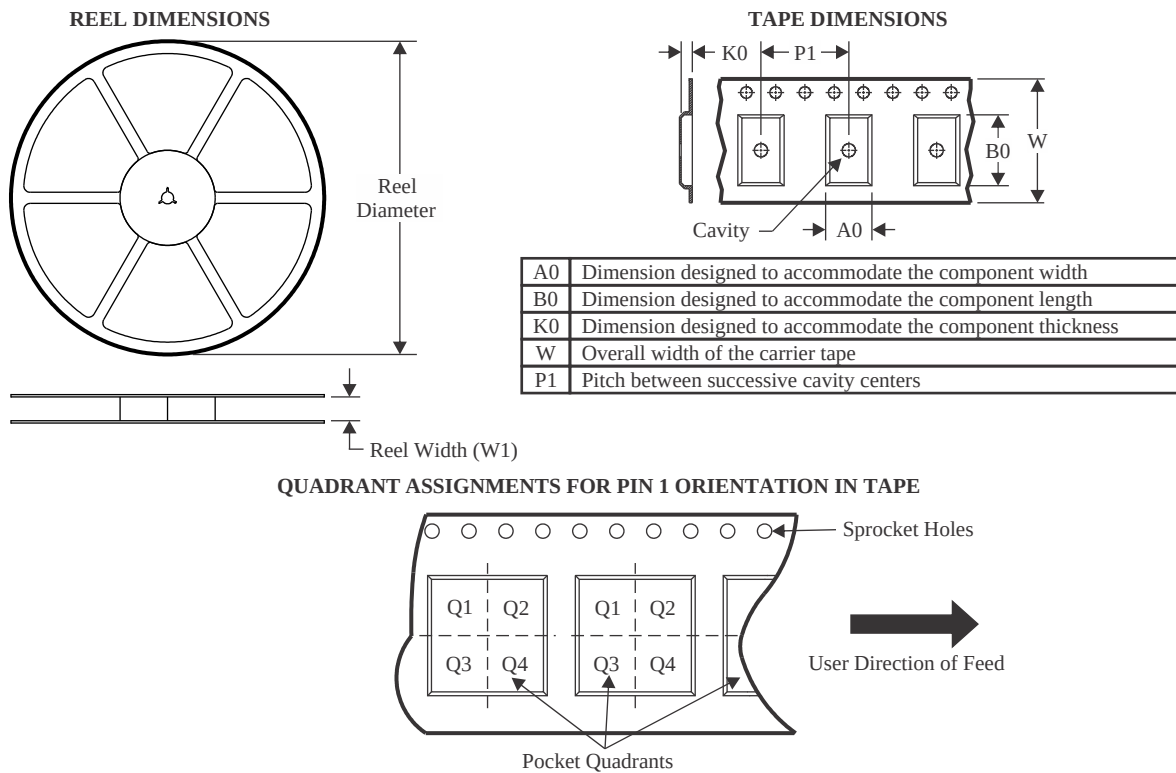
OTHER QUALIFIED VERSIONS OF SN54BCT640, SN74BCT640 :

- Catalog : [SN74BCT640](#)
- Military : [SN54BCT640](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

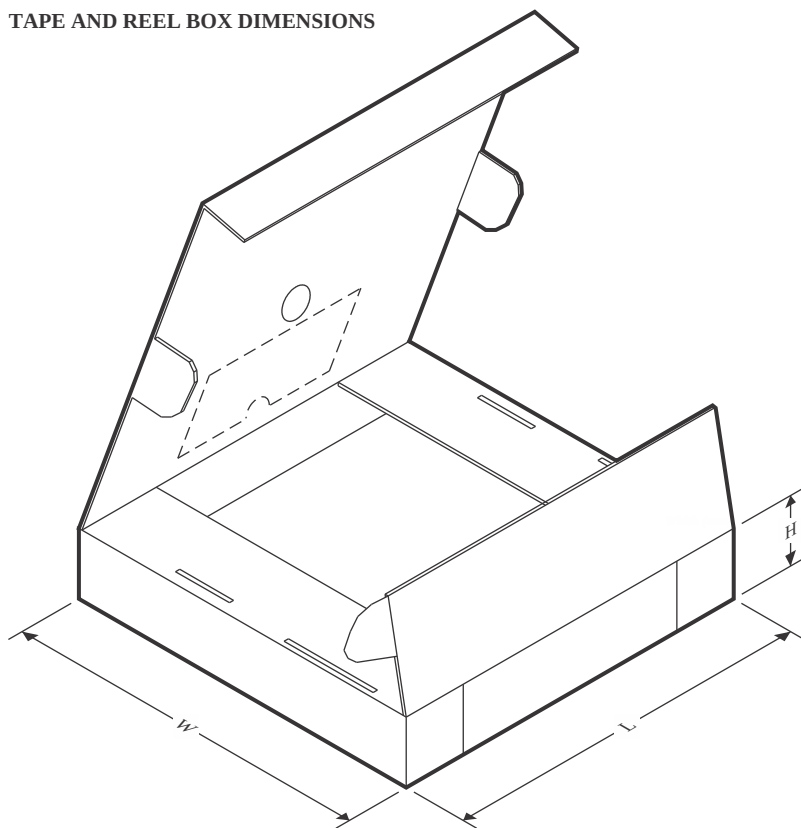
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT640NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT640NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

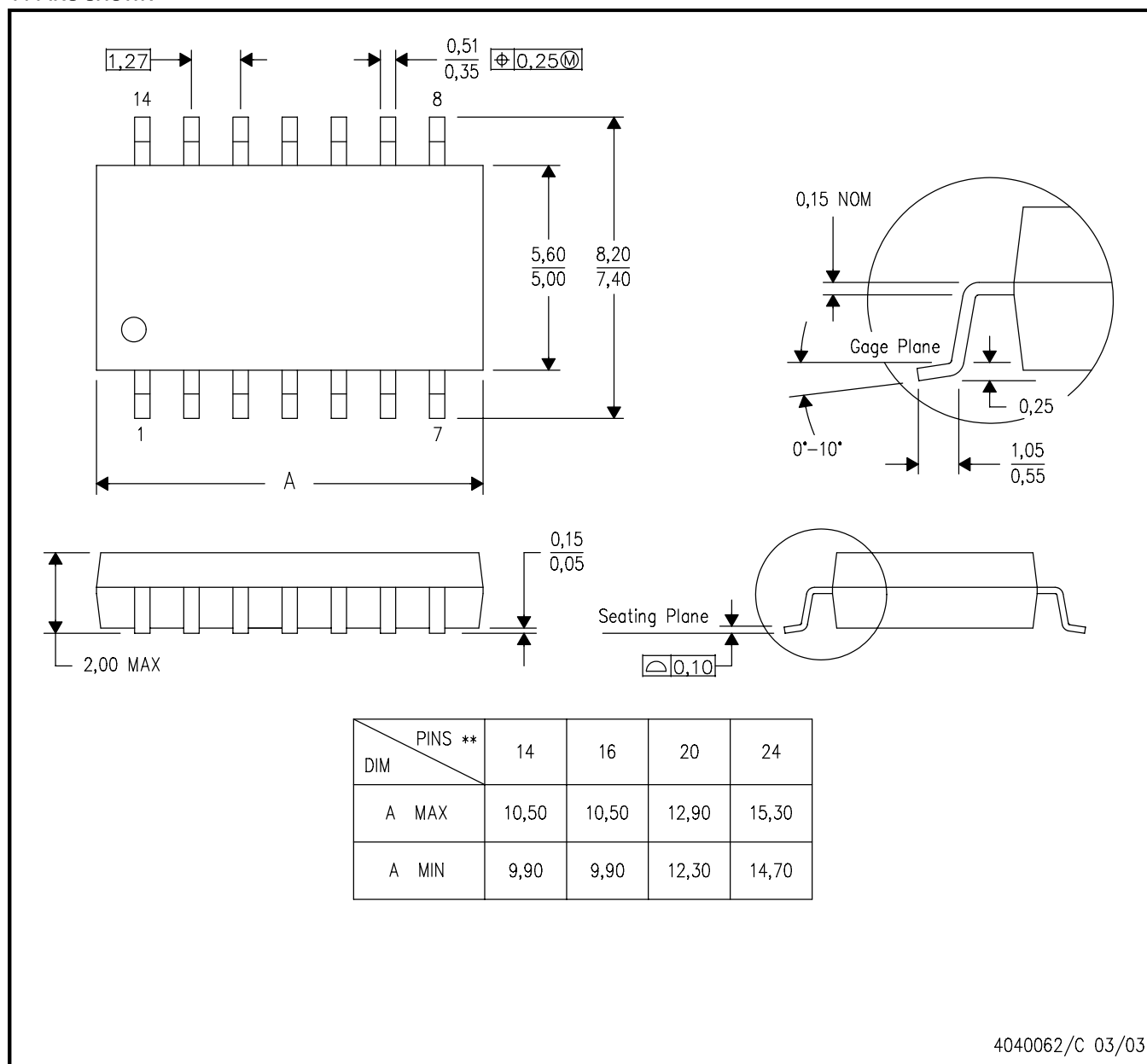
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9075201M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9075201MSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74BCT640DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT640DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT640N	N	PDIP	20	20	506	13.97	11230	4.32
SN74BCT640N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54BCT640FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT640FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT640W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54BCT640W.A	W	CFP	20	25	506.98	26.16	6220	NA

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

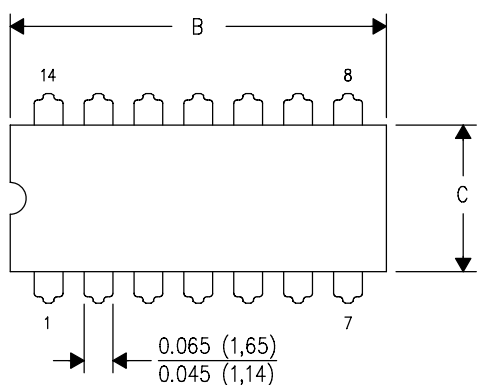


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

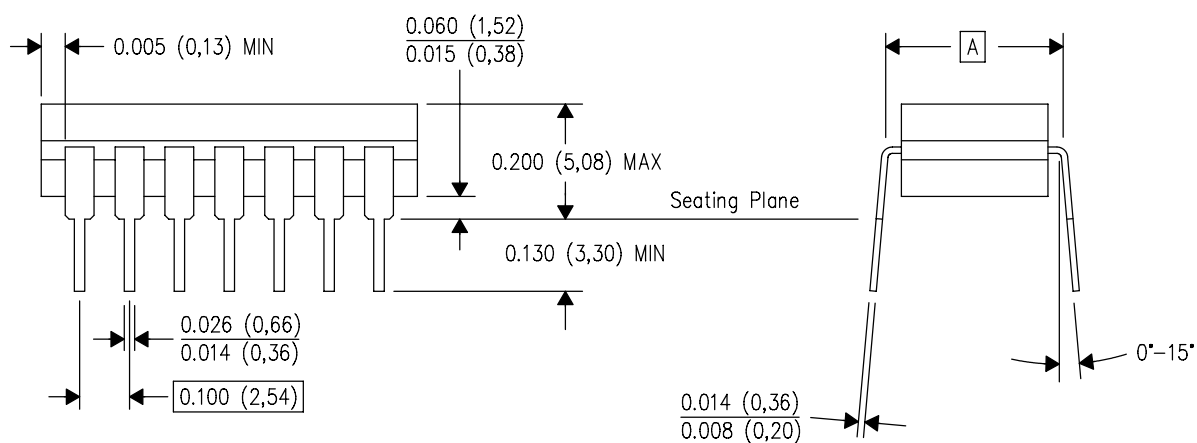
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

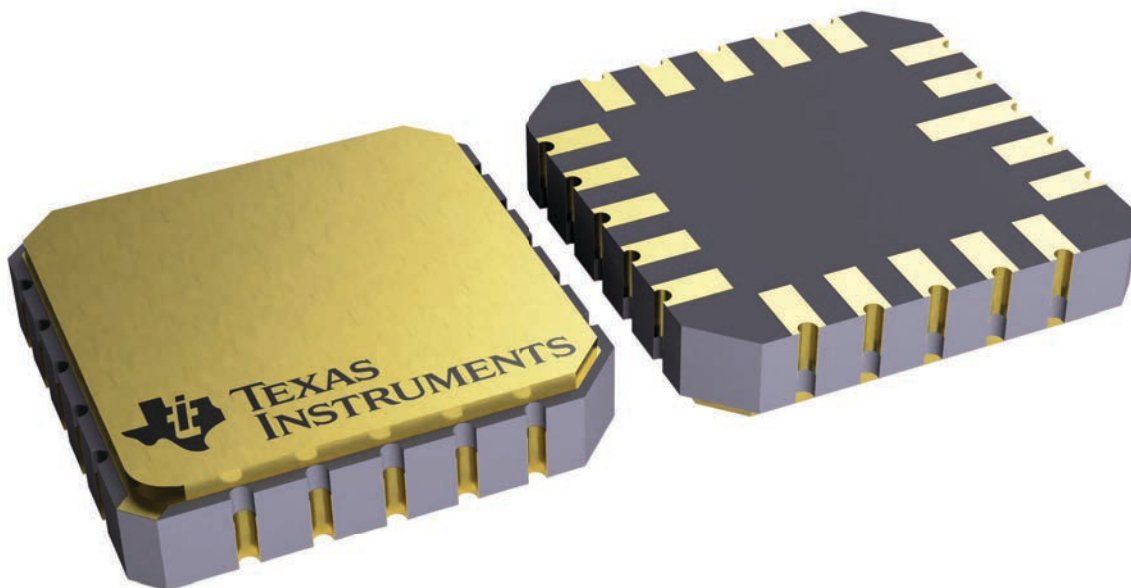
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

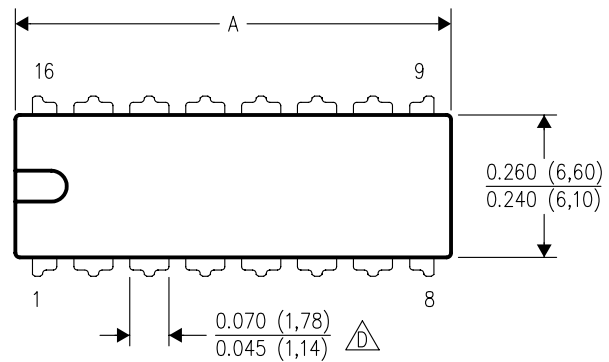


4229370VA\

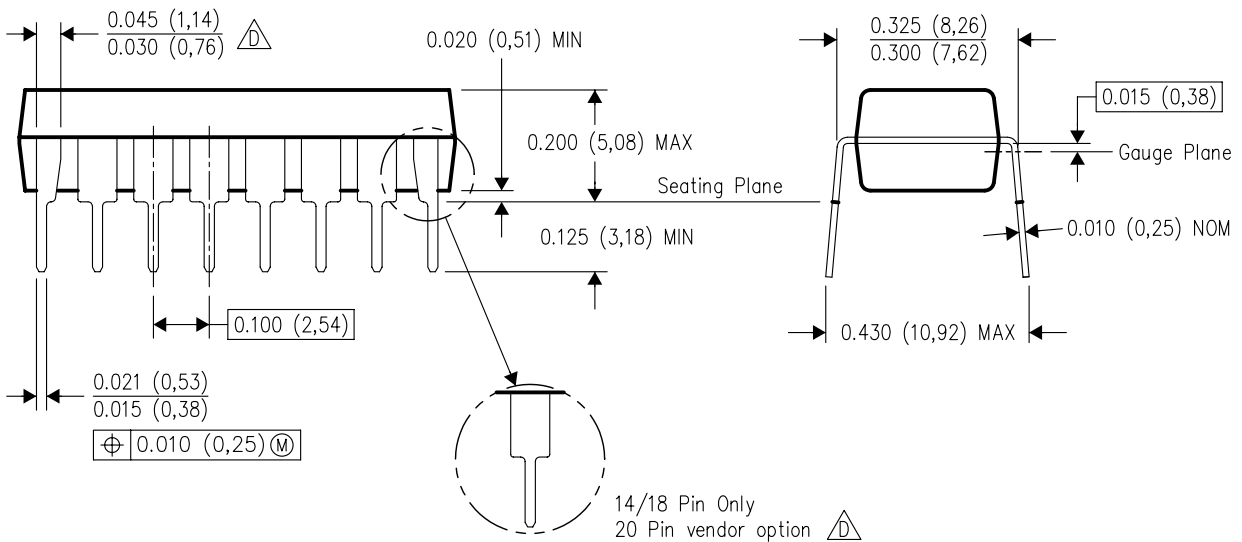
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



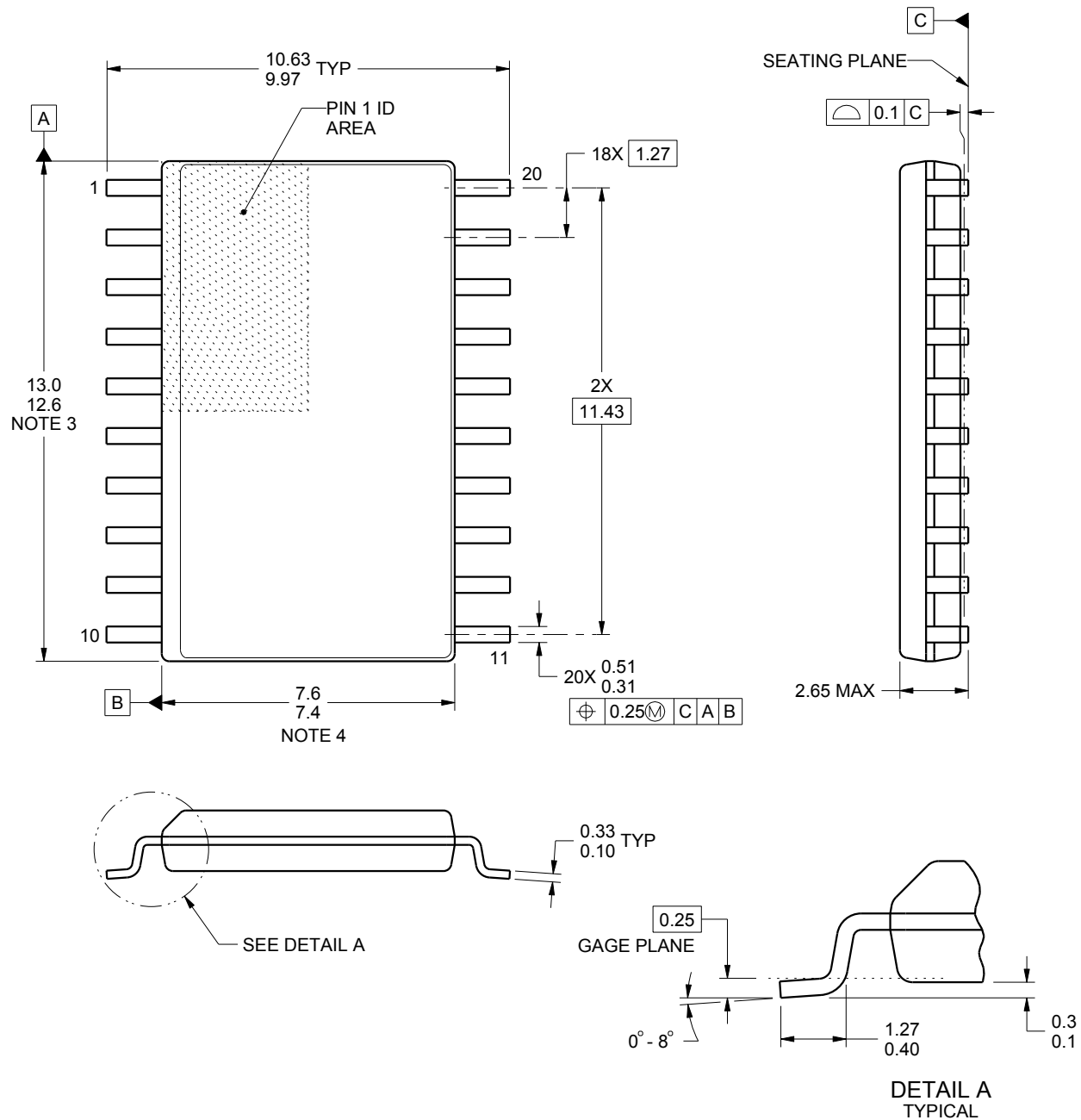
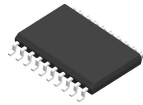
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

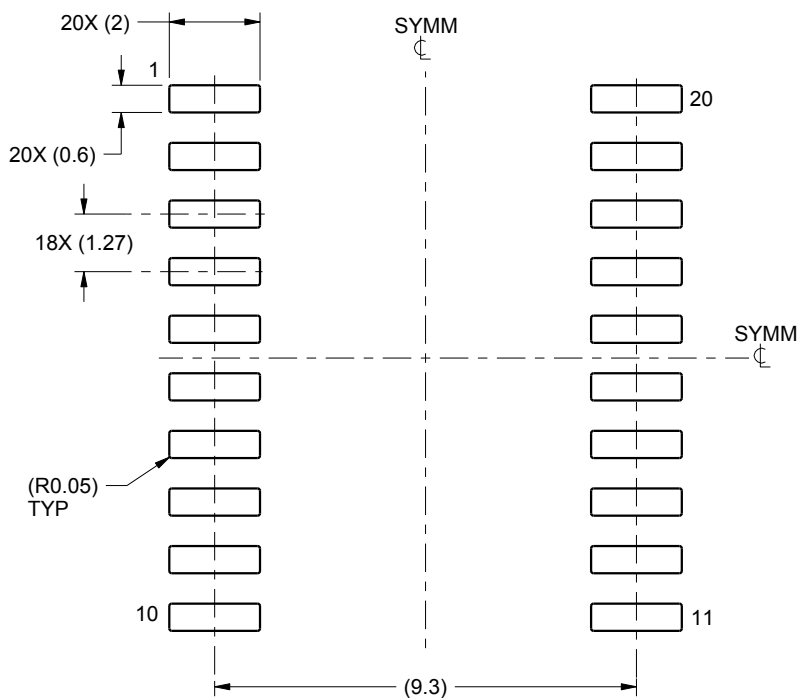
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

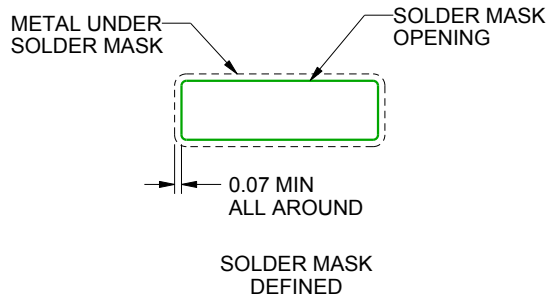
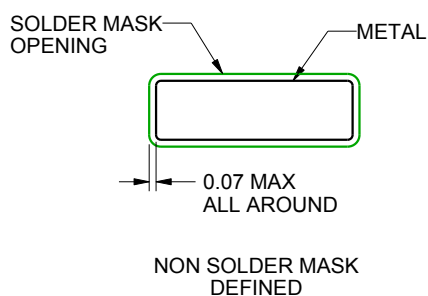
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

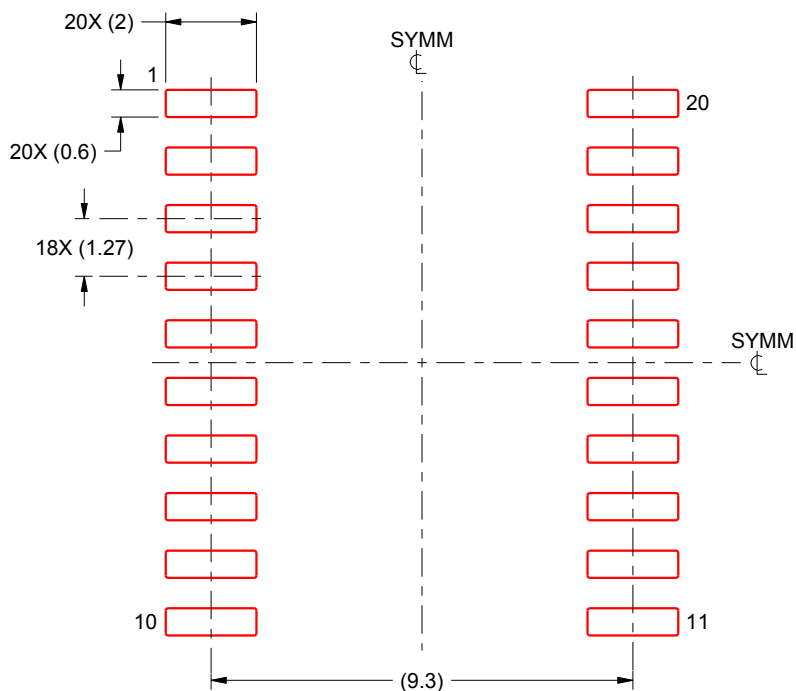
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

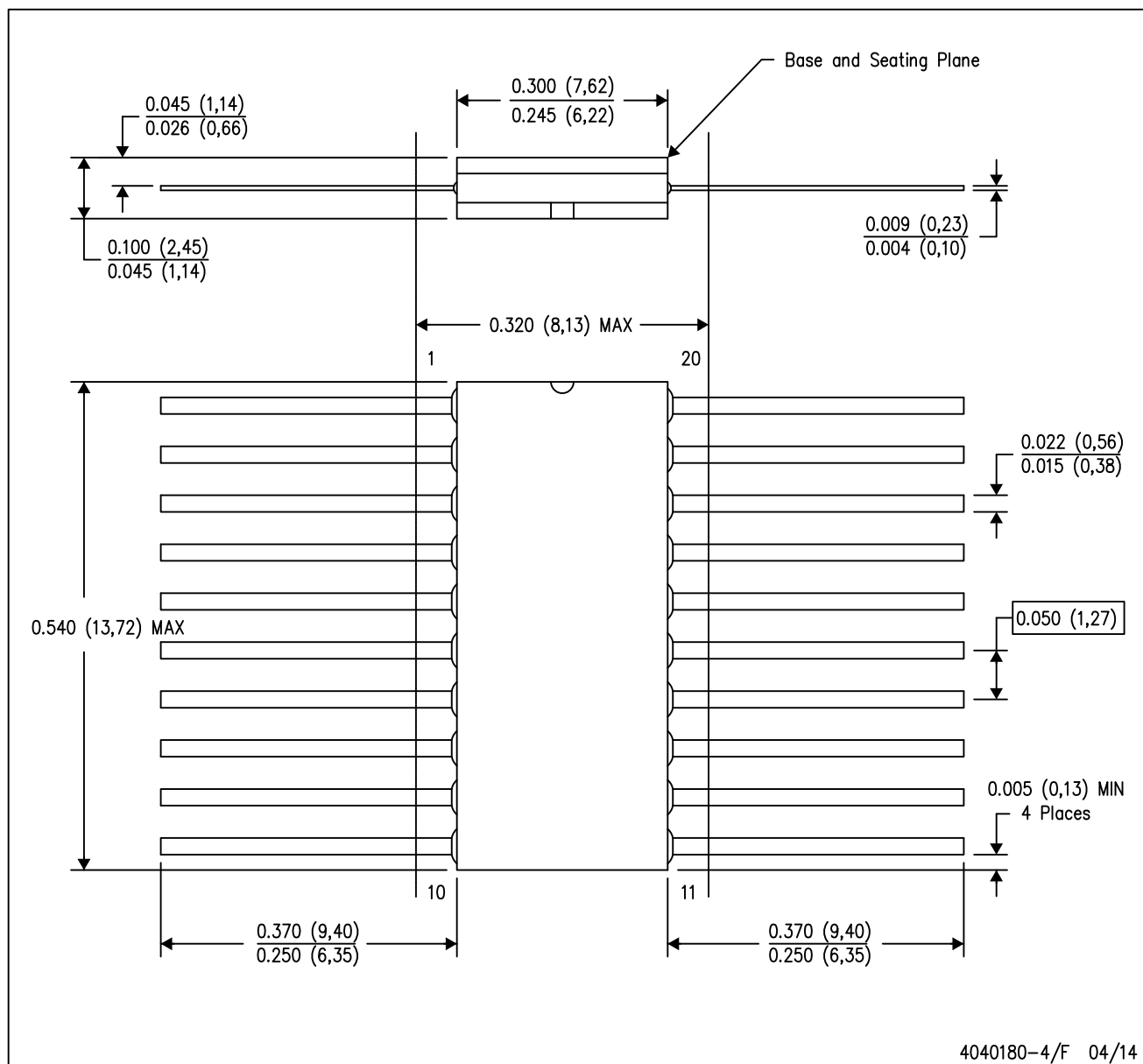
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

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