SCBS004F - OCTOBER 1987 - REVISED MARCH 2003

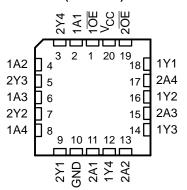
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}

SN54BCT240 . . . J OR W PACKAGE SN74BCT240 . . . DB, DW, N, OR NS PACKAGE (TOP VIEW)

1 <u>OE</u> [1	\bigcup_{20}] v _{cc}
1A1 [2	19] 2 <u>OE</u>
2Y4 [3	18] 1Y1
1A2 [4	17] 2A4
2Y3 [5	16] 1Y2
1A3 [6	15] 2A3
2Y2 [7	14] 1Y3
1A4 [8	13] 2A2
2Y1 [9	12] 1Y4
GND [10	11	2A1

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22
 2000-V Human-Body Model (A114-A)

SN54BCT240 . . . FK PACKAGE (TOP VIEW)



description/ordering information

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'BCT241 and 'BCT244 devices, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{\text{OE}}$ (active-low output-enable) inputs, and complementary $\overline{\text{OE}}$ inputs. These devices feature high fan-out and improved fan-in.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKA	GE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube	SN74BCT240N	SN74BCT240N		
	SOIC - DW	Tube	SN74BCT240DW	BCT240		
0°C to 70°C	301C - DVV	Tape and reel	SN74BCT240DWR	BC1240		
	SOP – NS Tape and r		SN74BCT240NSR	BCT240		
	SSOP – DB Tape and reel		SN74BCT240DBR	BT240		
	CDIP – J	Tube	SNJ54BCT240J	SNJ54BCT240J		
–55°C to 125°C	CFP – W	Tube	SNJ54BCT240W	SNJ54BCT240W		
	LCCC – FK	Tube	SNJ54BCT240FK	SNJ54BCT240FK		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



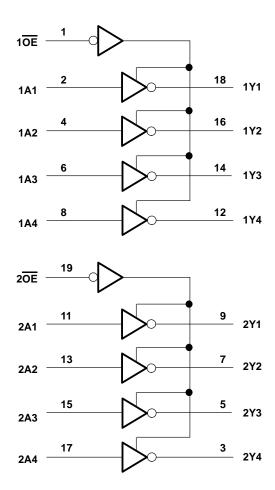
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FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT					
OE	Α	Y					
L	Н	L					
L	L	Н					
Н	Χ	Z					

logic diagram (positive logic)





SCBS004F - OCTOBER 1987 - REVISED MARCH 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Voltage range applied to any output in the disable	led or power-off state, VO	
Voltage range applied to any output in the high s	state, V _O	–0.5 V to V _{CC}
Input clamp current, I _{IK}		
Current into any output in the low state: SN54B	CT240	96 mA
SN74B	CT240	128 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	70°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
Storage temperature range, T _{sta}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54BCT240			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
liK	Input clamp current			-18			-18	mA
ЮН	High-level output current			-12			-15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SN54BCT240, SN74BCT240 **OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS**

SCBS004F - OCTOBER 1987 - REVISED MARCH 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			54BCT2	40	SN	UNIT		
PARAMETER	l E	SI CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
		$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		
Voн	V _{CC} = 4.5 V	$I_{OH} = -12 \text{ mA}$	2	3.2					V
		$I_{OH} = -15 \text{ mA}$				2	3.1		
Va	V00 - 45 V	$I_{OL} = 48 \text{ mA}$		0.38	0.55				V
VOL	V _{CC} = 4.5 V	$I_{OL} = 64 \text{ mA}$					0.42	0.55	V
lį	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
lН	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
I _{ΙL}	$V_{CC} = 5.5 \text{ V},$	V _I = 0.5 V			-1			-1	mA
IOZH	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
I _{OZL}	$V_{CC} = 5.5 \text{ V},$	V _O = 0.5 V			-50			-50	μΑ
I _{OS} ‡	V _{CC} = 5.5 V,	VO = 0	-100		-225	-100		-225	mA
ICCH	V _{CC} = 5.5 V,	Outputs open		19	31		19	31	mA
ICCL	$V_{CC} = 5.5 \text{ V},$	Outputs open		46	71		46	71	mA
Iccz	$V_{CC} = 5.5 \text{ V},$	Outputs open		6	9		6	9	mA
C _i	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		6			6		pF
Co	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		11			11		pF

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				
			'BCT240			SN54B		SN74BCT240			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
^t PLH	А	Y	0.5	3.3	4.8	0.5	6.4	0.5	5.6	ns	
^t PHL	٨	ľ	0.4	1.8	3.5	0.4	4.5	0.4	4	115	
^t PZH	ŌĒ	Y	1	6.4	7.9	1	9.2	1	8.8	ns	
^t PZL	OE	T T	1	7.5	9.4	1	10.8	1	10.5	113	
^t PHZ	ŌĒ	Y	1	6	6.8	1	8.5	1	8.1	ns	
t _{PLZ}	ŬL.	Υ	1	6.7	8.1	1	10.6	1	9.5	115	

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

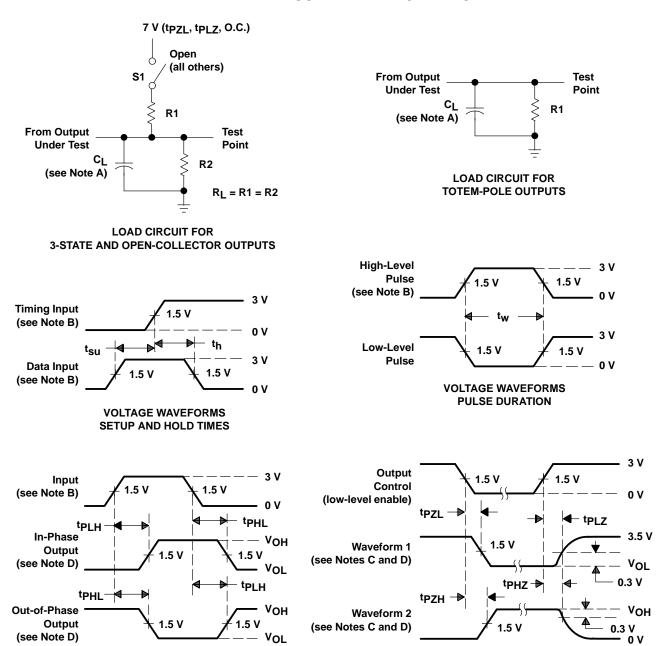


[†] All typical values are at V_{CC} = 5 V. ‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $t_f = t_f \leq 2.5$ ns, duty cycle = 50%.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9074201M2A	Active	Production	LCCC (FK) 20	55 TUBE No SNPB		N/A for Pkg Type	-55 to 125	5962- 9074201M2A SNJ54 BCT240FK	
5962-9074201MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074201MR A SNJ54BCT240J
5962-9074201MSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074201MS A SNJ54BCT240W
SN74BCT240DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT240
SN74BCT240DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT240
SN74BCT240N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT240N
SN74BCT240N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT240N
SN74BCT240NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT240
SN74BCT240NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT240
SNJ54BCT240FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9074201M2A SNJ54 BCT240FK
SNJ54BCT240FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9074201M2A SNJ54 BCT240FK
SNJ54BCT240J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074201MF A SNJ54BCT240J
SNJ54BCT240J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074201MI A SNJ54BCT240J
SNJ54BCT240W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074201MS A SNJ54BCT240W



www.ti.com	14-Oct-2025

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54BCT240W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9074201MS A SNJ54BCT240W

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54BCT240, SN74BCT240:

Catalog: SN74BCT240

Military: SN54BCT240

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

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NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025



*All dimensions are nominal

Device		Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT240	NSR	SOP	NS	20	2000	356.0	356.0	45.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9074201M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9074201MSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74BCT240DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT240DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT240N	N	PDIP	20	20	506	13.97	11230	4.32
SN74BCT240N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54BCT240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT240FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT240W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54BCT240W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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