







SN74AXC8T245-Q1

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SN74AXC8T245-Q1 Automotive 8-Bit Dual-Supply Bus Transceiver With Configurable **Voltage Translation and Tri-State Outputs**

1 Features

- AEC-Q100 qualified for automotive applications
- Available in wettable flank QFN (WRGY) package
- Qualified fully configurable dual-rail design allows each port to operate with a power supply range from 0.65V to 3.6V
- Operating temperature from -40°C to +125°C
- Multiple direction-control pins to allow simultaneous up and down translation
- Up to 380Mbps support when translating from 1.8V to 3.3V
- V_{CC} isolation feature to effectively Isolate both buses in a power-down scenario
- Partial power-down mode to limit backflow current in a power-down scenario
- Compatible with SN74AVC8T245-Q1 level shifter
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- Infotainment head unit
- **ADAS** fusion
- ADAS front camera
- HEV battery management system

3 Description

The SN74AXC8T245-Q1 AEC-Q100 qualified device is an 8-bit non-inverting bus transceiver that resolves voltage level mismatch between devices operating at the latest voltage nodes (0.7V, 0.8V, and 0.9V) and devices operating at industry standard voltage nodes (1.8V, 2.5V, and 3.3V) and vice versa.

The device operates by using two independent powersupply rails (V_{CCA} and V_{CCB}) that operate as low as 0.65V. Data pins A1 through A8 are designed to track V_{CCA}, which accepts any supply voltage from 0.65V to 3.6V. Data pins B1 through B8 are designed to track V_{CCB}, which accepts any supply voltage from 0.65V to 3.6V.

The SN74AXC8T245-Q1 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (DIR1 and DIR2). The output-enable (OE) input is used to disable the outputs so the buses are effectively isolated.

The SN74AXC8T245-Q1 device is designed so the control pins (DIR and \overline{OE}) are referenced to V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

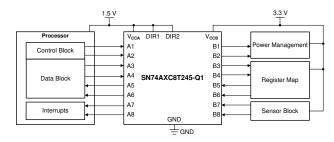
The V_{CC} isolation feature is designed so that if either V_{CC} input supply is below 100mV, all level shifter outputs are disabled and placed into a highimpedance state.

To put the level shifter I/Os in the high-impedance state during power up or power down, tie \overline{OE} to V_{CCA} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾				
	PW (TSSOP, 24)	7.8mm × 6.4mm				
SN74AXC8T245-Q1	RHL (VQFN, 24)	5.5mm × 3.5mm				
	RGY (VQFN, 24)	5.5mm × 3.5mm				

- (1) For more information, see Section 11
- (2)The package size (length × width) is a nominal value and includes pins, where applicable.



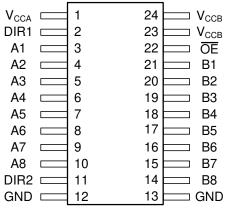
Typical Application Schematic

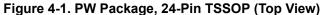


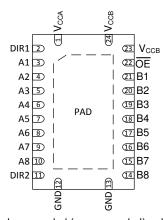
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4 Pin Configuration and Functions







PAD — may be grounded (recommended) or left floating.

Figure 4-2. RHL and WRGY Package, 24-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		DESCRIPTION						
NO.		DESCRIPTION						
3	I/O	Input/output A1. Referenced to V _{CCA} .						
4	I/O	Input/output A2. Referenced to V _{CCA} .						
5	I/O	Input/output A3. Referenced to V _{CCA} .						
6	I/O	Input/output A4. Referenced to V _{CCA} .						
7	I/O	Input/output A5. Referenced to V _{CCA} .						
8	I/O	Input/output A6. Referenced to V _{CCA} .						
9	I/O	Input/output A7. Referenced to V _{CCA} .						
10	I/O	Input/output A8. Referenced to V _{CCA} .						
	NO. 3 4 5 6 7 8 9	NO. 3 I/O 4 I/O 5 I/O 6 I/O 7 I/O 8 I/O 9 I/O						

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Table 4-1. Pin Functions (continued)

I	PIN	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	- ITPE\''	DESCRIPTION
B1	21	I/O	Input/output B1. Referenced to V _{CCB} .
B2	20	I/O	Input/output B2. Referenced to V _{CCB} .
B3	19	I/O	Input/output B3. Referenced to V _{CCB} .
B4	18	I/O	Input/output B4. Referenced to V _{CCB} .
B5	17	I/O	Input/output B5. Referenced to V _{CCB} .
B6	16	I/O	Input/output B6. Referenced to V _{CCB} .
B7	15	I/O	Input/output B7. Referenced to V _{CCB} .
B8	14	I/O	Input/output B8. Referenced to V _{CCB} .
DIR1	2	I	Direction-control signal 1. Referenced to V _{CCA} . Refer to Table 7-1.
DIR2	11	I	Direction-control signal 2. Refer to Table 7-1. Referenced to V _{CCA} . Tie to GND to maintain backward compatibility with SN74AVC8T245-Q1 device.
CND	12	_	Ground
GND	13	_	Ground
ŌĒ	22	ı	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA} . Refer to Table 7-1.
V _{CCA}	1	_	A-port supply voltage. 0.65V ≤ V _{CCA} ≤ 3.6V
V	23	_	B-port supply voltage. 0.65V ≤ V _{CCB} ≤ 3.6V
V _{CCB}	24	_	B-port supply voltage. 0.65V ≤ V _{CCB} ≤ 3.6V

⁽¹⁾ PAD - may be grounded (recommended) or left floating.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	,	MIN	MAX	UNIT		
Supply voltage, V _{CCA}		-0.5	4.2	V		
Supply voltage, V _{CCB}		-0.5	4.2	V		
	I/O ports (A port)	-0.5	4.2			
Input voltage, V _I ⁽²⁾	I/O ports (B port)	-0.5	4.2	V		
	Control inputs	-0.5	4.2			
Voltage applied to any output	A port	-0.5	4.2	V		
in the high-impedance or power-off state, $V_{O}^{(2)}$	B port	-0.5	4.2	V		
Valtage applied to any output in the high or law state (2) (3)	A port	-0.5	V _{CCA} + 0.2	V		
voltage applied to any output in the high of low state, $v_0 \leftarrow v_0$	B port	-0.5	V _{CCB} + 0.2	V		
Input clamp current, I _{IK}	V _I < 0	-50		mA		
Output clamp current, I _{OK}	V _O < 0	-50		mA		
Continuous output current, I _O	<u> </u>	-50	50	mA		
Continuous current through V _{CCA} , V _{CCB} , or GND		-100	100	mA		
Junction Temperature, T _J	blied to any output in the high or low state, V_O (2) (3) B port Current, I_{IK} $V_I < 0$ Proportion output current, I_{OK} $V_O < 0$ Current through V_{CCA} , V_{CCB} , or GND Imperature, T_J					
Storage temperature, T _{stg}	poplied to any output in the high or low state, V_{O} (2) (3) A port B port In pourrent, I_{IK} In pourrent, I_{OK} Is output current, I_{O} Is current through V_{CCA} , V_{CCB} , or GND Temperature, T_{J}					

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.2V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±8000	V
V _(ESD)	Liectiostatic discriarge	Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

				MIN	MAX	UNIT		
V _{CCA}	Supply voltage			0.65	3.6	V		
V _{CCB}	Supply voltage			0.65	3.6	V		
			V _{CCI} = 0.65V - 0.75V	V _{CCI} × 0.70				
			V _{CCI} = 0.76V - 1V	V _{CCI} × 0.70				
		Data inputs	V _{CCI} = 1.1V - 1.95V	V _{CCI} × 0.65				
			V _{CCI} = 2.3V - 2.7V	1.6				
,	High-level input voltage		V _{CCI} = 3V - 3.6V	2		V		
/ _{IH}	riigii-ievei iriput voitage		V _{CCA} = 0.65V - 0.75V	V _{CCA} × 0.70		V		
		Control inputs	V _{CCA} = 0.76V - 1V	V _{CCA} × 0.70				
		(DIR, OE)	V _{CCA} = 1.1V - 1.95V	V _{CCA} × 0.65				
		Referenced to V _{CCA}	V _{CCA} = 2.3V - 2.7V	1.6				
			V _{CCA} = 3V - 3.6V	2				
			V _{CCI} = 0.65V - 0.75V		V _{CCI} × 0.30			
			V _{CCI} = 0.76V - 1V		V _{CCI} × 0.30			
		Data inputs	V _{CCI} = 1.1V - 1.95V		V _{CCI} × 0.35			
			V _{CCI} = 2.3V - 2.7V		0.7			
V _{IL}	Low-level input voltage		V _{CCI} = 3V - 3.6V		0.8	V		
v IL	Low-level input voltage		V _{CCA} = 0.65V - 0.75V		V _{CCA} × 0.30	V		
		Control inputs	V _{CCA} = 0.76V - 1V		V _{CCA} × 0.30			
		(DIR, OE)	V _{CCA} = 1.1V - 1.95V		V _{CCA} × 0.35			
		Referenced to V _{CCA}	$V_{CCA} = 2.3V - 2.7V$		0.7			
			V _{CCA} = 3V - 3.6V		0.8			
√ _I	Input voltage ⁽³⁾			0	3.6	V		
1-	Output voltage	Active state		0	V _{CCO} (2)	V		
V _O	Output voitage	Tri-state		0	3.6	v		
∆t/Δv	Input transition rise or fall rate				10	ns/V		
T _A	Operating free-air temperature	e		-40	125	°C		

- V_{CCI} is the V_{CC} associated with the input port. V_{CCO} is the V_{CC} associated with the output port. All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. See the *Implications of Slow or Floating* CMOS Inputs application report.

5.4 Thermal Information

		SN	74AXC8T245-Q1	-Q1	
	THERMAL METRIC ⁽¹⁾	PW (TSSOP)	RHL (VQFN)	WRGY (VQFN)	UNIT
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.0	35.0	48.1	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	29.3	39.9	43.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	13.8	26.1	°C/W
ΨЈТ	Junction-to-top characterization parameter	1.5	0.3	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46.2	13.8	26.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.4	15.8	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



5.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

D/	ARAMETER	TEO	T CONDITIONS	V	V	-40°C	to 85°C		–40°C t	o 125°C		UNI
PA	ARAIVIETER	IES	CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP ⁽⁴⁾	MAX	MIN	TYP ⁽⁴⁾	MAX	UN
			$I_{OH} = -100 \mu A$	0.7V - 3.6V	0.7V - 3.6V	V _{CCO} – 0.1			V _{CCO} – 0.1			
			$I_{OH} = -50\mu A$	0.65V	0.65V	0.55			0.55			
			$I_{OH} = -200 \mu A$	0.76V	0.76V	0.58			0.58			
	High-level	V _I = V _{IH}	I _{OH} = -500μA	0.85V	0.85V	0.65			0.65			
/ _{OH}	output		I _{OH} = -3mA	1.1V	1.1V	0.85			0.85			\
	voltage		I _{OH} = -6mA	1.4V	1.4V	1.05			1.05			
			I _{OH} = -8mA	1.65V	1.65V	1.2			1.2			İ
			I _{OH} = -9mA	2.3V	2.3V	1.75			1.75			1
			I _{OH} = -12mA	3V	3V	2.3			2.3			1
			I _{OL} = 100μA	0.7V - 3.6V	0.7V - 3.6V			0.1			0.1	
			I _{OL} = 50μA	0.65V	0.65V			0.1			0.1	
			I _{OL} = 200μA	0.76V	0.76V			0.18			0.18	1
	Low-level		I _{OL} = 500μA	0.85V	0.85V			0.2			0.2	1
/ _{OL}		$V_I = V_{IL}$	I _{OL} = 3mA	1.1V	1.1V			0.25			0.25	\
			I _{OL} = 6mA	1.4V	1.4V			0.35			0.35	1
			I _{OL} = 8mA	1.65V	1.65V			0.45			0.45	1
			I _{OL} = 9mA	2.3V	2.3V		0.55				0.55	
			I _{OL} = 12mA	3V	3V			0.7			0.7	1
ı	Input leakage current	Control In	puts (DIR, OE): or GND	0.65V - 3.6V	0.65V - 3.6V	-0.5		0.5	-1		1	μ
	Partial power	A Port: V _I or V _O =	= 0V - 3.6V	0V	0V - 3.6V	-8		8	-12		12	
off	down current	B Port: V _I or V _O =	= 0V - 3.6V	0V - 3.6V	0V	-8		8	-12		12	- μ
OZ 3)	High- impedance	A Port: V _O = V _{CC} or GND, 0	O or GND, V _I = V _{CCI}	3.6V	3.6V	-8		8	-12		12	
3)	state output current	B Port: V _O = V _{CC} or GND, (O or GND, V _I = V _{CCI}	3.6V	3.6V	-8		8	-12		12	- μ
				0.65V - 3.6V	0.65V - 3.6V			20			40	
CCA	V _{CCA} supply current	V _I = V _{CCI}	or GND, $I_O = 0mA$	0V	3.6V	-2			-12			μ
	ourront			3.6V	0V			12			25	
				0.65V - 3.6V	0.65V - 3.6V			20			40	
ССВ	V _{CCB} supply current	V _I = V _{CCI}	or GND, I _O = 0mA	0V	3.6V			12		25		μ
	ourient			3.6V	0V	-2			-12			1
CCA - CCB	Combined supply current	V _I = V _{CCI} or GND, I _O = 0mA		0.65V - 3.6V	0.65V - 3.6V			30			60	μ
) _i	Input capacitance	Control In	puts (DIR, OE): or GND	3.3V	3.3V		4.5			4.5		р
C _{io}	Data I/O capacitance	Ports A ar OE = V _{CC} 1MHz -16	nd B: _{A,} V _O = 1.65V DC + dBm sine wave	3.3V	3.3V		5.7			5.7		p

 $[\]begin{array}{ll} \hbox{(1)} & V_{CCO} \text{ is the V_{CC} associated with the output port.} \\ \hbox{(2)} & V_{CCI} \text{ is the V_{CC} associated with the input port.} \\ \hbox{(3)} & \text{For I/O ports, the parameter I_{OZ} includes the input leakage current.} \\ \hbox{(4)} & \text{All typical values are for T_A} = 25^{\circ}\text{C} \\ \end{array}$



5.6 Switching Characteristics, $V_{CCA} = 0.7V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-POR	T SUPPLY \	OLTAGE (V _{CCB})			
P/	ARAMETER	TEST CONDITIONS		0.7V	0.7V ± 0.05V		0.8V ± 0.04V		0.9V ± 0.045V		± 0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A to output B	-40°C to 85°C	0.5	172	0.5	114	0.5	82	0.5	49	
	Propagation		–40°C to 125°C	0.5	172	0.5	114	0.5	82	0.5	49]
t _{pd}	delay	From input B to output A	–40°C to 85°C	0.5	172	0.5	153	0.5	126	0.5	88	ns
			–40°C to 125°C	0.5	172	0.5	153	0.5	126	0.5	88	
		From input OE to output A	–40°C to 85°C	0.5	192	0.5	192	0.5	192	0.5	192	ns
	Disable time		–40°C to 125°C	0.5	195	0.5	195	0.5	195	0.5	195	
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	156	0.5	129	0.5	118	0.5	120	
		to output B	–40°C to 125°C	0.5	157	0.5	129	0.5	120	0.5	122	
		From input OE	–40°C to 85°C	0.5	237	0.5	237	0.5	237	0.5	237	
	Carlo dias	to output A	-40°C to 125°C	0.5	237	0.5	237	0.5	237	0.5	237]
t _{en}	Enable time	From input OE to output B	-40°C to 85°C	0.5	223	0.5	145	0.5	106	0.5	74	ns
			-40°C to 125°C	0.5	223	0.5	145	0.5	106	0.5	74	1

Switching Characteristics, $V_{CCA} = 0.7V$

						B-POR	T SUPPLY \	/OLTAGE (V _{CCB})			
Р	ARAMETER	TEST CONDITIONS		1.5V	1.5V ± 0.1V		1.8V ± 0.15V		± 0.2V	3.3V ± 0.3V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A to output B	-40°C to 85°C	0.5	46	0.5	49	0.5	61	0.5	142	
	Propagation		–40°C to 125°C	0.5	46	0.5	49	0.5	61	0.5	142	no.
t _{pd}	delay	From input B to output A	–40°C to 85°C	0.5	83	0.5	82	0.5	81	0.5	81	ns
			-40°C to 125°C	0.5	83	0.5	82	0.5	81	0.5	81	
		From input OE to output A	–40°C to 85°C	0.5	192	0.5	192	0.5	192	0.5	192	ns
	Disable time		-40°C to 125°C	0.5	195	0.5	195	0.5	195	0.5	195	
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	69	0.5	66	0.5	67	0.5	150	
		to output B	-40°C to 125°C	0.5	70	0.5	67	0.5	67	0.5	150	
		From input OE	–40°C to 85°C	0.5	237	0.5	237	0.5	237	0.5	237	
	Enable time	to output A	-40°C to 125°C	0.5	237	0.5	237	0.5	237	0.5	237	ns
t _{en}	Enable time	From input OE to output B	–40°C to 85°C	0.5	68	0.5	69	0.5	84	0.5	552	
			-40°C to 125°C	0.5	68	0.5	69	0.5	84	0.5	552	



5.7 Switching Characteristics, $V_{CCA} = 0.8V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-POR	T SUPPLY	VOLTAGE	(V _{CCB})			
P	ARAMETER	TEST CONDITIONS		0.7V :	0.7V ± 0.05V		0.8V ± 0.04V		0.9V ± 0.045V		1.2V ± 0.1V	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A to output B	-40°C to 85°C	0.5	153	0.5	95	0.5	62	0.5	32	
	Propagation		-40°C to 125°C	0.5	153	0.5	95	0.5	62	0.5	32]
t _{pd}	delay	From input B to output A	-40°C to 85°C	0.5	114	0.5	95	0.5	78	0.5	52	- ns
			-40°C to 125°C	0.5	114	0.5	95	0.5	78	0.5	52	
		From input OE to output A	-40°C to 85°C	0.5	101	0.5	101	0.5	101	0.5	101	- ns
	Disable time		-40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	
t _{dis}	Disable time	From input OE	-40°C to 85°C	0.5	141	0.5	114	0.5	104	0.5	106	
		to output B	-40°C to 125°C	0.5	142	0.5	115	0.5	106	0.5	109	1
		From input OE	-40°C to 85°C	0.5	102	0.5	102	0.5	102	0.5	102	
	Enable time	to output A	-40°C to 125°C	0.5	102	0.5	102	0.5	102	0.5	102	1
t _{en}	Enable time	From input OE to output B	-40°C to 85°C	0.5	202	0.5	124	0.5	86	0.5	52	ns
			-40°C to 125°C	0.5	202	0.5	124	0.5	86	0.5	52	

Switching Characteristics, $V_{CCA} = 0.8V$

			. 00A			B-POR	T SUPPLY	VOLTAGE (V _{CCB})			
P	ARAMETER	TEST C	ONDITIONS	1.5V	± 0.1V	1.8V ±	0.15V	2.5V ±	: 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	26	0.5	25	0.5	25	0.5	35	
	Propagation	to output B	-40°C to 125°C	0.5	26	0.5	25	0.5	25	0.5	35]
t _{pd}	delay	to output A	-40°C to 85°C	0.5	42	0.5	41	0.5	40	0.5	40	ns
	to output A	-40°C to 125°C	0.5	42	0.5	41	0.5	40	0.5	40		
	Fr	From input OE	-40°C to 85°C	0.5	101	0.5	101	0.5	101	0.5	101	
	Disable time	to output A	-40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	
t _{dis}	Disable time		-40°C to 85°C	0.5	55	0.5	51	0.5	49	0.5	51	ns
		to output B	-40°C to 125°C	0.5	57	0.5	53	0.5	50	0.5	52	
	From input Oi to output A	From input OE	-40°C to 85°C	0.5	102	0.5	102	0.5	102	0.5	102	
		to output A	-40°C to 125°C	0.5	102	0.5	102	0.5	102	0.5	102	
Len		From input OE	-40°C to 85°C	0.5	44	0.5	43	0.5	45	0.5	58	ns
		to output B	-40°C to 125°C	0.5	44	0.5	43	0.5	45	0.5	58	1

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5.8 Switching Characteristics, $V_{CCA} = 0.9V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-POR	SUPPLY \	/OLTAGE	(V _{CCB})			
P/	ARAMETER	TEST CO	ONDITIONS	0.7V ±	t 0.05V	0.8V ±	0.04V	0.9V ±	t 0.045V	1.2V	± 0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	127	0.5	78	0.5	52	0.5	23	
	Propagation	to output B	-40°C to 125°C	0.5	127	0.5	78	0.5	52	0.5	23	
t _{pd}	F	From input B	-40°C to 85°C	0.5	82	0.5	63	0.5	52	0.5	39	ns
		to output A	-40°C to 125°C	0.5	82	0.5	63	0.5	52	0.5	39	
		From input OE	–40°C to 85°C	0.5	125	0.5	125	0.5	125	0.5	125	
	to	to output A	-40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	, no
t _{dis}	Disable time	From input OE	-40°C to 85°C	0.5	131	0.5	105	0.5	96	0.5	99	ns
		to output B	-40°C to 125°C	0.5	133	0.5	107	0.5	98	0.5	101	
		From input OE	-40°C to 85°C	0.5	124	0.5	124	0.5	124	0.5	124	
	Enable time	to output A	-40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	1
t _{en}	Enable time	From input OE	-40°C to 85°C	0.5	191	0.5	113	0.5	75	0.5	41	ns
		to output B	-40°C to 125°C	0.5	191	0.5	113	0.5	75	0.5	41	1

Switching Characteristics, V_{CCA} = 0.9V

						B-POF	RT SUPPLY	VOLTAGE	(V _{CCB})			
P	ARAMETER	TEST C	ONDITIONS	1.5V	± 0.1V	1.8V	± 0.15V	2.5V	± 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	17	0.5	15	0.5	14	0.5	17	
	Propagation	to output B	-40°C to 125°C	0.5	17	0.5	15	0.5	14	0.5	17]
t _{pd}	delay From input B to output A	–40°C to 85°C	0.5	28	0.5	24	0.5	22	0.5	22	ns	
		to output A	-40°C to 125°C	0.5	28	0.5	24	0.5	22	0.5	22	
		From input OE	–40°C to 85°C	0.5	125	0.5	125	0.5	125	0.5	125	
	From input OE to output A Disable time	-40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128		
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	47	0.5	44	0.5	40	0.5	73	ns
	to o	to output B	-40°C to 125°C	0.5	50	0.5	46	0.5	42	0.5	73	
		From input OE	–40°C to 85°C	0.5	124	0.5	124	0.5	124	0.5	124	
		to output A	-40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
t _{en}	Enable time	From input OE	-40°C to 85°C	0.5	34	0.5	32	0.5	31	0.5	35	ns
		to output B	-40°C to 125°C	0.5	34	0.5	32	0.5	31	0.5	35	1



5.9 Switching Characteristics, $V_{CCA} = 1.2V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-PORT	SUPPLY V	OLTAGE	(V _{CCB})			
PA	RAMETER	TEST C	ONDITIONS	0.7V :	± 0.05V	0.8V	± 0.04V	0.9V ±	0.045V	1.2V	± 0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	–40°C to 85°C	0.5	88	0.5	52	0.5	39	0.5	15	
	Propagation	to output B	-40°C to 125°C	0.5	88	0.5	52	0.5	39	0.5	15	ns
t _{pd}	delay	From input B	–40°C to 85°C	0.5	49	0.5	32	0.5	23	0.5	15	115
	to output A From input	-40°C to 125°C	0.5	49	0.5	32	0.5	23	0.5	15		
	(–40°C to 85°C	0.5	87	0.5	87	0.5	87	0.5	87	
.		OE to output A	-40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	ns
t _{dis}	Disable tillle	From input	–40°C to 85°C	0.5	119	0.5	94	0.5	85	0.5	89	115
		-40°C to 125°C	0.5	121	0.5	96	0.5	88	0.5	93		
		From input	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	
	en Enable time OE to OE	OE to output A	-40°C to 125°C	0.5	36	0.5	36	0.5	36	0.5	36	ns
^L en		From input	–40°C to 85°C	0.5	168	0.5	98	0.5	61	0.5	29	115
		OE to output B	-40°C to 125°C	0.5	168	0.5	98	0.5	61	0.5	30	

Switching Characteristics, $V_{CCA} = 1.2V$

						B-POI	RT SUPPLY	VOLTAGE	(V _{CCB})			
P.	ARAMETER	TEST C	ONDITIONS	1.5V	± 0.1V	1.8V	± 0.15V	2.5V	± 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	10	0.5	9	0.5	7	0.5	7	
	Propagation	to output B	-40°C to 125°C	0.5	10	0.5	9	0.5	7	0.5	8	ns
t _{pd}	delay	From input B to output A	-40°C to 85°C	0.5	13	0.5	11	0.5	8	0.5	7	1 115
		to output A	-40°C to 125°C	0.5	13	0.5	11	0.5	8	0.5	7	
		From input OE	-40°C to 85°C	0.5	87	0.5	87	0.5	87	0.5	87	
	Disable time	to output A	-40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	ns
t _{dis}	Disable time	From input OE	-40°C to 85°C	0.5	38	0.5	35	0.5	31	0.5	29	1 115
		to output B	-40°C to 125°C	0.5	41	0.5	38	0.5	33	0.5	31	
	From input \overline{OE} to output A From input \overline{OE} to output B	-40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34		
		to output A	-40°C to 125°C	0.5	36	0.5	36	0.5	36	0.5	36	
Len		From input OE	-40°C to 85°C	0.5	22	0.5	19	0.5	17	0.5	17	ns
		to output B	-40°C to 125°C	0.5	23	0.5	20	0.5	18	0.5	18	

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5.10 Switching Characteristics, $V_{CCA} = 1.5V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-POR	T SUPPLY \	/OLTAGE (V _{CCB})			
P	ARAMETER	TEST CO	NDITIONS	0.7V :	t 0.05V	0.8V ±	0.04V	0.9V ±	0.045V	1.2V ±	0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	84	0.5	42	0.5	28	0.5	13	
	Propagation	to output B	–40°C to 125°C	0.5	84	0.5	42	0.5	28	0.5	13	ns
t _{pd}	· uelay	From input B	-40°C to 85°C	0.5	46	0.5	26	0.5	17	0.5	10	115
		to output A	-40°C to 125°C	0.5	46	0.5	26	0.5	17	0.5	10	
		From input OE	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	
	Disable time	to output A	–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	115	0.5	89	0.5	80	0.5	85	ns
		to output B	–40°C to 125°C	0.5	117	0.5	91	0.5	83	0.5	89	
		From input OE	–40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	
t _{en}	Enable time	to output A	-40°C to 125°C	0.5	23	0.5	23	0.5	23	0.5	23	
	Enable time	From input OE	–40°C to 85°C	0.5	159	0.5	90	0.5	55	0.5	24	ns
		to output B	-40°C to 125°C	0.5	159	0.5	90	0.5	55	0.5	25	

Switching Characteristics, $V_{CCA} = 1.5V$

						B-POR	T SUPPLY	VOLTAGE	(V _{CCB})			
ı	PARAMETER	TEST CC	NDITIONS	1.5V	± 0.1V	1.8V :	± 0.15V	2.5V	± 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	9	0.5	7	0.5	6	0.5	5	
	Propagation	to output B	–40°C to 125°C	0.5	9	0.5	7	0.5	6	0.5	6	no
t _{pd}	delay From input B to output A	-40°C to 85°C	0.5	9	0.5	7	0.5	6	0.5	5	ns	
		to output A	-40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	5	
		From input OE	-40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	
	D: 11 ''	to output A	-40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	no
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	35	0.5	31	0.5	28	0.5	25	ns
		to output B	–40°C to 125°C	0.5	38	0.5	34	0.5	31	0.5	27	
		From input OE	–40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	
	Enable time	to output A	–40°C to 125°C	0.5	23	0.5	23	0.5	23	0.5	23	
t _{en}	Enable time	From input OE	–40°C to 85°C	0.5	17	0.5	15	0.5	12	0.5	11	ns
		to output B	-40°C to 125°C	0.5	18	0.5	15	0.5	13	0.5	12	



5.11 Switching Characteristics, V_{CCA} = 1.8V

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-PORT	SUPPLY V	OLTAGE (V _{CCB})			
F	PARAMETER	TEST CO	NDITIONS	0.7V	± 0.05V	0.8V	t 0.04V	0.9V ±	0.045V	1.2V	± 0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	82	0.5	41	0.5	24	0.5	11	
	Propagation	to output B	-40°C to 125°C	0.5	82	0.5	41	0.5	24	0.5	11	ns
t _{pd}	· uelay	From input B	-40°C to 85°C	0.5	49	0.5	25	0.5	15	0.5	9	115
		to output A	-40°C to 125°C	0.5	49	0.5	25	0.5	15	0.5	9	
		From input OE	-40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	
	Disable time	to output A	-40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
t _{dis}	Disable time	From input OE	-40°C to 85°C	0.5	113	0.5	87	0.5	78	0.5	83	ns
		to output B	-40°C to 125°C	0.5	115	0.5	89	0.5	81	0.5	87	
		From input OE	-40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	
t _{en}	Enable time	to output A	-40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	
	Enable time	From input OE	-40°C to 85°C	0.5	157	0.5	88	0.5	54	0.5	23	ns
		to output B	-40°C to 125°C	0.5	157	0.5	88	0.5	54	0.5	23	

Switching Characteristics, $V_{CCA} = 1.8V$

						B-POR	T SUPPLY \	/OLTAGE ((V _{CCB})			
F	PARAMETER	TEST CO	NDITIONS	1.5V :	± 0.1V	1.8V :	± 0.15V	2.5V	± 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	8	0.5	6	0.5	5	0.5	5	
	Propagation	to output B	-40°C to 125°C	0.5	8	0.5	7	0.5	6	0.5	5	ns
t _{pd}	delay	From input B	-40°C to 85°C	0.5	7	0.5	6	0.5	5	0.5	4	1115
	to	to output A	-40°C to 125°C	0.5	7	0.5	7	0.5	5	0.5	4	
		From input OE	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	
	Disable time	to output A	-40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	33	0.5	30	0.5	27	0.5	57	ns
		to output B	-40°C to 125°C	0.5	36	0.5	33	0.5	29	0.5	60	
	From input to output A	From input OE	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	
		to output A	-40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	
Len		From input OE	-40°C to 85°C	0.5	15	0.5	13	0.5	10	0.5	9	ns
		to output B	-40°C to 125°C	0.5	16	0.5	14	0.5	11	0.5	10	

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5.12 Switching Characteristics, $V_{CCA} = 2.5V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-PORT	SUPPLY V	OLTAGE (V _{CCB})			
P	ARAMETER	TEST CO	NDITIONS	0.7V :	± 0.05V	0.8V	± 0.04V	0.9V ±	0.045V	1.2V	± 0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	81	0.5	40	0.5	22	0.5	8	
	Propagation	to output B	-40°C to 125°C	0.5	81	0.5	40	0.5	22	0.5	8	no
t _{pd}	^{od} delay	From input B	-40°C to 85°C	0.5	61	0.5	25	0.5	14	0.5	7	ns
		to output A	-40°C to 125°C	0.5	61	0.5	25	0.5	14	0.5	7	
		From input OE	-40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	
	Disable time	to output A	-40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	no
t _{dis}	Disable time	From input OE	-40°C to 85°C	0.5	111	0.5	85	0.5	76	0.5	81	ns
		to output B	-40°C to 125°C	0.5	113	0.5	87	0.5	78	0.5	84	
		From input OE	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	
t _{en}	Enable time	to output A	-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	no
	Enable time	From input OE	-40°C to 85°C	0.5	155	0.5	86	0.5	52	0.5	21	ns
		to output B	-40°C to 125°C	0.5	155	0.5	86	0.5	52	0.5	21	

Switching Characteristics, $V_{CCA} = 2.5V$

						B-PORT	SUPPLY V	OLTAGE (V _{CCB})			
ı	PARAMETER	TEST CO	NDITIONS	1.5V	± 0.1V	1.8V ±	0.15V	2.5V	± 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	6	0.5	5	0.5	4	0.5	4	
	Propagation	to output B	-40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	no.
t _{pd}	^{pd} delay	From input B	-40°C to 85°C	0.5	6	0.5	5	0.5	4	0.5	4	ns
		to output A	-40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
		From input OE	-40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	
	D: 11 "	to output A	-40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
t _{dis}	Disable time	From input OE	-40°C to 85°C	0.5	31	0.5	28	0.5	25	0.5	23	ns
		to output B	-40°C to 125°C	0.5	34	0.5	31	0.5	28	0.5	25	
		From input OE	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	
	Enable time	to output A	-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	
t _{en}	Enable time	From input OE	-40°C to 85°C	0.5	14	0.5	11	0.5	9	0.5	7	ns
		to output B	-40°C to 125°C	0.5	14	0.5	12	0.5	9	0.5	8	



5.13 Switching Characteristics, $V_{CCA} = 3.3V$

See Figure 6-1 and Figure 6-2 for test circuit and loading conditions. See Figure 6-3 and Figure 6-4 for measurement waveforms.

						B-POR	T SUPPLY V	OLTAGE	(V _{CCB})			
P	ARAMETER	TEST CO	ONDITIONS	0.7V :	t 0.05V	0.8V	± 0.04V	0.9V ±	0.045V	1.2V :	± 0.1V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	81	0.5	40	0.5	22	0.5	7	
	Propagation	to output B	–40°C to 125°C	0.5	81	0.5	40	0.5	22	0.5	7	no
t _{pd}	· uelay	From input B	–40°C to 85°C	0.5	142	0.5	35	0.5	17	0.5	7	ns
		to output A	-40°C to 125°C	0.5	142	0.5	35	0.5	17	0.5	8	
		From input OE	–40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	
	Disable time	to output A	-40°C to 125°C	0.5	24	0.5	24	0.5	24	0.5	24	
t _{dis}	Disable time	From input OE	–40°C to 85°C	0.5	111	0.5	84	0.5	75	0.5	80	ns
		to output B	-40°C to 125°C	0.5	113	0.5	86	0.5	78	0.5	83	
		From input OE	–40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	
t _{en}	Enable time	to output A	-40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	10	
	Enable time	From input OE	-40°C to 85°C	0.5	154	0.5	86	0.5	51	0.5	20	ns
		to output B	-40°C to 125°C	0.5	154	0.5	86	0.5	51	0.5	20	

Switching Characteristics, $V_{CCA} = 3.3V$

						B-POR	SUPPLY	VOLTAGE	(V _{CCB})			
F	PARAMETER	TEST CONDITIONS		1.5V	± 0.1V	1.8V ±	0.15V	2.5V	± 0.2V	3.3V	± 0.3V	UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		From input A	-40°C to 85°C	0.5	5	0.5	4	0.5	4	0.5	4	
	Propagation	to output B	-40°C to 125°C	0.5	5	0.5	4	0.5	4	0.5	4	ns
t _{pd}	delay	From input B	-40°C to 85°C	0.5	5	0.5	5	0.5	4	0.5	4	1115
		to output A	–40°C to 125°C	0.5	6	0.5	5	0.5	4	0.5	4	
		From input \overline{OE} to output A From input \overline{OE} to output B	–40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	- ns
	Disable time		–40°C to 125°C	0.5	24	0.5	24	0.5	24	0.5	24	
t _{dis}	Disable time		–40°C to 85°C	0.5	30	0.5	27	0.5	25	0.5	23	
			–40°C to 125°C	0.5	33	0.5	30	0.5	27	0.5	25	
		From input OE	-40°C to 85°C 0.5 9 0.5 9	9	0.5	9	0.5	9				
	Enable time	to output A	–40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	10	
t _{en}	Enable time	From input OE	-40°C to 85°C	0.5	13	0.5	10	0.5	8	0.5	7	ns
		to output B	-40°C to 125°C	0.5	14	0.5	11	0.5	8	0.5	7	

Product Folder Links: SN74AXC8T245-Q1



5.14 Operating Characteristics: $T_A = 25$ °C

	PARAMETER	TES	ST CONDITIONS	MIN TYP MAX	UNIT		
			V _{CCA} = V _{CCB} = 0.7V	1.2			
			$V_{CCA} = V_{CCB} = 0.8V$	1.8			
			$V_{CCA} = V_{CCB} = 0.9V$	1.8			
^	Power dissipation	C _L = 0, R _L = Open	V _{CCA} = V _{CCB} = 1.2V	1.7			
- pdA	capacitance per transceiver (A to B: outputs enabled)	$f = 1MHz$, $t_r = t_f = 1 \text{ ns}$	V _{CCA} = V _{CCB} = 1.5V	1.7	pF		
	,		V _{CCA} = V _{CCB} = 1.8V	1.7			
			V _{CCA} = V _{CCB} = 2.5V	2			
			$V_{CCA} = V_{CCB} = 3.3V$	2.5			
			V _{CCA} = V _{CCB} = 0.7V	1.1			
			$V_{CCA} = V_{CCB} = 0.8V$	1.8			
			$V_{CCA} = V_{CCB} = 0.9V$	1.8			
_	Power dissipation	$C_L = 0$, $R_L = Open$	V _{CCA} = V _{CCB} = 1.2V	1.7			
− pdA	capacitance per transceiver (A to B: outputs disabled)	$f = 1MHz$, $t_r = t_f = 1 \text{ ns}$	V _{CCA} = V _{CCB} = 1.5V	1.7	pF		
	(V _{CCA} = V _{CCB} = 1.8V	1.7			
			$V_{CCA} = V_{CCB} = 2.5V$	2			
			V _{CCA} = V _{CCB} = 3.3V	2.1			
			V _{CCA} = V _{CCB} = 0.7V	9.3			
			$V_{CCA} = V_{CCB} = 0.8V$	11.8			
			$V_{CCA} = V_{CCB} = 0.9V$	11.8			
,	Power dissipation	$C_L = 0$, $R_L = Open$	V _{CCA} = V _{CCB} = 1.2V	12	1		
PpdA	capacitance per transceiver (B to A: outputs enabled)	$f = 1MHz$, $t_r = t_f = 1 \text{ ns}$	V _{CCA} = V _{CCB} = 1.5V	12.2	pF		
	,		V _{CCA} = V _{CCB} = 1.8V	13			
			V _{CCA} = V _{CCB} = 2.5V	16.4			
			V _{CCA} = V _{CCB} = 3.3V	18.1			
			$V_{CCA} = V_{CCB} = 0.7V$	2.6			
			$V_{CCA} = V_{CCB} = 0.8V$	1.2			
			V _{CCA} = V _{CCB} = 0.9V	1.1			
	Power dissipation	C _L = 0, R _L = Open	V _{CCA} = V _{CCB} = 1.2V	1.2			
pdA	capacitance per transceiver (B to A: outputs disabled)	$f = 1MHz$, $t_r = t_f = 1 \text{ ns}$	V _{CCA} = V _{CCB} = 1.5V	1.2	pF		
	, , , , , , , , , , , , , , , , , , , ,		V _{CCA} = V _{CCB} = 1.8V	1.3	-		
			V _{CCA} = V _{CCB} = 2.5V	1.6			
			V _{CCA} = V _{CCB} = 3.3V	3.9			

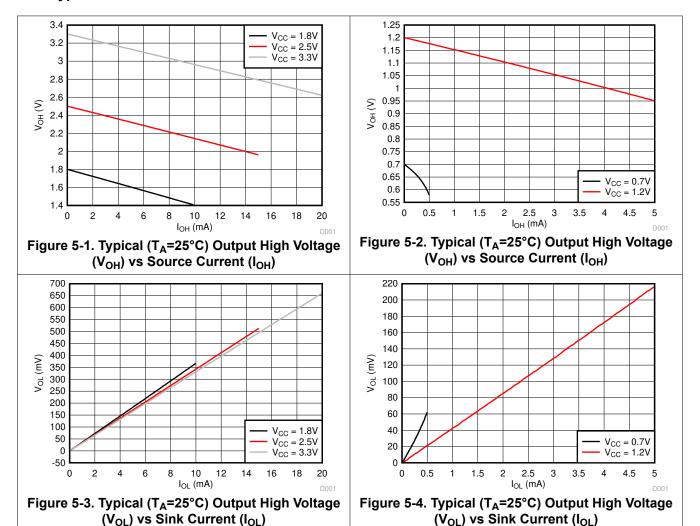


5.14 Operating Characteristics: T_A = 25°C (continued)

	PARAMETER	TES	ST CONDITIONS	MIN TYP	MAX	UNIT		
			V _{CCA} = V _{CCB} = 0.7V	9.3				
			$V_{CCA} = V_{CCB} = 0.8V$	11.7				
			$V_{CCA} = V_{CCB} = 0.9V$	11.8				
	Power dissipation	C _L = 0, R _L = Open	$V_{CCA} = V_{CCB} = 1.2V$	11.9				
C _{pdB}	capacitance per transceiver (A to B: outputs enabled)	$f = 1MHz$, $t_r = t_f = 1 ns$	$V_{CCA} = V_{CCB} = 1.5V$	12.2		pF		
			V _{CCA} = V _{CCB} = 1.8V	12.9				
			$V_{CCA} = V_{CCB} = 2.5V$	16.3				
			$V_{CCA} = V_{CCB} = 3.3V$	18				
			$V_{CCA} = V_{CCB} = 0.7V$	2.6				
			$V_{CCA} = V_{CCB} = 0.8V$	11.7				
			$V_{CCA} = V_{CCB} = 0.9V$	11.8				
	Power dissipation	$C_L = 0$, $R_L = Open$	$V_{CCA} = V_{CCB} = 1.2V$	11.9				
C _{pdB}	capacitance per transceiver (A to B: outputs disabled)	$f = 1MHz$, $t_r = t_f = 1$ ns	$V_{CCA} = V_{CCB} = 1.5V$	12.2		pF		
	,		$V_{CCA} = V_{CCB} = 1.8V$	12.9				
			$V_{CCA} = V_{CCB} = 2.5V$	16.3				
			$V_{CCA} = V_{CCB} = 3.3V$	3.9				
			V _{CCA} = V _{CCB} = 0.7V					
			$V_{CCA} = V_{CCB} = 0.8V$	1.8				
			$V_{CCA} = V_{CCB} = 0.9V$	1.8				
	Power dissipation	$C_L = 0$, $R_L = Open$	$V_{CCA} = V_{CCB} = 1.2V$	1.7				
C _{pdB}	capacitance per transceiver (B to A: outputs enabled)	$f = 1MHz$, $t_r = t_f = 1 ns$	$V_{CCA} = V_{CCB} = 1.5V$	1.7		pF		
	,		$V_{CCA} = V_{CCB} = 1.8V$	1.7				
			$V_{CCA} = V_{CCB} = 2.5V$	2				
			$V_{CCA} = V_{CCB} = 3.3V$	2.5				
			$V_{CCA} = V_{CCB} = 0.7V$	1.1				
			$V_{CCA} = V_{CCB} = 0.8V$	1.8				
			$V_{CCA} = V_{CCB} = 0.9V$	1.8				
	Power dissipation	$C_L = 0$, $R_L = Open$	V _{CCA} = V _{CCB} = 1.2V	1.7				
C _{pdB}	capacitance per transceiver (B to A: outputs disabled)	$f = 1MHz$, $t_r = t_f = 1 \text{ ns}$	V _{CCA} = V _{CCB} = 1.5V	1.7		pF		
	, ,		$V_{CCA} = V_{CCB} = 1.8V$	1.7				
			V _{CCA} = V _{CCB} = 2.5V	2				
			$V_{CCA} = V_{CCB} = 3.3V$	2.1				



5.15 Typical Characteristics

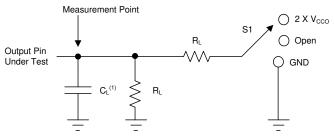




6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f =1MHz
- $Z_0 = 50 \Omega$
- dv / dt ≤ 1 ns/V



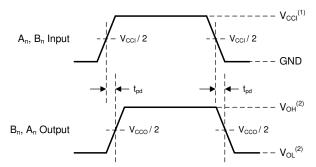
A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

Parameter	V _{cco}	RL	CL	S1	V_{TP}
t _{pd}	1.1 V - 3.6 V	2 kΩ	15 pF	Open	N/A
фи	0.65 V - 0.95 V	20 kΩ	15 pF	Open	N/A
	3 V - 3.6 V	2 kΩ	15 pF	2 X V _{CCO}	0.3 V
. (1) . (1)	1.65 V - 2.7 V	2 kΩ	15 pF	2 X V _{CCO}	0.15 V
t _{en} ⁽¹⁾ , t _{dis} ⁽¹⁾	1.1 V - 1.6 V	2 kΩ	15 pF	2 X V _{CCO}	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	2 X V _{CCO}	0.1 V
	3 V - 3.6 V	2 kΩ	15 pF	GND	0.3 V
t _{en} (2), t _{dis} (2)	1.65V - 2.7 V	2 kΩ	15 pF	GND	0.15 V
ten y tuis	1.1 V - 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	GND	0.1 V

- A. Output waveform on the conditions that input is driven to a valid Logic Low.
- B. Output waveform on the condition that input is driven to a valid Logic High.

Figure 6-2. Load Circuit Conditions

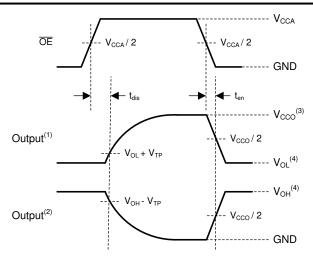


- A. V_{CCI} is the supply pin associated with the input port.
- B. V_{OH} and V_{OL} are typical output voltage levels with specified R_L , C_L , and S_1 .

Figure 6-3. Propagation Delay

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- A. Output waveform on the condition that input is driven to a valid Logic Low.
- B. Output waveform on the condition that input is driven to a valid Logic High.
- C. V_{CCO} is the supply pin associated with the output port.
- D. $\;\;$ V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S₁.

Figure 6-4. Enable Time And Disable Time

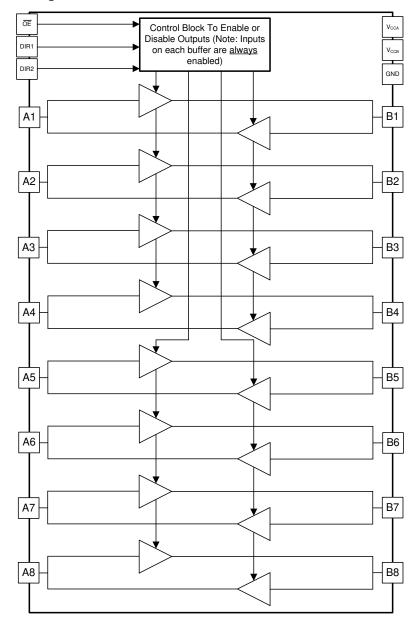


7 Detailed Description

7.1 Overview

The SN74AXC8T245-Q1 device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and $\overline{\text{OE}}$) are supported by V_{CCA}, and the I/O pins labeled with B are supported by V_{CCB}. The A port and the B port are able to accept I/O voltages ranging from 0.65V to 3.6V.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Up-Translation and Down-Translation From 0.65V to 3.6V

Both supply pins are configured from 0.65V to 3.6V, which makes the device suitable for translating between any of the low voltage nodes (0.7V, 0.8V, 0.9V, 1.2V, 1.8V, 2.5V, and 3.3V).

7.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both $V_{\rm CCA}$ and $V_{\rm CCB}$ are at least 1.40V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6V while having its corresponding power supply rail powered down. This is represented by the I_{off} parameter in the *Electrical Characteristics* table.

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7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

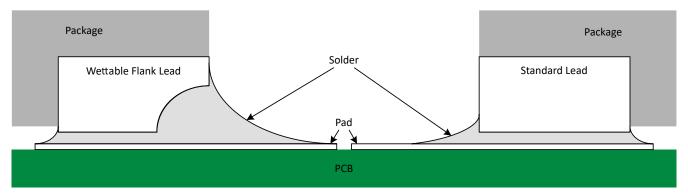


Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.5 I/Os with Integrated Static Pull-Down Resistors

To help avoid floating inputs on the I/Os, this device has $288k\Omega$ typical integrated weak pull-downs on all data I/Os. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than $30k\Omega$ to avoid contention with the $288k\Omega$ internal pull-down.

7.4 Device Functional Modes

All control inputs are referenced to V_{CCA} and must be driven to a valid Logic High or Logic Low (that is, not floating) to assure proper device operation and to prevent excessive power consumption. Table 7-1 summarizes the possible modes of device operation based on the configuration of the control inputs.

	CONTROL INPUTS)	Signal Direction					
ŌĒ	DIR1	DIR2	Bits 1:4 Bits 5:8					
Н	X	X	Disabled (Hi-Z)					
L	L	L	B to A					
L	L	Н	B to A	A to B				
L	Н	L	A to B					
L	Н	Н	A to B B to A					

Table 7-1. Function Table

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AXC8T245-Q1 AEC-Q100 qualified SN74AXC8T245-Q1-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. Figure 9-1 depicts an application in which the SN74AXC8T245-Q1 device is up-translating a 0.7V input to a 3.3V output to interface between a system controller and a peripheral device.

8.2 Typical Application

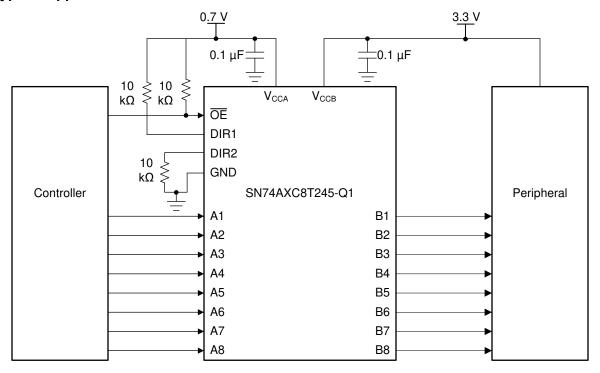


Figure 8-1. Typical Application Schematic



8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

·	<u> </u>
DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65V to 3.6V
Output voltage range	0.65V to 3.6V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- · Input voltage range
 - Use the supply voltage of the device that is driving the SN74AXC8T245-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- · Output voltage range
 - Use the supply voltage of the device that the SN74AXC8T245-Q1 device is driving to determine the output voltage range.

8.2.3 Application Curve

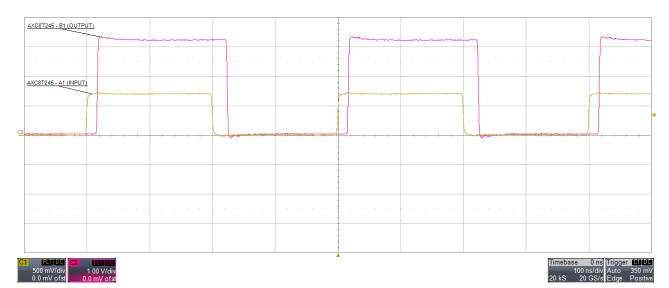


Figure 8-2. Translation Up (0.7V to 3.3V) at 2.5MHz

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8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. There are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, follow common printed-circuit board layout guidelines.

- · Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

8.4.2 Layout Example

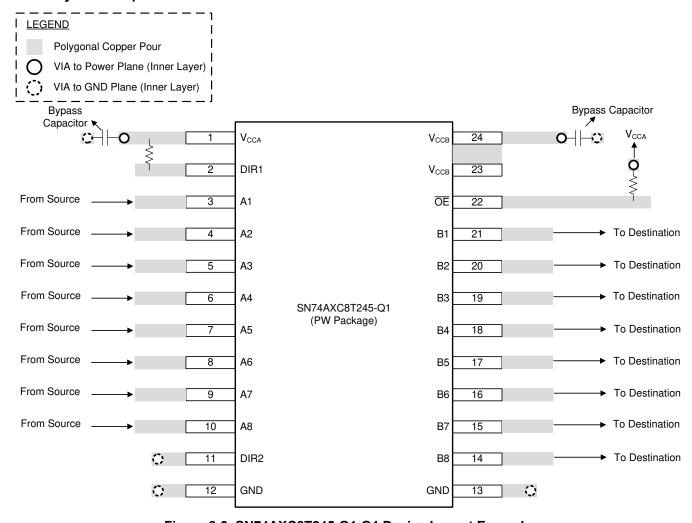


Figure 8-3. SN74AXC8T245-Q1-Q1 Device Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, SN74AXC8245-Q1 Evaluation Module user's guide
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application report
- · Texas Instruments, Power Sequencing for AXC Family of Devices application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2021) to Revision D (January 2024)	Page
Added the I _{off} Supports Partial-Power-Down Mode Operation section	21
Changes from Revision B (May 2021) to Revision C (October 2021)	Page
Reformatted the Device Information table	
Added wettable flank information in <i>Features</i>	1
Added wettable flank information in Feature Description	21
Changes from Revision A (July 2019) to Revision B (May 2021)	Page

Product Folder Links: SN74AXC8T245-Q1



5
Page
1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
CAXC8T245QRHLRQ1	Active	Production	VQFN (RHL) 24	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245Q
CAXC8T245QRHLRQ1.B	Active	Production	VQFN (RHL) 24	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245Q
CAXC8T245QWRGYRQ1	Active	Production	VQFN (RGY) 24	3000 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AX8T245Q
CAXC8T245QWRGYRQ1.B	Active	Production	VQFN (RGY) 24	3000 LARGE T&R	Yes	FULL NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AX8T245Q
			7.1						
SN74AXC8T245QPWRQ1	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245Q
SN74AXC8T245QPWRQ1.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN74AXC8T245-Q1:

● Catalog : SN74AXC8T245

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAXC8T245QRHLRQ1	VQFN	RHL	24	1000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
CAXC8T245QWRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAXC8T245QRHLRQ1	VQFN	RHL	24	1000	367.0	367.0	35.0
CAXC8T245QWRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



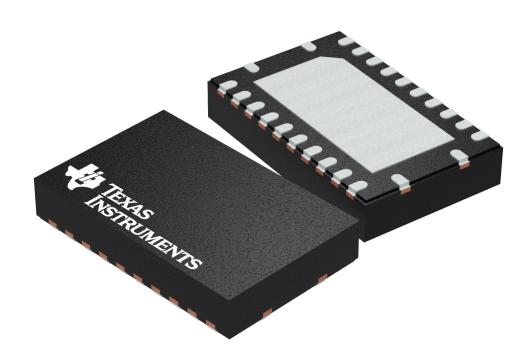
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



5.5 x 3.5 mm, 0.5 mm pitch

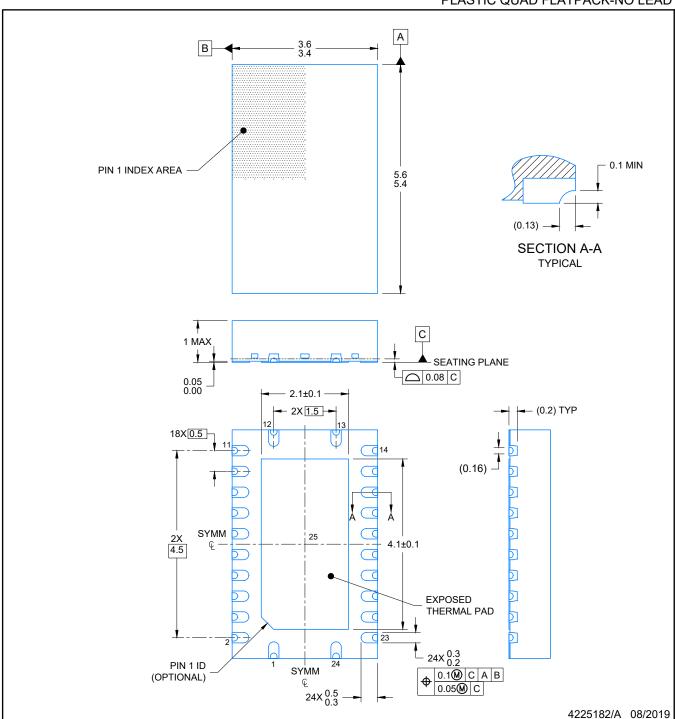
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



PLASTIC QUAD FLATPACK-NO LEAD

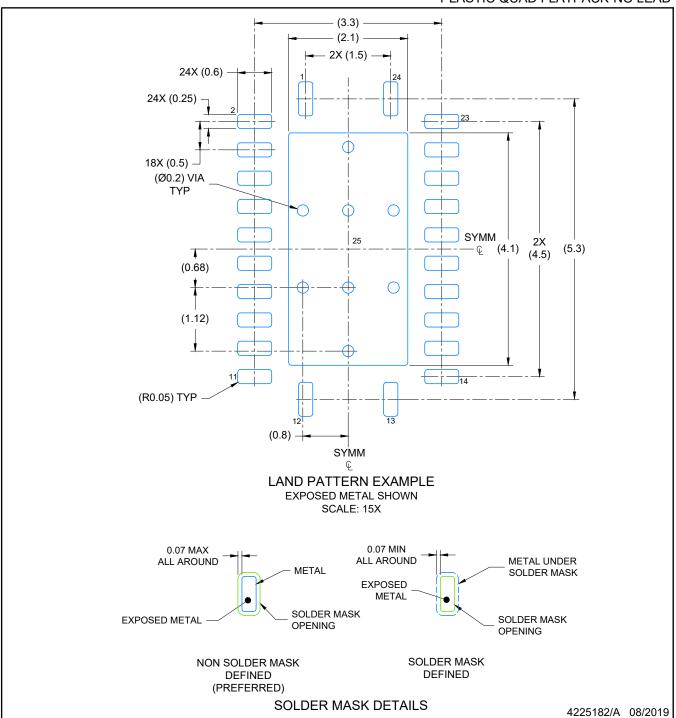


NOTES:

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- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLATPACK-NO LEAD

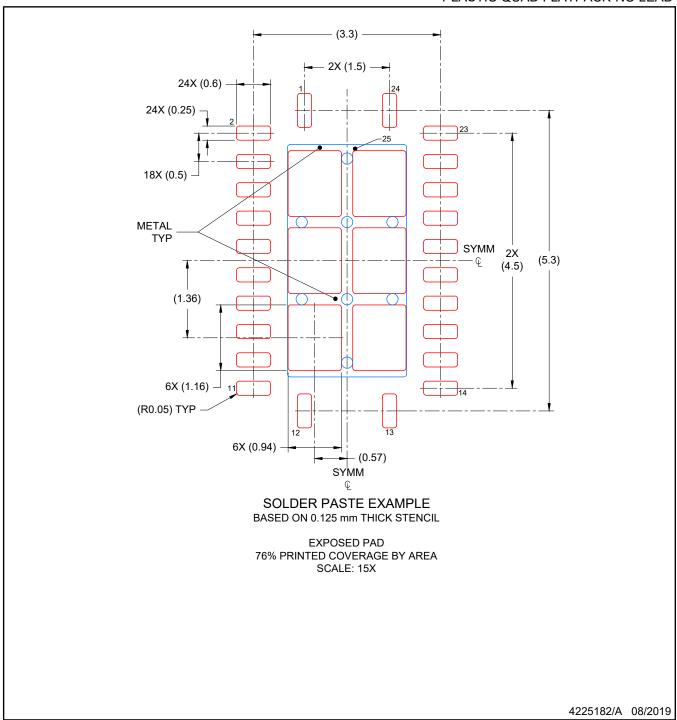


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK-NO LEAD

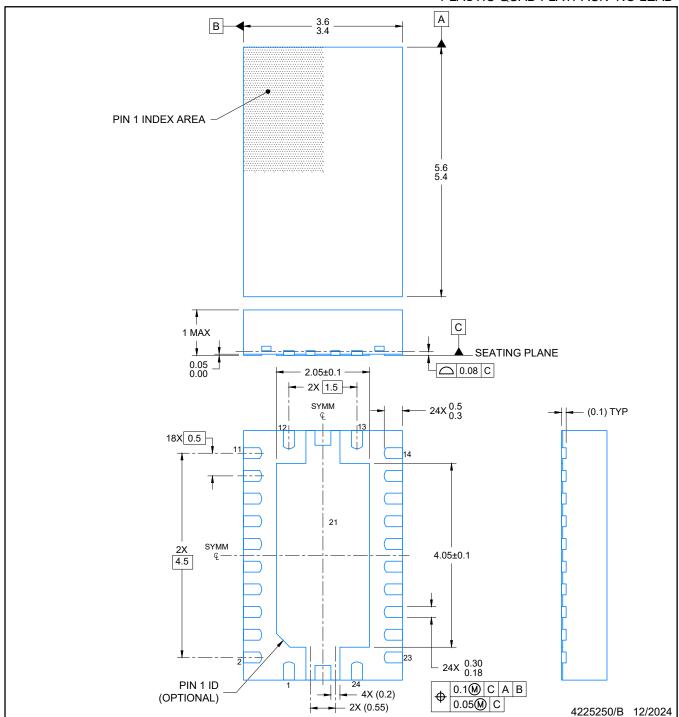


NOTES: (continued)

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PLASTIC QUAD FLATPACK- NO LEAD

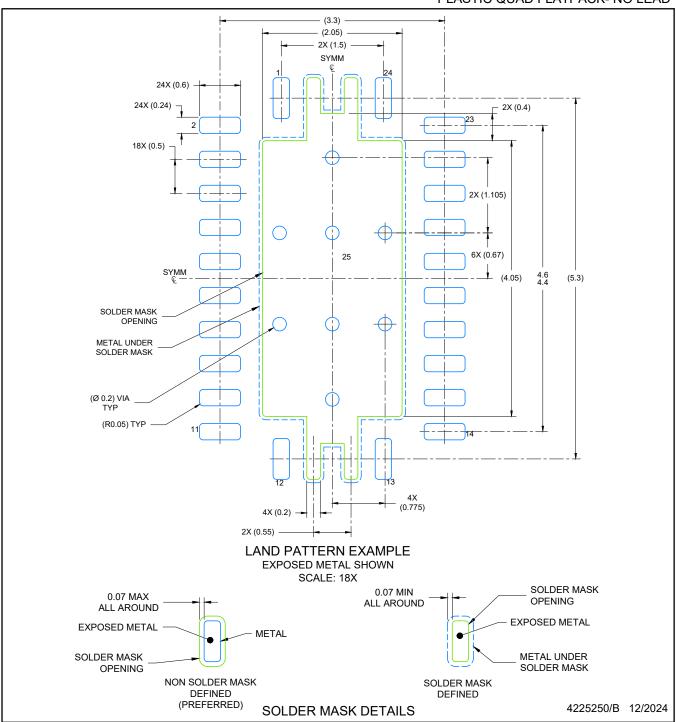


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLATPACK- NO LEAD

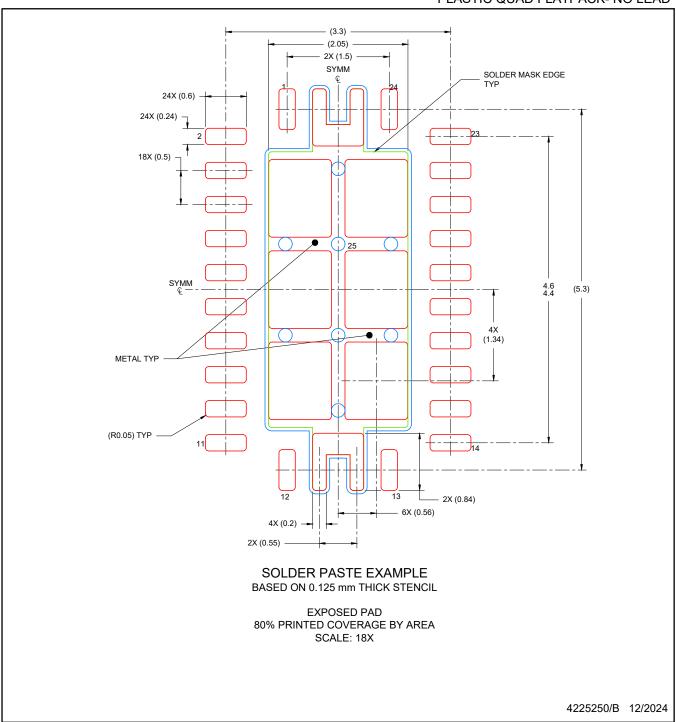


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

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