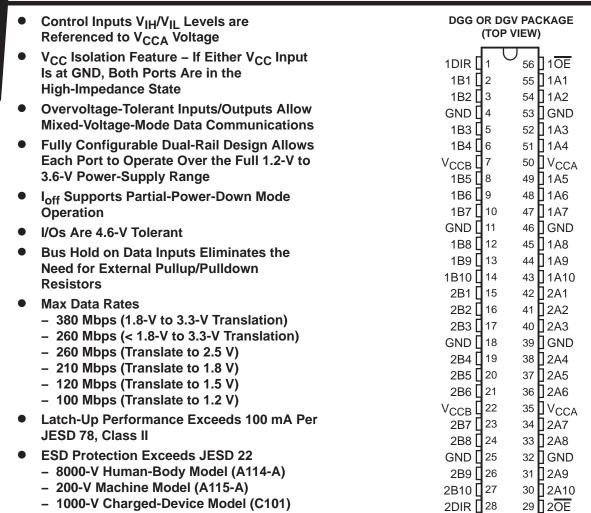
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description/ordering information

This 20-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVCH20T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

ORDERING INFORMATION

TA	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	TSSOP - DGG	Tape and reel	SN74AVCH20T245GR	AVCH20T245
-40°C to 85°C	TVSOP - DGV	Tape and reel	SN74AVCH20T245VR	WK245
-40°C 10 65°C	VFBGA – GQL	Tape and reel	SN74AVCH20T245KR	WK245
	VFBGA – ZQL (Pb-free)	rape and reer	74AVCH20T245ZQLR	VVNZ45

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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description/ordering information (continued)

The SN74AVCH20T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so that the buses are effectively isolated.

The SN74AVCH20T245 is designed so that the control (1DIR, 2DIR, 1OE, and 2OE) inputs are supplied by VCCA.

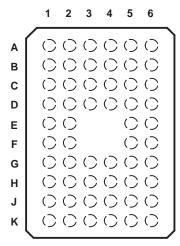
This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
Α	1B1	1B2	1DIR	1OE	1A2	1A1
В	1B3	1B4	GND	GND	1A4	1A3
С	1B5	1B6	VCCB	VCCA	1A6	1A5
D	1B7	1B8	GND	GND	1A8	1A7
Ε	1B9	1B10			1A10	1A9
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
Н	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2B9	2B10	2DIR	2OE	2A10	2A9

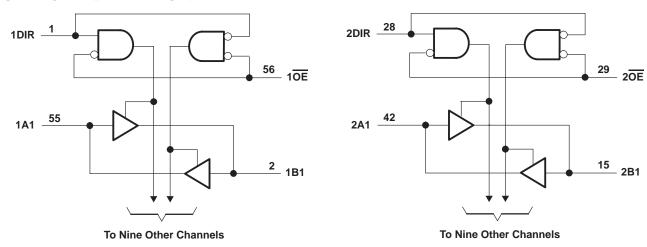
FUNCTION TABLE (each 10-bit section)

INP	UTS	
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation



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logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V _I (see Note 1): I/O ports (A po	-0.5 V to 4.6 V ort) -0.5 V to 4.6 V ort) -0.5 V to 4.6 V
·	6
Voltage range applied to any output in the high-imp	
(B port)	
Voltage range applied to any output in the high or lo	ow state, V _O
(see Notes 1 and 2): (A port)	0.5 V to V _{CCA} + 0.5 V
	0.5 V to V _{CCB} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
	–50 mA
	±50 mA
	d GND ±100 mA
Package thermal impedance, θ _{.IA} (see Note 3): DG	GG package 64°C/W
	GV package 48°C/W
	QL/ZQL package 42°C/W
	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 8)

			VCCI	Vcco	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
Vссв	Supply voltage				1.2	3.6	V
			1.2 V to 1.95 V		V _{CCI} ×0.65		
V_{IH}	High-level input voltage	Data inputs (see Note 7)	1.95 V to 2.7 V		1.6		V
	voltage	(See Note 1)	2.7 V to 3.6 V		2		
			1.2 V to 1.95 V			V _{CCI} × 0.35	
\vee_{IL}	Low-level input voltage	Data inputs (see Note 7)	1.95 V to 2.7 V			0.7	V
	vollago	(300 14010 1)	2.7 V to 3.6 V			0.8	
		DIR	1.2 V to 1.95 V		V _{CCA} ×0.65		
VIH	High-level input voltage	(referenced to V _{CCA})	1.95 V to 2.7 V		1.6		V
	voltage	(see Note 8)	2.7 V to 3.6 V		2		
		DIR	1.2 V to 1.95 V			V _{CCA} ×0.35	
V_{IL}	Low-level input voltage	(referenced to V _{CCA})	1.95 V to 2.7 V			0.7	V
	voltage	(see Note 8)	2.7 V to 3.6 V			0.8	
VI	Input voltage				0	3.6	V
\/ -	Output valtage	Active state			0	Vcco	V
VO	Output voltage	3-state			0	3.6	V
				1.2 V		-3	
				1.4 V to 1.6 V		-6	
lOH	High-level output curr	ent		1.65 V to 1.95 V		-8	mA
				2.3 V to 2.7 V		-9	
				3 V to 3.6 V		-12	
				1.2 V		3	
				1.4 V to 1.6 V		6	
loL	Low-level output curre	ent		1.65 V to 1.95 V		8	mA
lOL				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δν	Input transition rise or	fall rate				5	ns/V
TA	Operating free-air tem	nperature			-40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.

- 5. V_{CCO} is the V_{CC} associated with the output port.
- 6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
- 7. For V_{CCI} values not specified in the data sheet, V_{IH(min)} = V_{CCI} x 0.7 V, V_{IL(max)} = V_{CCI} x 0.3 V.

 8. For V_{CCI} values not specified in the data sheet, V_{IH(min)} = V_{CCA} x 0.7 V, V_{IL(max)} = V_{CCA} x 0.3 V.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 9)

				.,	T,	Δ = 25°C	;	–40°C to	LINUT		
PARAMETER	TEST COND	ITIONS	VCCA	VCCB	MIN	TYP	MAX	MIN	MAX	UNIT	
	I _{OH} = -100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V				Vcco-	0.2 V		
	IOH = -3 mA		1.2 V	1.2 V		0.95					
V	$I_{OH} = -6 \text{ mA}$,, ,,	1.4 V	1.4 V				1.05			
VOH	I _{OH} = -8 mA	VI = VIH	1.65 V	1.65 V				1.2		V	
	$I_{OH} = -9 \text{ mA}$		2.3 V	2.3 V				1.75			
1	I _{OH} = -12 mA		3 V	3 V				2.3			
	I _{OL} = 100 μA		1.2 V to 3.6 V	1.2 V to 3.6 V					0.2		
	I _{OL} = 3 mA		1.2 V	1.2 V		0.15					
V	I _{OL} = 6 mA	,, ,,	1.4 V	1.4 V					0.35		
VOL	I _{OL} = 8 mA	$V_I = V_{IL}$	1.65 V	1.65 V					0.45	V	
	I _{OL} = 9 mA		2.3 V	2.3 V					0.55		
	I _{OL} = 12 mA		3 V	3 V					0.7		
I _I Control inputs	V _I = V _{CCA} or GI	ND	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μΑ	
I _{BHL} †	V _I = 0.42 V		1.2 V	1.2 V		25					
	V _I = 0.49 V		1.4 V	1.4 V				15			
	V _I = 0.58 V		1.65 V	1.65 V				25		μΑ	
	V _I = 0.7 V		2.3 V	2.3 V				45		•	
	V _I = 0.8 V		3.3 V	3.3 V				100			
	V _I = 0.78 V		1.2 V	1.2 V		-25					
	V _I = 0.91 V		1.4 V	1.4 V				-15			
I _{BHH} ‡	V _I = 1.07 V		1.65 V	1.65 V				-25		μΑ	
	V _I = 1.6 V		2.3 V	2.3 V				-45			
1	V _I = 2 V		3.3 V	3.3 V				-100			
			1.2 V	1.2 V		50					
			1.6 V	1.6 V				125			
I _{BHLO} §	$V_I = 0$ to V_{CC}		1.95 V	1.95 V				200		μΑ	
			2.7 V	2.7 V				300			
			3.6 V	3.6 V				500			
			1.2 V	1.2 V		-50					
			1.6 V	1.6 V				-125			
I _{BHHO} ¶	$V_{I} = 0$ to V_{CC}		1.95 V	1.95 V				-200		μА	
-		2.7 V	2.7 V				-300				
			3.6 V	3.6 V				-500			

[†] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

NOTE 9: VCCO is the VCC associated with the output port.



[‡] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[§] An external driver must source at least I_{BHLO} to switch this node from low to high.

[¶] An external driver must sink at least IBHHO to switch this node from high to low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 10 and 11) (continued)

				.,	.,	T,	\ = 25°C	;	-40°C to	o 85°C	
PARA	AMETER	TEST CONDIT	IONS	VCCA	VCCB	MIN	TYP	MAX	MIN	MAX	UNIT
1	A port	\/. 0 x \/ 0 \ 0 to 2 6 \/		0 V	0 to 3.6 V		±0.1	±1		±5	
l _{off}	B port	$V_I \text{ or } V_O = 0 \text{ to } 3.6 \text{ V}$		0 to 3.6 V	0 V		±0.1	±1		±5	μΑ
	A or B ports	$V_O = V_{CCO}$ or	= VCCO or \overline{OE} = V _{IH}		3.6 V		±0.5	±2.5		±5	
loz†	B port	GND, V _I = V _{CCI} or GND	OE =	0 V	3.6 V					±5	μΑ
	A port	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	don't care	3.6 V	0 V					±5	
				1.2 V to 3.6 V	1.2 V to 3.6 V					35	
ICCA		$V_I = V_{CCI}$ or GND,	$I_O = 0$	0 V	3.6 V					-5	μΑ
				3.6 V	0 V					35	
				1.2 V to 3.6 V	1.2 V to 3.6 V					35	
ICCB		$V_I = V_{CCI}$ or GND,	$I_{O} = 0$	0 V	3.6 V					35	μΑ
				3.6 V	0 V					-5	
ICCA	+ ICCB	$V_I = V_{CCI}$ or GND,	IO = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					65	μΑ
C _i	Control inputs	$V_I = 3.3 \text{ V or GND}$ 3.		3.3 V	3.3 V		3.5				pF
C _{io}	A or B ports	V _O = 3.3 V or GND		3.3 V	3.3 V		7				pF

[†] For I/O ports, the parameter IOZ includes the input leakage current.

NOTES: 10. V_{CCO} is the V_{CC} associated with the output port.

switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 1.2 \text{ V}$ (see Figure 1)

DADAMETED	FROM	то	V _{CCB} = 1.2 V	V _{CCB} = 1.5 V	V _{CCB} = 1.8 V	V _{CCB} = 2.5 V	V _{CCB} = 3.3 V	LINUT
PARAMETER	(INPUT)	(OUTPUT)	TYP	TYP	TYP	TYP	TYP	UNIT
^t PLH			3.8	3.1	2.8	2.7	3.3	
^t PHL	Α	В	3.8	3.1	2.8	2.7	3.3	ns
^t PLH	6	Δ.	4.1	3.8	3.6	3.5	3.4	
^t PHL	В	Α	4.1	3.8	3.6	3.5	3.4	ns
^t PZH	ŌĒ	Δ.	6.5	6.5	6.5	6.5	6.5	
tPZL	OE	Α	6.5	6.5	6.5	6.5	6.5	ns
^t PZH	ŌĒ		5.6	4.4	3.8	3.3	3.2	
t _{PZL}	OE	В	5.6	4.4	3.8	3.3	3.2	ns
^t PHZ	ŌĒ		6.4	6.4	6.4	6.4	6.4	
tPLZ	OE	Α	6.4	6.4	6.4	6.4	6.4	ns
^t PHZ	ŌĒ	В	5.7	4.6	4.7	4.1	5.4	
t _{PLZ}	OE	R	5.7	4.6	4.7	4.1	5.4	ns

^{11.} V_{CCI} is the V_{CC} associated with the input port.

SN74AVCH20T245 **20-BIT DUAL-SUPPLY BUS TRANSCEIVER** WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS SCES567F - MAY 2004 - REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 1.5 V \pm 0.1 V$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO	V _{CCB} = 1.2 V	V _{CCB} =		V _{CCB} = ± 0.1		V _{CCB} =		V _{CCB} =		UNIT																			
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX																				
tPLH	Α	В	3.8	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9																				
^t PHL	А	Ь	3.8	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	ns																			
tPLH	В	Δ.	3.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7																				
^t PHL	В	А	3.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	ns																			
^t PZH	ŌĒ	Δ.	4.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2																				
tPZL	OE	А	4.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	ns																			
^t PZH	ŌE		5.2	1	10.3	1	8.4	0.5	6.1	0.5	5.3																				
tPZL	OE	В	5.2	1	10.3	1	8.4	0.5	6.1	0.5	5.3	ns																			
^t PHZ	<u></u>	Δ.	4.5	2	9	2	9	2	9	2	9																				
tpLZ	OĒ	ŌE A	4.5	2	9	2	9	2	9	2	9	ns																			
^t PHZ	<u> </u>		5.1	1.5	9	1.5	7.8	1	6.4	1	5.9																				
tPLZ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	OE	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	В	5.1	1.5	9	1.5	7.8	1	6.4	1	5.9	ns

switching characteristics over recommended operating free-air temperature range, $V_{CCA} = 1.8 V \pm 0.15 V$ (see Figure 1)

PARAMETER	FROM	TO	V _{CCB} = 1.2 V	V _{CCB} =		V _{CCB} = ± 0.1		V _{CCB} =		VCCB =		UNIT												
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX													
tPLH	Α	В	3.6	0.5	6.1	0.5	5	0.5	3.9	0.5	3.5	20												
tPHL	А	В	3.6	0.5	6.1	0.5	5	0.5	3.9	0.5	3.5	ns												
tPLH	В	^	2.8	0.5	5.4	0.5	5	0.5	4.7	0.5	4.6													
^t PHL	В	Α	2.8	0.5	5.4	0.5	5	0.5	4.7	0.5	4.6	ns												
^t PZH	ŌĒ		3.4	1	8.1	1	7.9	1	7.9	1	7.9													
tPZL	OE	А	3.4	1	8.1	1	7.9	1	7.9	1	7.9	ns												
^t PZH	ŌĒ	В	5	0.5	10	0.5	7.9	0.5	5.7	0.5	4.8													
tPZL	OE	В	5	0.5	10	0.5	7.9	0.5	5.7	0.5	4.8	ns												
t _{PHZ}	<u></u>	^	4.1	2	7.4	2	7.4	2	7.4	2	7.4													
tPLZ	ŌĒ	Α	A	4.1	2	7.4	2	7.4	2	7.4	2	7.4	ns											
t _{PHZ}	<u> </u>		4.9	1.5	8.7	1.5	7.4	1	5.8	1	5.1													
tPLZ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	В	4.9	1.5	8.7	1.5	7.4	1	5.8	1	5.1	ns

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switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V \pm 0.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO	V _{CCB} = 1.2 V	V _{CCB} =		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT												
	(INPUI)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX													
tPLH	Δ.	В	3.5	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3													
t _{PHL}	Α	В	3.5	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3	ns												
t _{PLH}	В	А	2.7	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	20												
tPHL	Ь	A	2.7	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	ns												
^t PZH	ŌĒ		2.5	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2													
t _{PZL}	OE	OE A	2.5	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	ns												
^t PZH	ŌĒ	В	4.8	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3													
tPZL	OE	В	4.8	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	ns												
^t PHZ	<u> </u>	Δ.	3	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2													
tPLZ	ŌĒ	Α	3	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	ns												
^t PHZ	<u> </u>		4.7	1.2	8.2	1.2	6.9	1	5.3	1	5													
tPLZ	ŌĒ	ŌĒ	ŌĒ	OE	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	В	4.7	1.2	8.2	1.2	6.9	1	5.3	1	5	ns

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V \pm 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO	V _{CCB} = 1.2 V	V _{CCB} = ± 0.7		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT															
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX																
tPLH	٨	В	3.4	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9																
tPHL	Α	В	3.4	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	ns															
tPLH	В	Δ.	3.3	0.5	3.9	0.5	3.5	0.5	3	0.5	2.9																
t _{PHL}	В	А	3.3	0.5	3.9	0.5	3.5	0.5	3	0.5	2.9	ns															
^t PZH	ŌĒ		2.2	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1																
tPZL	OE	Α	2.2	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	ns															
t _{PZH}	ŌĒ	В	4.7	1	9.6	0.5	7.5	0.5	5.1	0.5	4.1																
tPZL	OE	В	4.7	1	9.6	0.5	7.5	0.5	5.1	0.5	4.1	ns															
tPHZ	ŌĒ	Δ.	3.4	0.8	5	0.8	5	0.8	5	0.8	5																
tPLZ	OE	А	3.4	0.8	5	0.8	5	0.8	5	0.8	5	ns															
t _{PHZ}	<u> </u>	В	4.6	1.2	8.1	1.2	6.7	1	5.1	0.8	5																
tPLZ	ŌĒ	ŌĒ	ŌĒ	OE	ŌĒ	ŌĒ	ŌĒ	OE	OE	ŌĒ	OE	ŌĒ	ŌĒ	ŌĒ	ŌĒ	ŌĒ	R	4.6	1.2	8.1	1.2	6.7	1	5.1	0.8	5	ns

SN74AVCH20T245 20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS SCES567F - MAY 2004 - REVISED APRIL 2005

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS	V _{CCA} = V _{CCA} = V _{CCB} = 1.5 V		V _{CCA} = V _{CCB} = 1.8 V	V _{CCA} = V _{CCB} = 2.5 V	V _{CCA} = V _{CCB} = 3.3 V	UNIT	
			CONDITIONS	TYP	TYP	TYP	TYP	TYP	1	
	A to B	Outputs Enabled		1	1	1	1	2		
c _{pdA} †	Alob	Outputs Disabled	$C_L = 0,$ f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	1	1	1	1	1		
CpdA	B to A	Outputs Enabled		12	13	14	15	16	pF	
		Outputs Disabled		1	1	1	1	1		
	A to B	Outputs Enabled		13	13	14	15	16		
c _{pdB} †	AIOB	Outputs Disabled	C _L = 0,	1	1	1	1	1	pF	
⊃pdB¹	D	Outputs Enabled	f = 10 MHz, $t_{\Gamma} = t_{f} = 1 \text{ ns}$	1	1	1	2	2	þΓ	
	B to A	Outputs Disabled		1	1	1	1	1		

[†] Power-dissipation capacitance per transceiver

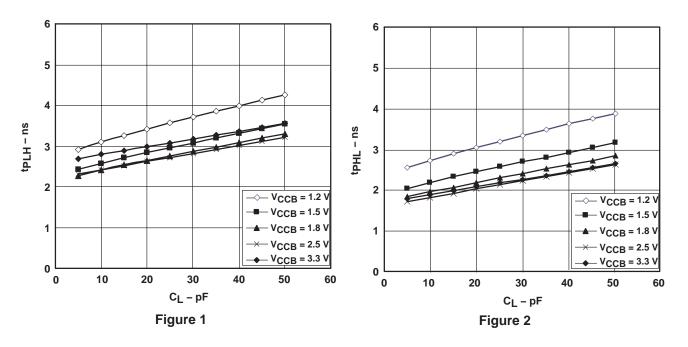
typical total static power consumption ($I_{CCA} + I_{CCB}$)

TABLE 1

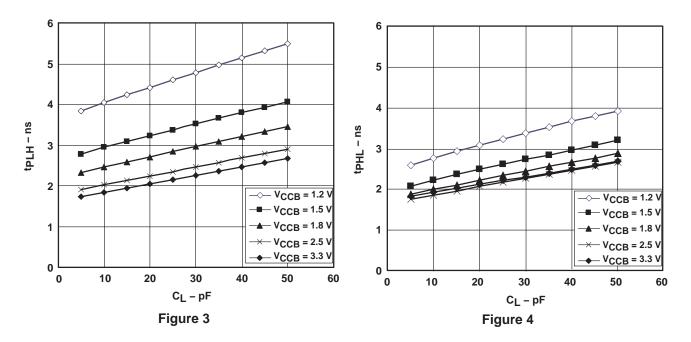
.,	VCCA										
VCCB	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	UNIT				
0 V	0	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5					
1.2 V	< 0.5	< 1	< 1	< 1	< 1	1					
1.5 V	< 0.5	< 1	< 1	< 1	< 1	1	_				
1.8 V	< 0.5	< 1	< 1	< 1	< 1	< 1	μΑ				
2.5 V	< 0.5	1	< 1	< 1	< 1	< 1					
3.3 V	< 0.5	1	< 1	< 1	< 1	< 1					

TYPICAL CHARACTERISTICS

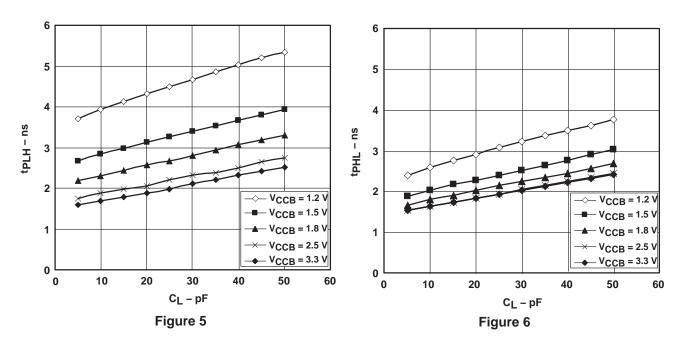
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_A = 25^{\circ}\text{C}$, $V_{CCA} = 1.2 \text{ V}$



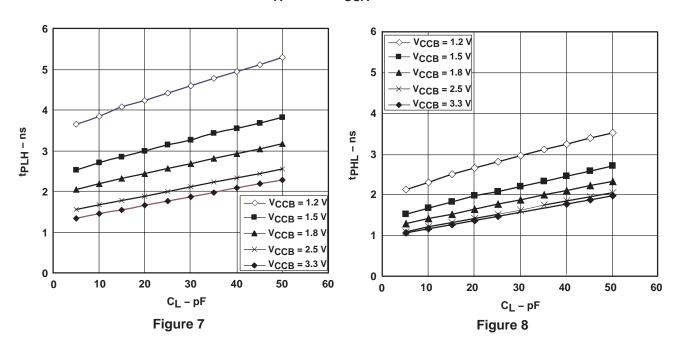
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_A = 25^{\circ}C$, $V_{CCA} = 1.5 \text{ V}$



TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_A = 25^{\circ}C, V_{CCA} = 1.8 V$

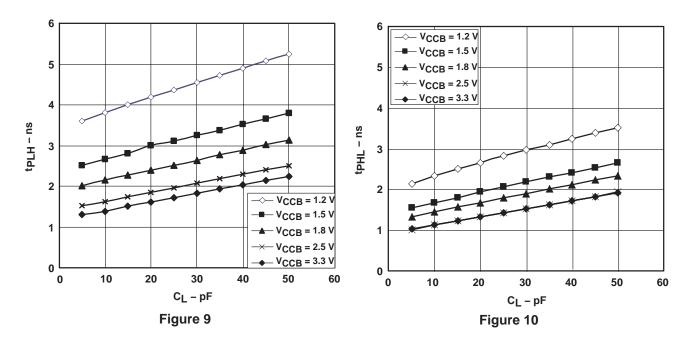


TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_{A}=25^{\circ}\text{C},\,V_{CCA}=2.5\,\text{V}$



SCES567F - MAY 2004 - REVISED APRIL 2005

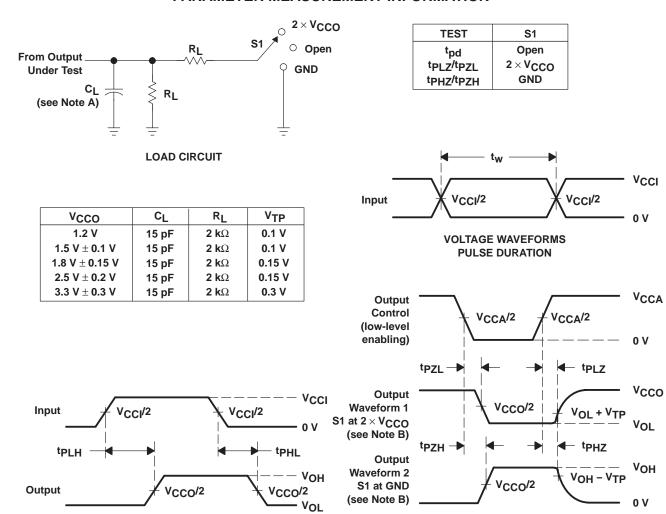
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE $T_A = 25^{\circ}C$, $V_{CCA} = 3.3 \text{ V}$



VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $dv/dt \geq 1 V/ns$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. VCCO is the VCC associated with the output port.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

Figure 11. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AVCH20T245GR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH20T245
SN74AVCH20T245GR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH20T245
SN74AVCH20T245VR	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WK245
SN74AVCH20T245VR.B	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WK245
SN74AVCH20T245VRG4	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WK245
SN74AVCH20T245VRG4.B	Active	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WK245

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH20T245GR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74AVCH20T245VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74AVCH20T245VRG4	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH20T245GR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74AVCH20T245VR	TVSOP	DGV	56	2000	356.0	356.0	45.0
SN74AVCH20T245VRG4	TVSOP	DGV	56	2000	356.0	356.0	45.0

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





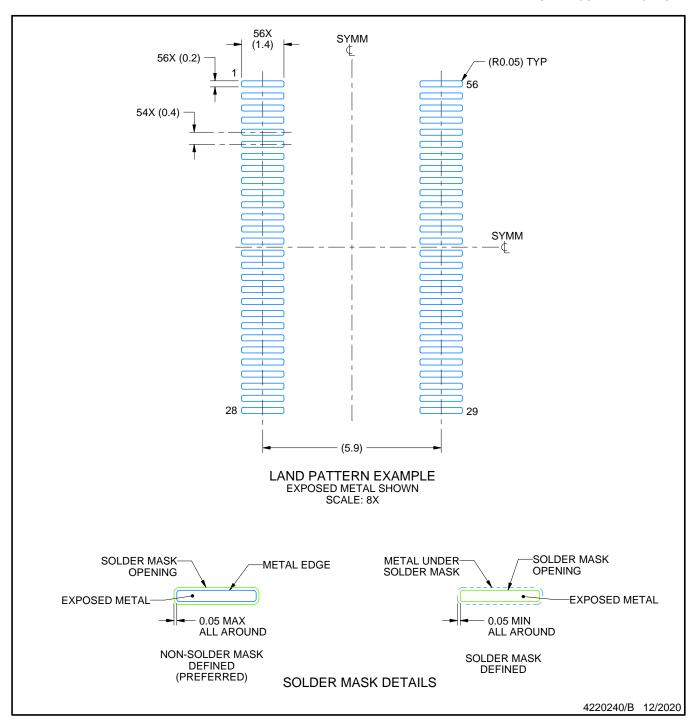
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-194.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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