SN74AVCH1T45 Single-Bit Dual-Supply Bus Transceiver With Configurable Level-Shifting, Voltage Translation, and 3-State Outputs

1 Features

- Available in Texas Instruments' NanoStar™ integrated circuit package
- Available in Texas Instruments' NanoFree™ package
- Control inputs (DIR) V_{IH} and V_{IL} levels are referenced to V_{CCA} voltage
- Bus hold on data inputs eliminates the need for external pullup and pulldown resistors
- V_{CC} isolation
- Fully configurable dual-rail design
- I/Os are 4.6V tolerant
- I_{off} supports partial-power-down mode operation
- Typical max data rates
  - 500Mbps (1.8V to 3.3V translation)
  - 320Mbps (<1.8V to 3.3V translation)
  - 320Mbps (translate to 2.5V or 1.8V)
  - 280Mbps (translate to 1.5V)
  - 240Mbps (translate to 1.2V)
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - Human-Body Model (A114-A): 2000V
  - Machine Model (A115-A): 200V
  - Charged-Device Model (C101): 1000V

2 Applications

- Personal electronics
- Industrial
- Enterprise
- Telecommunications

3 Description

The SN74AVCH1T45 is a single-bit noninverting bus transceiver that uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}, which accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}, which accepts any supply voltage from 1.2V to 3.6V. This feature allows for universal low-voltage, bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

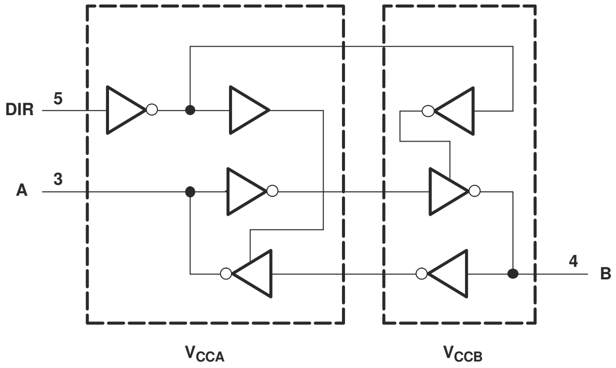
The SN74AVCH1T45 is designed for asynchronous communication between two data buses. The device transmits data from either the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input.

The SN74AVCH1T45 is designed so that the DIR input is referenced to V_{CCA}.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74AVCH1T45	DCK (SC70, 6)	2.00mm × 1.25mm
	DBV (SOT-23, 6)	2.90mm × 1.60mm
	YZP (DSBGA, 6)	1.50mm × 0.90mm

(1) For all available packages, see Section 14.



Logic Diagram (Positive Logic)

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Table of Contents

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4 Description (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. TI does not recommend the use of pullup or pulldown resistors with bus-hold circuitry.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device.

The V_{CC} isolation feature places the outputs in the high-impedance state if either V_{CCA} or V_{CCB} is at GND. The bus-hold circuitry on the powered-up side always stays active.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

5 Pin Configuration and Functions

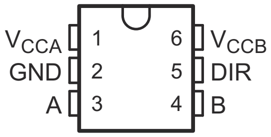

Figure 5-1. DBV or DCK Package 6-Pin SOT-23 or SC70 Top View

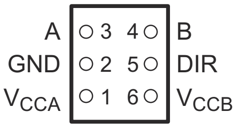

Figure 5-2. YZP Package 6-Pin DSBGA Bottom View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	3	I/O	Input/output A. Referenced to V_{CCA}
B	4	I/O	Input/output B. Referenced to V_{CCB}
DIR	5	I	Direction control signal. Referenced to V_{CCA}
GND	2	—	Ground
V_{CCA}	1	—	A-port supply voltage. $1.2\ V \leq V_{CCA} \leq 3.6\ V$
V_{CCB}	6	—	B-port supply voltage. $1.2\ V \leq V_{CCB} \leq 3.6\ V$

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CCA} and V_{CCB}	–0.5	4.6	V
Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
	I/O ports (B port)	–0.5	4.6	
	Control inputs	–0.5	4.6	
Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
	B port	–0.5	4.6	
Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	
Input clamp current	V_I < 0		–50	mA
Output clamp current	V_O < 0		–50	mA
Continuous output current			±50	mA
Continuous through current	V_{CCA}, V_{CCB}, or GND		±100	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model, per A115-A	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (1) (2) (3) (4) (5)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.2	3.6	V
V_{CCB}	Supply voltage			1.2	3.6	V
V_{IH}	High-level input voltage(1)	Data inputs(4)	V_{CCI} = 1.2 V to 1.95 V	V_{CCI} × 0.65		V
			V_{CCI} = 1.95 V to 2.7 V	1.6		
			V_{CCI} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage(1)	Data inputs(4)	V_{CCI} = 1.2 V to 1.95 V		V_{CCI} × 0.35	V
			V_{CCI} = 1.95 V to 2.7 V		0.7	
			V_{CCI} = 2.7 V to 3.6 V		0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	V_{CCI} = 1.2 V to 1.95 V	V_{CCA} × 0.65		V
			V_{CCI} = 1.95 V to 2.7 V	1.6		
			V_{CCI} = 2.7 V to 3.6 V	2		

6.3 Recommended Operating Conditions (continued)

see (1) (2) (3) (4) (5)

				MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	V_{CCI} = 1.2 V to 1.95 V		V_{CCA} × 0.35	V
			V_{CCI} = 1.95 V to 2.7 V		0.7	
			V_{CCI} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage	Control Inputs(3)		0	3.6	V
V_O	Output voltage(2)	Active state		0	V_{CCO}	V
		3-state		0	3.6	
I_{OH}	High-level output current		V_{CCO} = 1.2 V		–3	mA
			V_{CCO} = 1.4 V to 1.6 V		–6	
			V_{CCO} = 1.65 V to 1.95 V		–8	
			V_{CCO} = 2.3 V to 2.7 V		–9	
			V_{CCO} = 3 V to 3.6 V		–12	
I_{OL}	Low-level output current		V_{CCO} = 1.2 V		3	mA
			V_{CCO} = 1.4 V to 1.6 V		6	
			V_{CCO} = 1.65 V to 1.95 V		8	
			V_{CCO} = 2.3 V to 2.7 V		9	
			V_{CCO} = 3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused control inputs of the device must be held at V_{CCI} or GND for proper device operation.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AVCH1T45			UNIT
		DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	210.5	239.9	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130.6	175.0	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.3	94.4	51	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	69.0	75.6	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	N/A	93.9	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted).(1) (2) (5) (6)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage(1)	I_{OH} = –100 µA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V		V_{CCO} - 0.2 V			V
		I_{OH} = –3 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.2 V			0.95		
		I_{OH} = –6 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.4 V		1.05			
		I_{OH} = –8 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 1.65 V		1.2			
		I_{OH} = –9 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 2.3 V		1.75			
		I_{OH} = –12 mA, V_I= V_{IH}	V_{CCA} = V_{CCB} = 3 V		2.3			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V				0.2	V
		I_{OL} = 3 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.2 V			0.15		
		I_{OL} = 6 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.4 V				0.35	
		I_{OL} = 8 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 1.65 V				0.45	
		I_{OL} = 9 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 2.3 V				0.55	
		I_{OL} = 12 mA, V_I= V_{IL}	V_{CCA} = V_{CCB} = 3 V				0.7	
I_I	Control Input (DIR)	V_I = V_{CCA} or GND	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V			±0.025	±1	µA
I_{BHL}	Bus-hold low sustaining current(3)	V_I = 0.42 V	V_{CCA} = V_{CCB} = 1.2 V			25		µA
		V_I = 0.49 V	V_{CCA} = V_{CCB} = 1.4 V		15			
		V_I = 0.58 V	V_{CCA} = V_{CCB} = 1.65 V		25			
		V_I = 0.7 V	V_{CCA} = V_{CCB} = 2.3 V		45			
		V_I = 0.8 V	V_{CCA} = V_{CCB} = 3.3 V		100			
I_{BHH}	Bus-hold high sustaining current(4)	V_I = 0.78 V	V_{CCA} = V_{CCB} = 1.2 V			–25		µA
		V_I = 0.91 V	V_{CCA} = V_{CCB} = 1.4 V		–15			
		V_I = 1.07 V	V_{CCA} = V_{CCB} = 1.65 V		–25			
		V_I = 1.6 V	V_{CCA} = V_{CCB} = 2.3 V		–45			
		V_I = 2 V	V_{CCA} = V_{CCB} = 3.3 V		–100			
I_{BHLO}	Bus-hold low overdrive current(5)	V_I = 0 to V_{CC}	V_{CCA} = V_{CCB} = 1.2 V			50		µA
			V_{CCA} = V_{CCB} = 1.6 V		125			
			V_{CCA} = V_{CCB} = 1.95 V		200			
			V_{CCA} = V_{CCB} = 2.7 V		300			
			V_{CCA} = V_{CCB} = 3.6 V		500			
I_{BHHO}	Bus-hold high overdrive current(6)	V_I = 0 to V_{CC}	V_{CCA} = V_{CCB} = 1.2 V			–50		µA
			V_{CCA} = V_{CCB} = 1.6 V		–125			
			V_{CCA} = V_{CCB} = 1.95 V		–200			
			V_{CCA} = V_{CCB} = 2.7 V		–300			
			V_{CCA} = V_{CCB} = 3.6 V		–500			
I_{off}	Input and output Power-off leakge current	V_I = 0 V to 3.6 V, V_O= 0 V to 3.6 V	V_{CCA} = 0 V, V_{CCB} = 0 V to 3.6 V	A Port		±0.1	±5	µA
			V_{CCA} = 0 V to 3.6 V, V_{CCB} = 0 V	B Port		±0.1	±5	
I_{OZ}	Off-state output current(7)	V_I = V_{CCI} or GND, V_O = V_{CCO} or GND	V_{CCA} = 0 V, V_{CCB} = 3.6 V	A Port		±0.5	±5	µA
			V_{CCA} = 3.6 V, V_{CCB} = 0 V	B port		±0.5	±5	
I_{CCA}	Supply current A port	V_I = V_{CCI} or GND, I_O = 0	V_{CCA} = V_{CCB} = 1.2 V to 3.6 V				10	µA
			V_{CCA} = 0 V, V_{CCB} = 3.6 V				–2	
			V_{CCA} = 3.6 V, V_{CCB} = 0 V				10	

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6.5 Electrical Characteristics (continued)

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted).(1) (2) (5) (6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CCB}	Supply current B port	$V_I = V_{CCI}$ or GND, $I_O = 0$	$V_{CCA} = V_{CCB}$ = 1.2 V to 3.6 V			10	μA
			V_{CCA} = 0 V, V_{CCB} = 3.6 V			10	
			V_{CCA} = 3.6 V, V_{CCB} = 0 V			–2	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$	$V_{CCA} = V_{CCB}$ = 1.2 V to 3.6 V			20	μA
C_i	Input capacitance control pin (DIR)	V_I = 3.3 V or GND	$V_{CCA} = V_{CCB}$ = 3.3 V		2.5		pF
C_{io}	Input and output capacitance A or B port	V_O = 3.3 V or GND	$V_{CCA} = V_{CCB}$ = 3.3 V		6		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. Measure I_{BHL} after lowering V_{IN} to GND and then raising it to V_{IL} max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. Measure I_{BHH} after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(7) For I/O ports, the parameter I_{OZ} includes the input leakage current.

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6.6 Switching Characteristics, V_{CCA}= 1.2V

T_A= 25°C (see Figure 7-1).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		3.3		ns
				V_{CCB} = 1.5 V		2.7		
				V_{CCB} = 1.8 V		2.4		
				V_{CCB} = 2.5 V		2.3		
				V_{CCB} = 3.3 V		2.4		
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		3.3		ns
				V_{CCB} = 1.5 V		3.1		
				V_{CCB} = 1.8 V		2.9		
				V_{CCB} = 2.5 V		2.8		
				V_{CCB} = 3.3 V		2.7		
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	A	V_{CCB} = 1.2 V		5.1		ns
				V_{CCB} = 1.5 V		5.2		
				V_{CCB} = 1.8 V		5.3		
				V_{CCB} = 2.5 V		5.2		
				V_{CCB} = 3.3 V		3.7		
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	B	V_{CCB} = 1.2 V		5.3		ns
				V_{CCB} = 1.5 V		4.3		
				V_{CCB} = 1.8 V		4		
				V_{CCB} = 2.5 V		3.3		
				V_{CCB} = 3.3 V		3.7		
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	A	V_{CCB} = 1.2 V		8.5		ns
				V_{CCB} = 1.5 V		6.9		
				V_{CCB} = 1.8 V		6.4		
				V_{CCB} = 2.5 V		5.5		
				V_{CCB} = 3.3 V		6.1		
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	B	V_{CCB} = 1.2 V		8.3		ns
				V_{CCB} = 1.5 V		7.8		
				V_{CCB} = 1.8 V		7.7		
				V_{CCB} = 2.5 V		7.5		
				V_{CCB} = 3.3 V		5.9		

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

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6.7 Switching Characteristics, V_{CCA}= 1.5V ± 0.1V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 7-1).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.9		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.7		5.6	
				V_{CCB} = 1.8 V ± 0.15 V	0.6		4.2	
				V_{CCB} = 2.5 V ± 0.2 V	0.5		4.2	
				V_{CCB} = 3.3 V ± 0.3 V	0.5		3.8	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		2.6		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.6		5.5	
				V_{CCB} = 1.8 V ± 0.15 V	0.4		5.3	
				V_{CCB} = 2.5 V ± 0.2 V	0.3		4.9	
				V_{CCB} = 3.3 V ± 0.3 V	0.3		4.8	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	A	V_{CCB} = 1.2 V		3.8		ns
				V_{CCB} = 1.5 V ± 0.1 V	1.6		6.7	
				V_{CCB} = 1.8 V ± 0.15 V	1.5		6.8	
				V_{CCB} = 2.5 V ± 0.2 V	0.3		6.9	
				V_{CCB} = 3.3 V ± 0.3 V	0.9		6.9	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	B	V_{CCB} = 1.2 V		5.1		ns
				V_{CCB} = 1.5 V ± 0.1 V	1.8		8.1	
				V_{CCB} = 1.8 V ± 0.15 V	1.6		7.1	
				V_{CCB} = 2.5 V ± 0.2 V	1.1		4.7	
				V_{CCB} = 3.3 V ± 0.3 V	1.4		4.5	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	A	V_{CCB} = 1.2 V		7.7		ns
				V_{CCB} = 1.5 V ± 0.1 V			13.6	
				V_{CCB} = 1.8 V ± 0.15 V			12.4	
				V_{CCB} = 2.5 V ± 0.2 V			9.6	
				V_{CCB} = 3.3 V ± 0.3 V			9.3	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	B	V_{CCB} = 1.2 V		6.7		ns
				V_{CCB} = 1.5 V ± 0.1 V			12.3	
				V_{CCB} = 1.8 V ± 0.15 V			12	
				V_{CCB} = 2.5 V ± 0.2 V			11.1	
				V_{CCB} = 3.3 V ± 0.3 V			10.7	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

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6.8 Switching Characteristics, V_{CCA}= 1.8V ± 0.15V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 7-1).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.8		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.6		5.3	
				V_{CCB} = 1.8 V ± 0.15 V	0.5		5	
				V_{CCB} = 2.5 V ± 0.2 V	0.4		3.9	
				V_{CCB} = 3.3 V ± 0.3 V	0.4		3.4	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		2.3		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.5		5.2	
				V_{CCB} = 1.8 V ± 0.15 V	0.4		5	
				V_{CCB} = 2.5 V ± 0.2 V	0.3		4.6	
				V_{CCB} = 3.3 V ± 0.3 V	0.2		4.4	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	A	V_{CCB} = 1.2 V		3.8		ns
				V_{CCB} = 1.5 V ± 0.1 V	1.6		5.9	
				V_{CCB} = 1.8 V ± 0.15 V	1.6		5.9	
				V_{CCB} = 2.5 V ± 0.2 V	1.6		5.9	
				V_{CCB} = 3.3 V ± 0.3 V	0.5		6	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	B	V_{CCB} = 1.2 V		5		ns
				V_{CCB} = 1.5 V ± 0.1 V	1.8		7.7	
				V_{CCB} = 1.8 V ± 0.15 V	1.4		6.8	
				V_{CCB} = 2.5 V ± 0.2 V	1		4.4	
				V_{CCB} = 3.3 V ± 0.3 V	1.4		4.3	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	A	V_{CCB} = 1.2 V		7.3		ns
				V_{CCB} = 1.5 V ± 0.1 V			12.9	
				V_{CCB} = 1.8 V ± 0.15 V			11.8	
				V_{CCB} = 2.5 V ± 0.2 V			9	
				V_{CCB} = 3.3 V ± 0.3 V			8.7	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	B	V_{CCB} = 1.2 V		6.5		ns
				V_{CCB} = 1.5 V ± 0.1 V			11.2	
				V_{CCB} = 1.8 V ± 0.15 V			10.9	
				V_{CCB} = 2.5 V ± 0.2 V			9.8	
				V_{CCB} = 3.3 V ± 0.3 V			9.4	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

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6.9 Switching Characteristics, V_{CCA}= 2.5V ± 0.2V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 7-1).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.6		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.5		4.9	
				V_{CCB} = 1.8 V ± 0.15 V	0.4		4.6	
				V_{CCB} = 2.5 V ± 0.2 V	0.3		3.4	
				V_{CCB} = 3.3 V ± 0.3 V	0.3		3	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		2.2		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.4		4.2	
				V_{CCB} = 1.8 V ± 0.15 V	0.3		3.8	
				V_{CCB} = 2.5 V ± 0.2 V	0.2		3.4	
				V_{CCB} = 3.3 V ± 0.3 V	0.2		3.3	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	A	V_{CCB} = 1.2 V		2.8		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.3		3.8	
				V_{CCB} = 1.8 V ± 0.15 V	0.8		3.8	
				V_{CCB} = 2.5 V ± 0.2 V	0.4		3.8	
				V_{CCB} = 3.3 V ± 0.3 V	0.5		3.8	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	B	V_{CCB} = 1.2 V		4.9		ns
				V_{CCB} = 1.5 V ± 0.1 V	2		7.6	
				V_{CCB} = 1.8 V ± 0.15 V	1.5		6.5	
				V_{CCB} = 2.5 V ± 0.2 V	0.6		4.1	
				V_{CCB} = 3.3 V ± 0.3 V	1		4	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	A	V_{CCB} = 1.2 V		7.1		ns
				V_{CCB} = 1.5 V ± 0.1 V			11.8	
				V_{CCB} = 1.8 V ± 0.15 V			10.3	
				V_{CCB} = 2.5 V ± 0.2 V			7.5	
				V_{CCB} = 3.3 V ± 0.3 V			7.3	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	B	V_{CCB} = 1.2 V		5.4		ns
				V_{CCB} = 1.5 V ± 0.1 V			8.6	
				V_{CCB} = 1.8 V ± 0.15 V			8.1	
				V_{CCB} = 2.5 V ± 0.2 V			7	
				V_{CCB} = 3.3 V ± 0.3 V			6.6	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

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6.10 Switching Characteristics, V_{CCA}= 3.3V ± 0.3V

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted) (see Figure 7-1).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	A	B	V_{CCB} = 1.2 V		2.6		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.4		4.7	
				V_{CCB} = 1.8 V ± 0.15 V	0.3		4.4	
				V_{CCB} = 2.5 V ± 0.2 V	0.2		3.3	
				V_{CCB} = 3.3 V ± 0.3 V	0.2		2.8	
t_{PLH}, t_{PHL}	Propagation delay time: low-to-high-level output and high-to-low level output	B	A	V_{CCB} = 1.2 V		2.2		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.4		3.8	
				V_{CCB} = 1.8 V ± 0.15 V	0.3		3.4	
				V_{CCB} = 2.5 V ± 0.2 V	0.2		3	
				V_{CCB} = 3.3 V ± 0.3 V	0.1		2.8	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	A	V_{CCB} = 1.2 V		3.1		ns
				V_{CCB} = 1.5 V ± 0.1 V	1.3		4.3	
				V_{CCB} = 1.8 V ± 0.15 V	1.3		4.3	
				V_{CCB} = 2.5 V ± 0.2 V	1.3		4.3	
				V_{CCB} = 3.3 V ± 0.3 V	1.3		4.3	
t_{PZH}, t_{PZL}	Enable time: to high level(1) and to low level(1)	DIR	B	V_{CCB} = 1.2 V		4		ns
				V_{CCB} = 1.5 V ± 0.1 V	0.7		7.4	
				V_{CCB} = 1.8 V ± 0.15 V	0.6		6.5	
				V_{CCB} = 2.5 V ± 0.2 V	0.7		4	
				V_{CCB} = 3.3 V ± 0.3 V	1.5		3.9	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	A	V_{CCB} = 1.2 V		6.2		ns
				V_{CCB} = 1.5 V ± 0.1 V			11.2	
				V_{CCB} = 1.8 V ± 0.15 V			9.9	
				V_{CCB} = 2.5 V ± 0.2 V			7	
				V_{CCB} = 3.3 V ± 0.3 V			6.7	
t_{PHZ}, t_{PLZ}	Disable time: from high level and from low level	DIR	B	V_{CCB} = 1.2 V		5.7		ns
				V_{CCB} = 1.5 V ± 0.1 V			8.9	
				V_{CCB} = 1.8 V ± 0.15 V			8.5	
				V_{CCB} = 2.5 V ± 0.2 V			7.2	
				V_{CCB} = 3.3 V ± 0.3 V			6.8	

(1) The enable time is a calculated value, derived using the formula shown in *Enable Times*.

6.11 Operating Characteristics

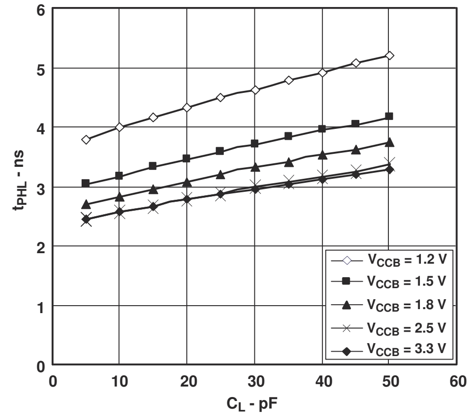
T_A= 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		TYP	UNIT
C_{pdA}	Power dissipation capacitance per transceiver(1) port A	A	B	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.2 V	3	pF
					$V_{CCA} = V_{CCB}$ = 1.5 V	3	
					$V_{CCA} = V_{CCB}$ = 1.8 V	3	
					$V_{CCA} = V_{CCB}$ = 2.5 V	3	
					$V_{CCA} = V_{CCB}$ = 3.3 V	4	
		B	A	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.2 V	14	pF
					$V_{CCA} = V_{CCB}$ = 1.5 V	14	
					$V_{CCA} = V_{CCB}$ = 1.8 V	14	
					$V_{CCA} = V_{CCB}$ = 2.5 V	15	
					$V_{CCA} = V_{CCB}$ = 3.3 V	16	
C_{pdB}	Power dissipation capacitance per transceiver(1) port B	A	B	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.2 V	14	pF
					$V_{CCA} = V_{CCB}$ = 1.5 V	14	
					$V_{CCA} = V_{CCB}$ = 1.8 V	14	
					$V_{CCA} = V_{CCB}$ = 2.5 V	15	
					$V_{CCA} = V_{CCB}$ = 3.3 V	16	
		B	A	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	$V_{CCA} = V_{CCB}$ = 1.2 V	3	pF
					$V_{CCA} = V_{CCB}$ = 1.5 V	3	
					$V_{CCA} = V_{CCB}$ = 1.8 V	3	
					$V_{CCA} = V_{CCB}$ = 2.5 V	3	
					$V_{CCA} = V_{CCB}$ = 3.3 V	4	

(1) See *CMOS Power Consumption and Cpd Calculation*.

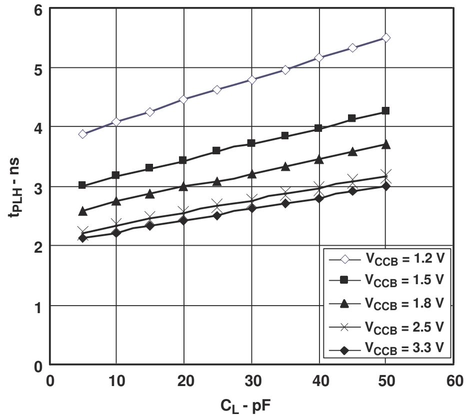
6.12 Typical Characteristics

T_A= 25°C



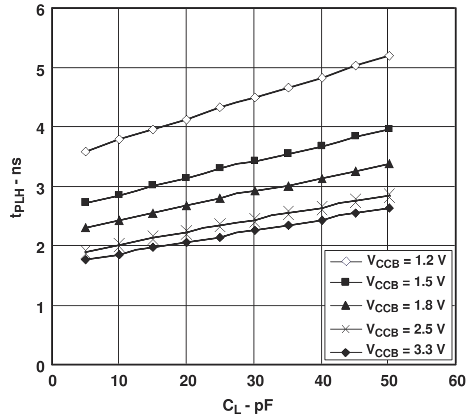
V_{CCA}= 1.2 V

Figure 6-1. Typical Propagation Delay (A to B) vs Load Capacitance



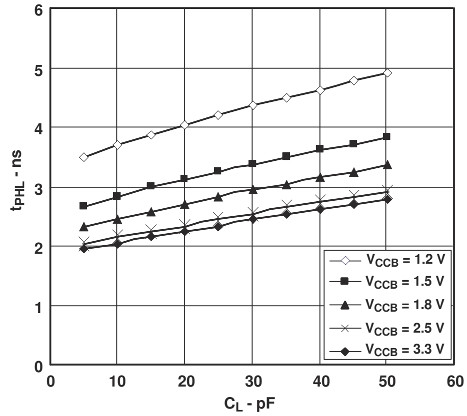
V_{CCA}= 1.2 V

Figure 6-2. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA}= 1.5 V

Figure 6-3. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA}= 1.5 V

Figure 6-4. Typical Propagation Delay (A to B) vs Load Capacitance

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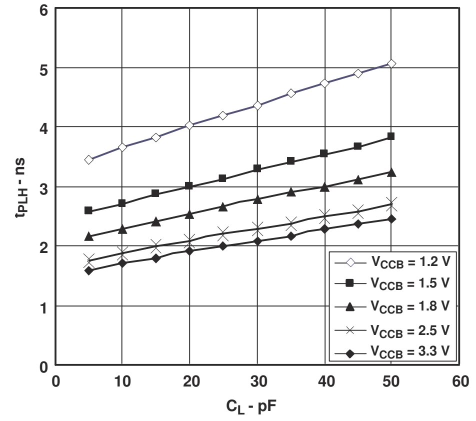
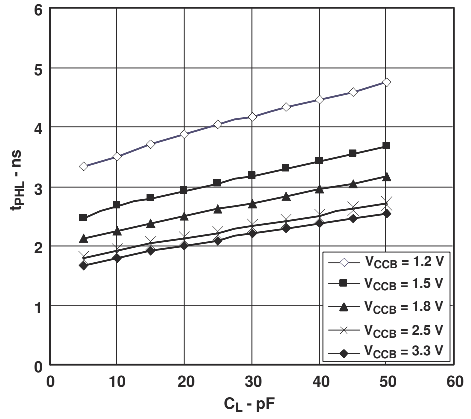
6.12 Typical Characteristics (continued)

T_A= 25°C



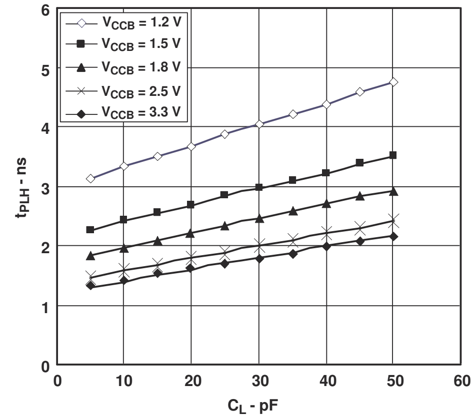
V_{CCA}= 1.8 V

Figure 6-5. Typical Propagation Delay (A to B) vs Load Capacitance



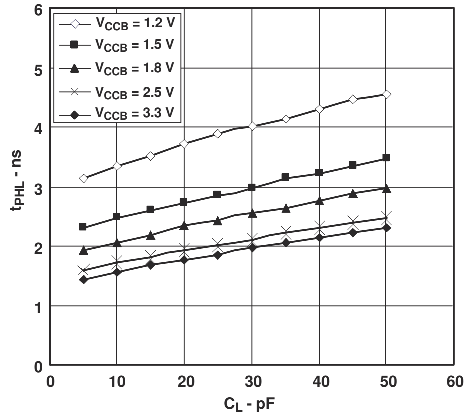
V_{CCA}= 1.8 V

Figure 6-6. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA}= 2.5 V

Figure 6-7. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA}= 2.5 V

Figure 6-8. Typical Propagation Delay (A to B) vs Load Capacitance

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6.12 Typical Characteristics (continued)

T_A= 25°C

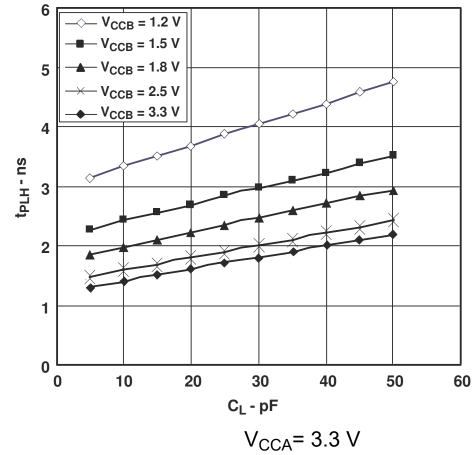


Figure 6-9. Typical Propagation Delay (A to B) vs Load Capacitance

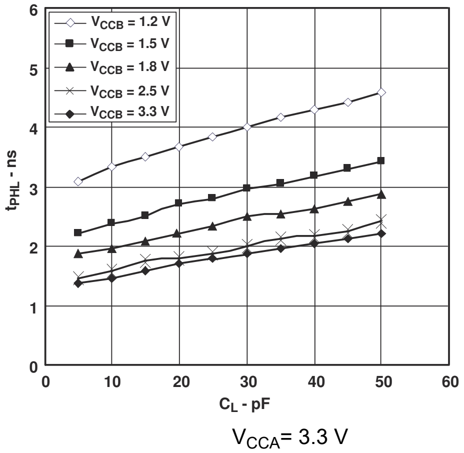
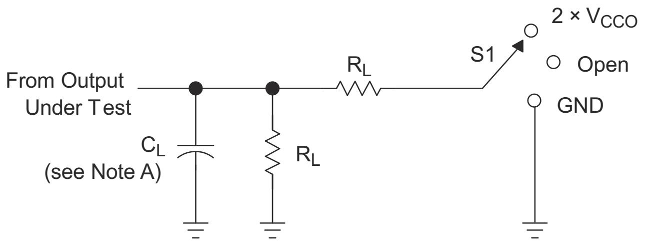


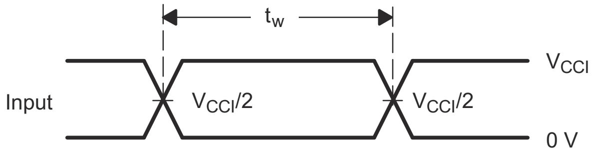
Figure 6-10. Typical Propagation Delay (A to B) vs Load Capacitance

7 Parameter Measurement Information



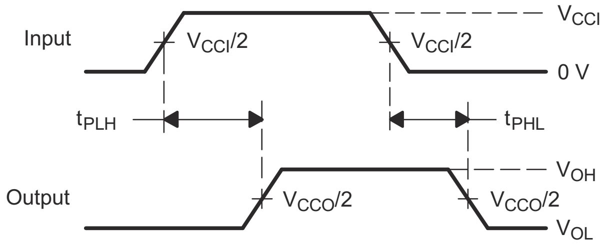
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

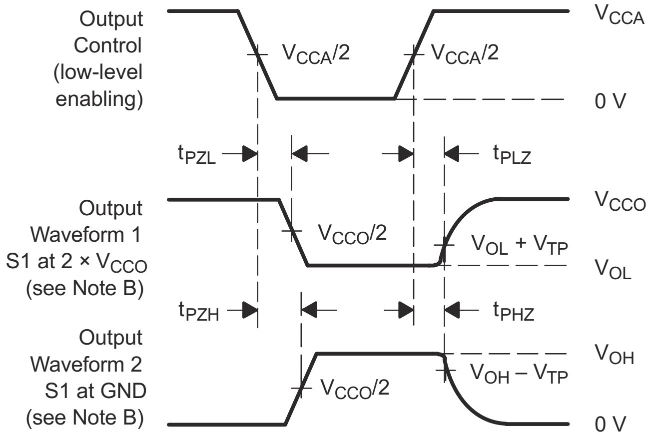


VOLTAGE WAVEFORMS
PULSE DURATION

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kW	0.1 V
1.5 V ± 0.1 V	15 pF	2 kW	0.1 V
1.8 V ± 0.15 V	15 pF	2 kW	0.15 V
2.5 V ± 0.2 V	15 pF	2 kW	0.15 V
3.3 V ± 0.3 V	15 pF	2 kW	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 7-1. Load Circuit and Voltage Waveforms

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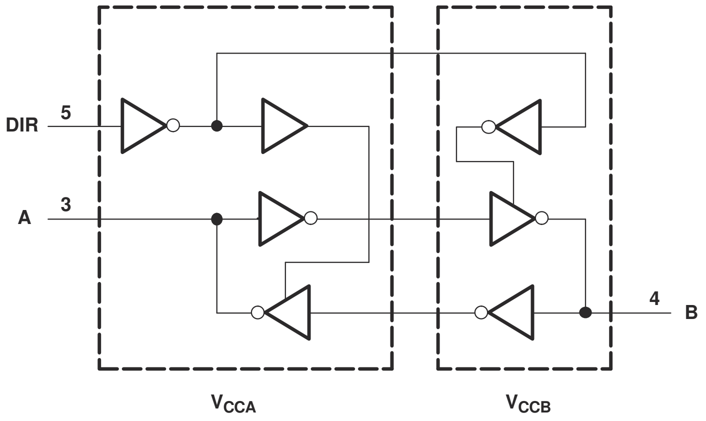
8 Detailed Description

8.1 Overview

The SN74AVCH1T45 is a single-bit, dual-supply, noninverting voltage level translator. Pins A and DIR are referenced to V_{CCA}, while pin B is referenced to V_{CCB}. Both the A port and B port can accept I/O voltages ranging from 1.2V to 3.6V. The high on DIR allows data transmission from Port A to Port B and a low on DIR allows data transmission from Port B to Port A. See application report, *AVC Logic Family Technology and Applications*, for more information.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2V to 3.6V, making the device an excellent choice for translating between any of the voltage nodes (1.2V, 1.8V, 2.5V and 3.3V).

8.3.2 Supports High-Speed Translation

SN74AVCH1T45 can support high data rate applications, which can be calculated from the maximum propagation delay. This support is dependent on output load. For example, a 1.8V to 3.3V conversion yields a maximum data rate of 500Mbps.

8.3.3 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the SN74AVCH1T45 when the device is powered down. This event can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

8.3.4 Active Bus-Hold Circuitry

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state, which helps with board space savings and reduced component costs. TI does not recommend using pullup or pulldown resistors with bus-hold circuitry. See applications report, *Bus-Hold Circuit*, for more information.

8.3.5 V_{CC} Isolation

The V_{CC} isolation feature places both ports in a high-impedance state (I_{OZ} as shown in *Electrical Characteristics*) if either V_{CCA} or V_{CCB} are at GND (or < 0.4V). This feature prevents false logic levels from being presented to either bus.

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8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74AVCH1T45.

Table 8-1. Function Table

DIR	OPERATION
L	B data to A bus
H	A data to B bus

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74AVCH1T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 500Mbps when the device translate signal is from 1.8V to 3.3V.

9.2 Typical Applications

9.2.1 Unidirectional Logic Level-Shifting Application

Figure 9-1 shows an example of the SN74AVCH1T45 being used in a unidirectional logic level-shifting application.

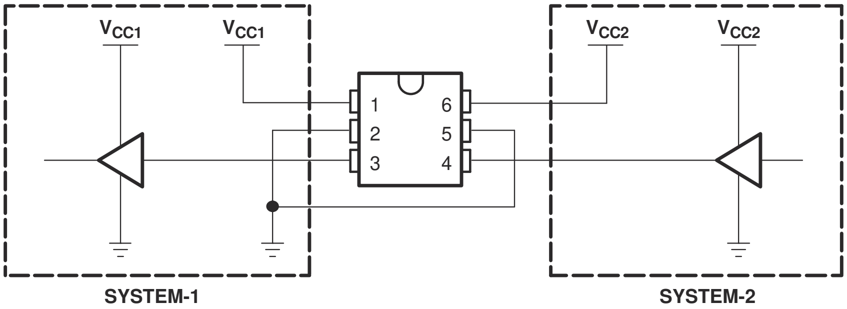

Figure 9-1. Unidirectional Logic Level-Shifting Application Diagram

Table 9-1. Data Transmission: SYSTEM-1 and SYSTEM-2

PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.2V to 3.6V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V_{CC1} voltage.
4	B	IN	Input threshold value depends on V_{CC2} voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.2V to 3.6V)

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9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-2.

Table 9-2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage	1.2V to 3.6V
Output voltage	1.2V to 3.6V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVCH1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVCH1T45 device is driving to determine the output voltage range.

9.2.1.3 Application Curve

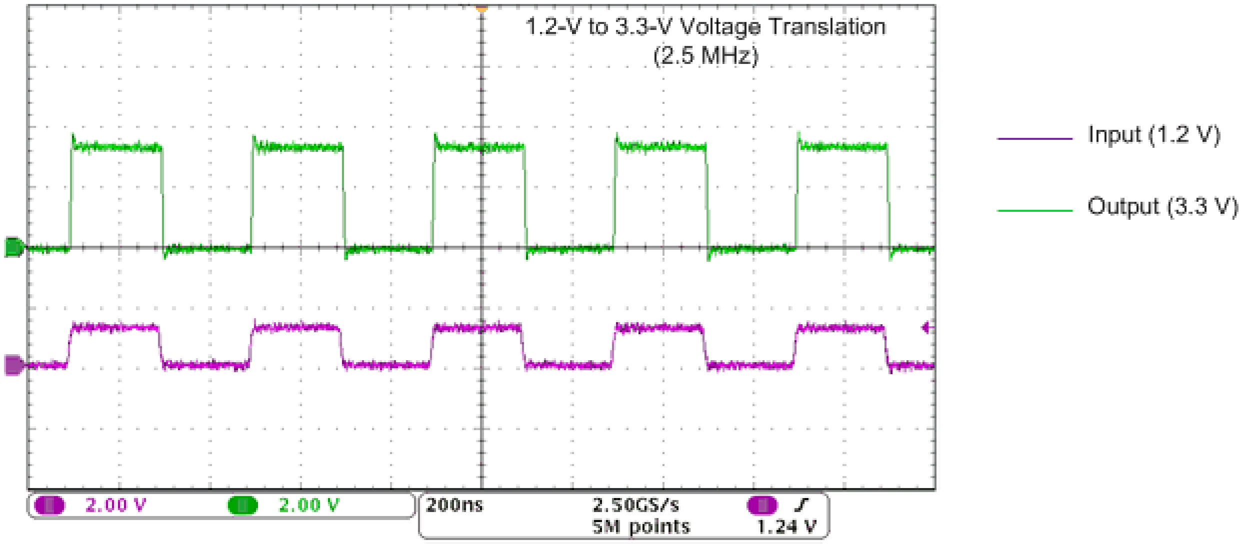

Figure 9-2. Translation Up (1.2V to 3.3V) at 2.5MHz

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9.2.2 Bidirectional Logic Level-Shifting Application

Figure 9-3 shows the SN74AVCH1T45 being used in a bidirectional logic level-shifting application. Take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions because the SN74AVCH1T45 does not have an output-enable (OE) pin.

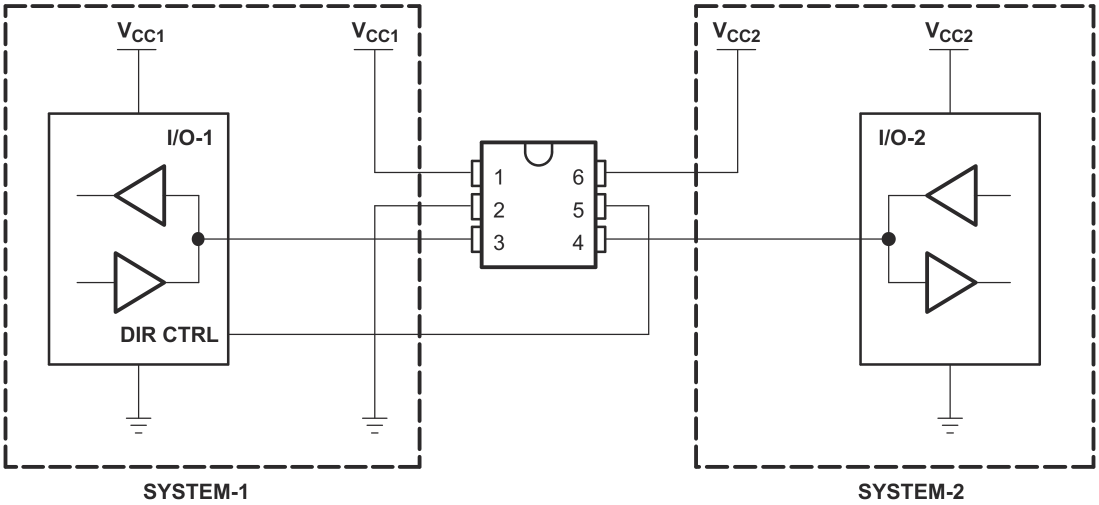

Figure 9-3. Bidirectional Logic Level-Shifting Application Diagram

The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 9-3. Data Transmission: SYSTEM-1 and SYSTEM-2

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled.
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled.
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

9.2.2.1 Design Requirements

Refer to *Design Requirements* found in *Unidirectional Logic Level-Shifting Application*.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Enable Times

Calculate the enable times for the SN74AVCH1T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ}(DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ}(DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ}(DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ}(DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVCH1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

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9.2.2.3 Application Curve

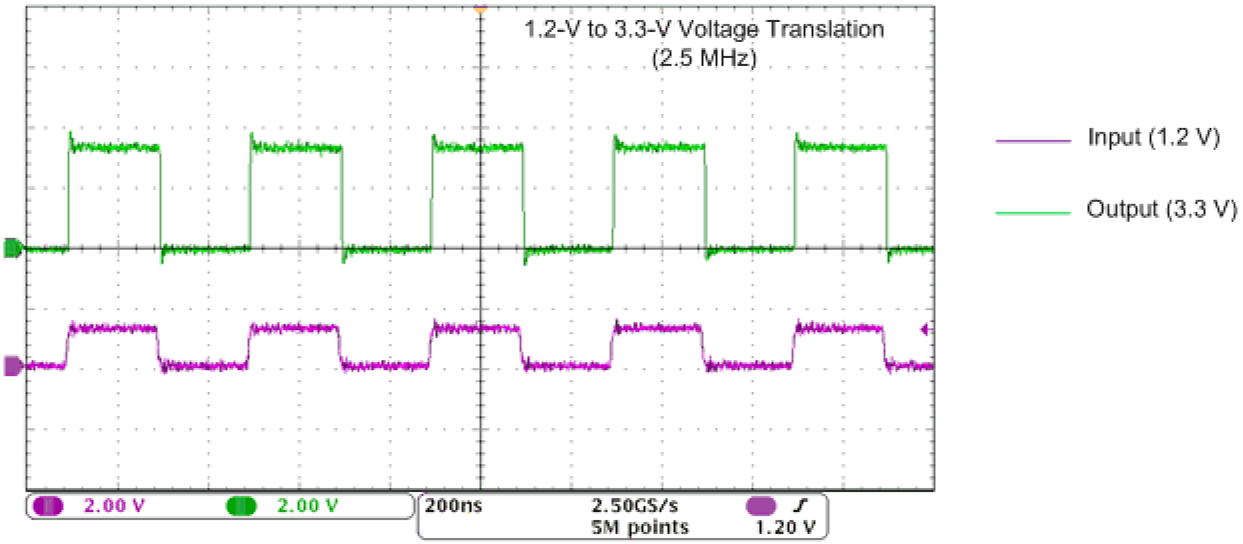

Figure 9-4. Translation Up (1.2V to 3.3V) at 2.5MHz

10 Power Supply Recommendations

A proper power-up sequence must be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

Table 10-1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0V	**1.2V**	**1.5V**	**1.8V**	**2.5V**	**3.3V**	
0V	0	<0.5	<0.5	<0.5	<0.5	<0.5	µA
1.2V	<0.5	<1	<1	<1	<1	1	
1.5V	<0.5	<1	<1	<1	<1	1	
1.8V	<0.5	<1	<1	<1	<1	<1	
2.5V	<0.5	1	<1	<1	<1	<1	
3.3V	<0.5	1	<1	<1	<1	<1	

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11 Layout

11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines for better device reliability.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors, or pullup resistors, to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

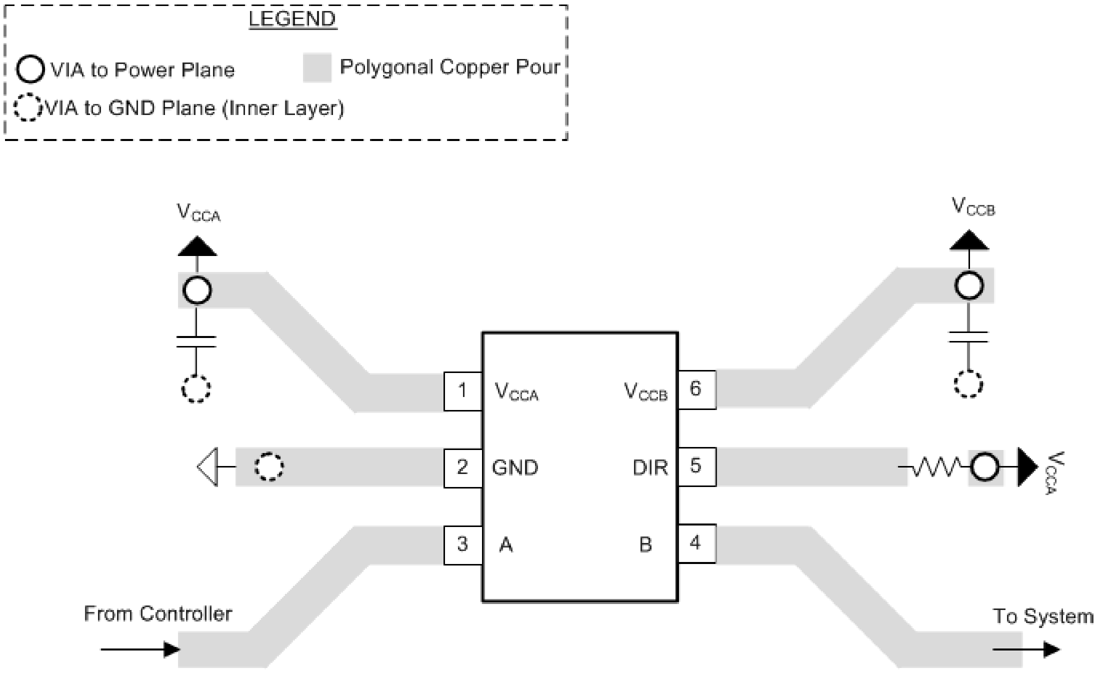

Figure 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/ Level-Shifters*, application report
- *Bus-Hold Circuit*, application report
- *AVC Logic Family Technology and Applications*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2016) to Revision F (April 2024)	**Page**
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated DBV and DCK thermal information	5

Changes from Revision D (January 2008) to Revision E (March 2016)	**Page**
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AVCH1T45DBVRE4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
74AVCH1T45DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
74AVCH1T45DCKRE4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
74AVCH1T45DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ET1F, ET1R)
SN74AVCH1T45DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKT.B	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TFF, TFR)
SN74AVCH1T45DCKTG4	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TFR
SN74AVCH1T45DCKTG4.B	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TFR
SN74AVCH1T45YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TE2, TEN)
SN74AVCH1T45YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TE2, TEN)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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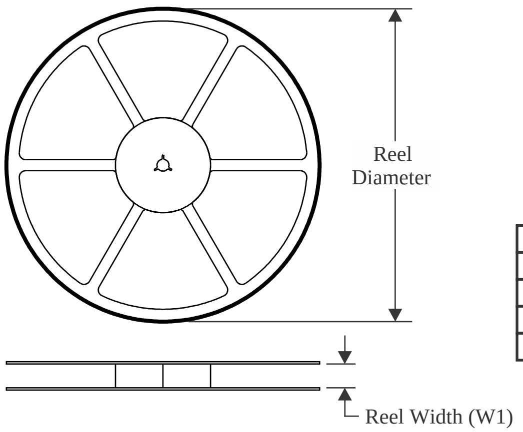
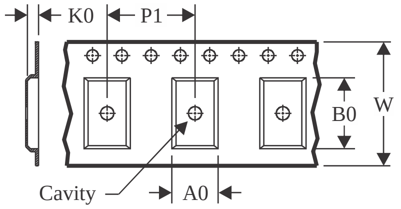
TAPE AND REEL INFORMATION

REEL DIMENSIONS

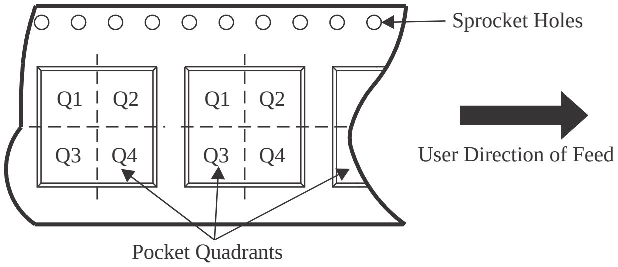


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

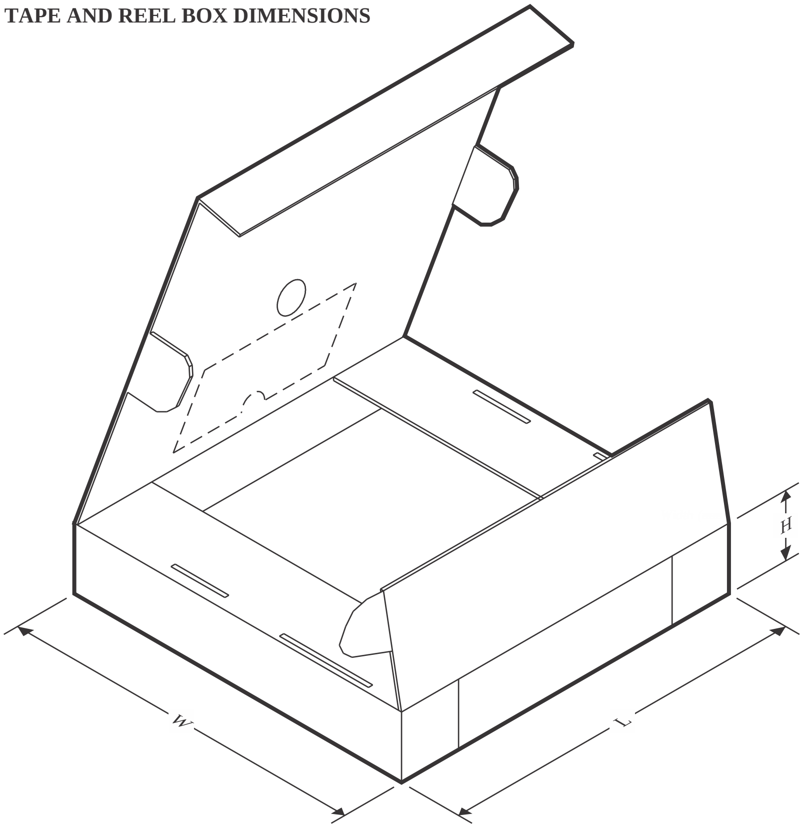
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AVCH1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVCH1T45DCKRG4	SC70	DCK	6	3000	180.0	8.4	2.3	2.52	1.2	4.0	8.0	Q3
SN74AVCH1T45DCKRG4	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVCH1T45DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVCH1T45DCKTG4	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AVCH1T45YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



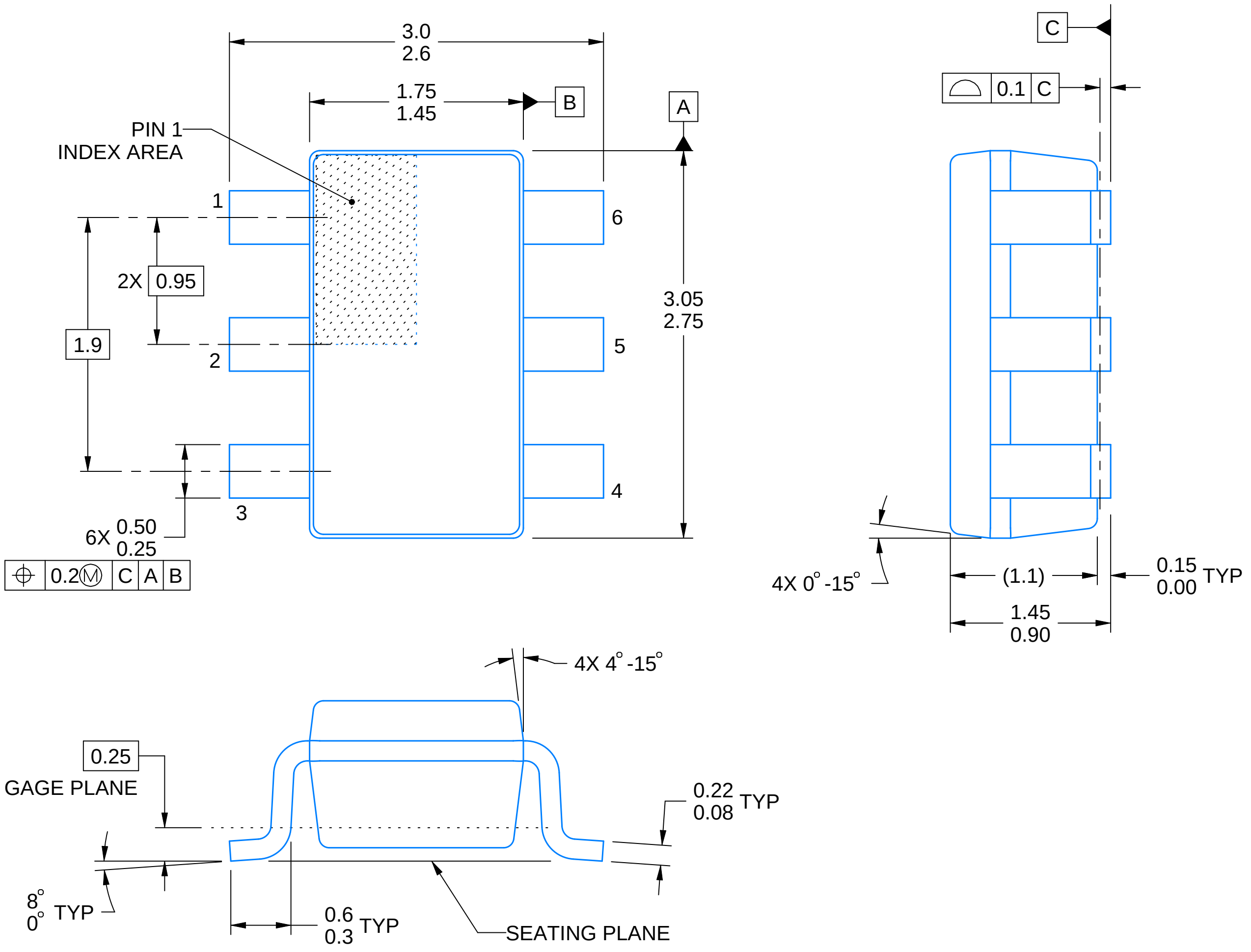
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH1T45DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AVCH1T45DBVRG4	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AVCH1T45DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AVCH1T45DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AVCH1T45DCKRG4	SC70	DCK	6	3000	214.0	199.0	55.0
SN74AVCH1T45DCKRG4	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AVCH1T45DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AVCH1T45DCKTG4	SC70	DCK	6	250	202.0	201.0	28.0
SN74AVCH1T45YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

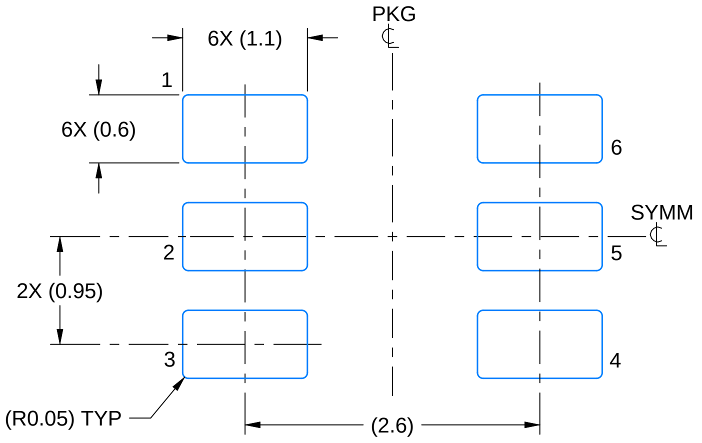


4214840/G 08/2024

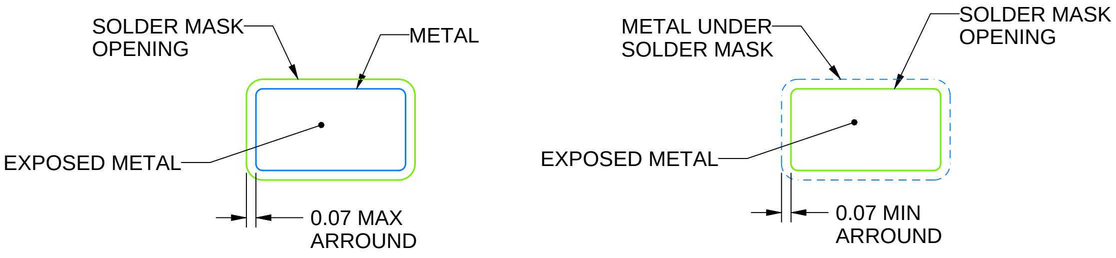
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



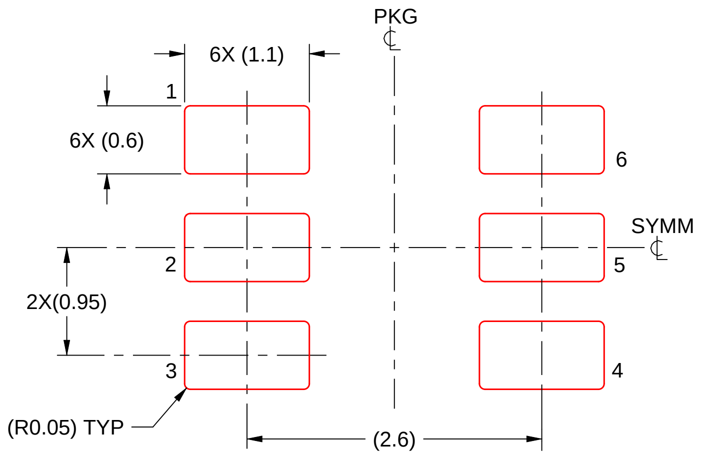
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

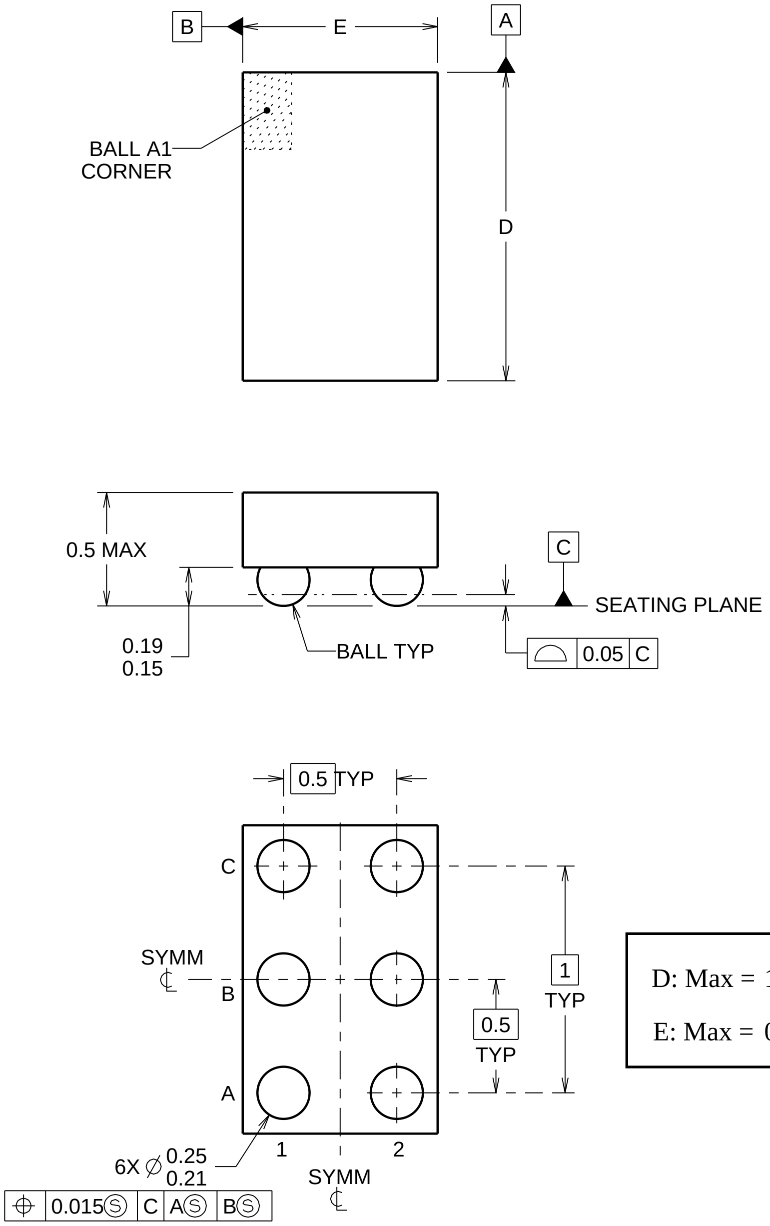
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

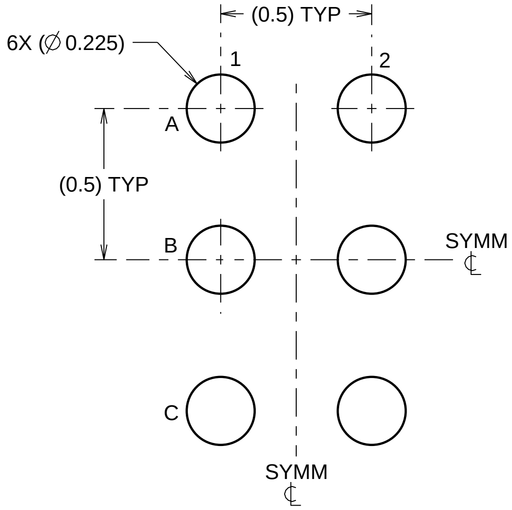
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

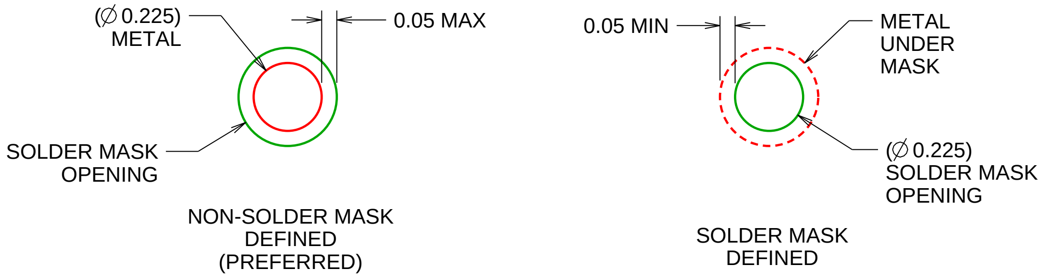
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



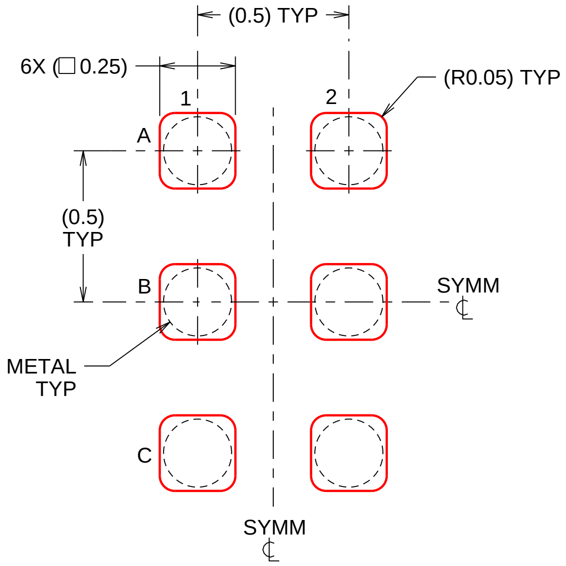
LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

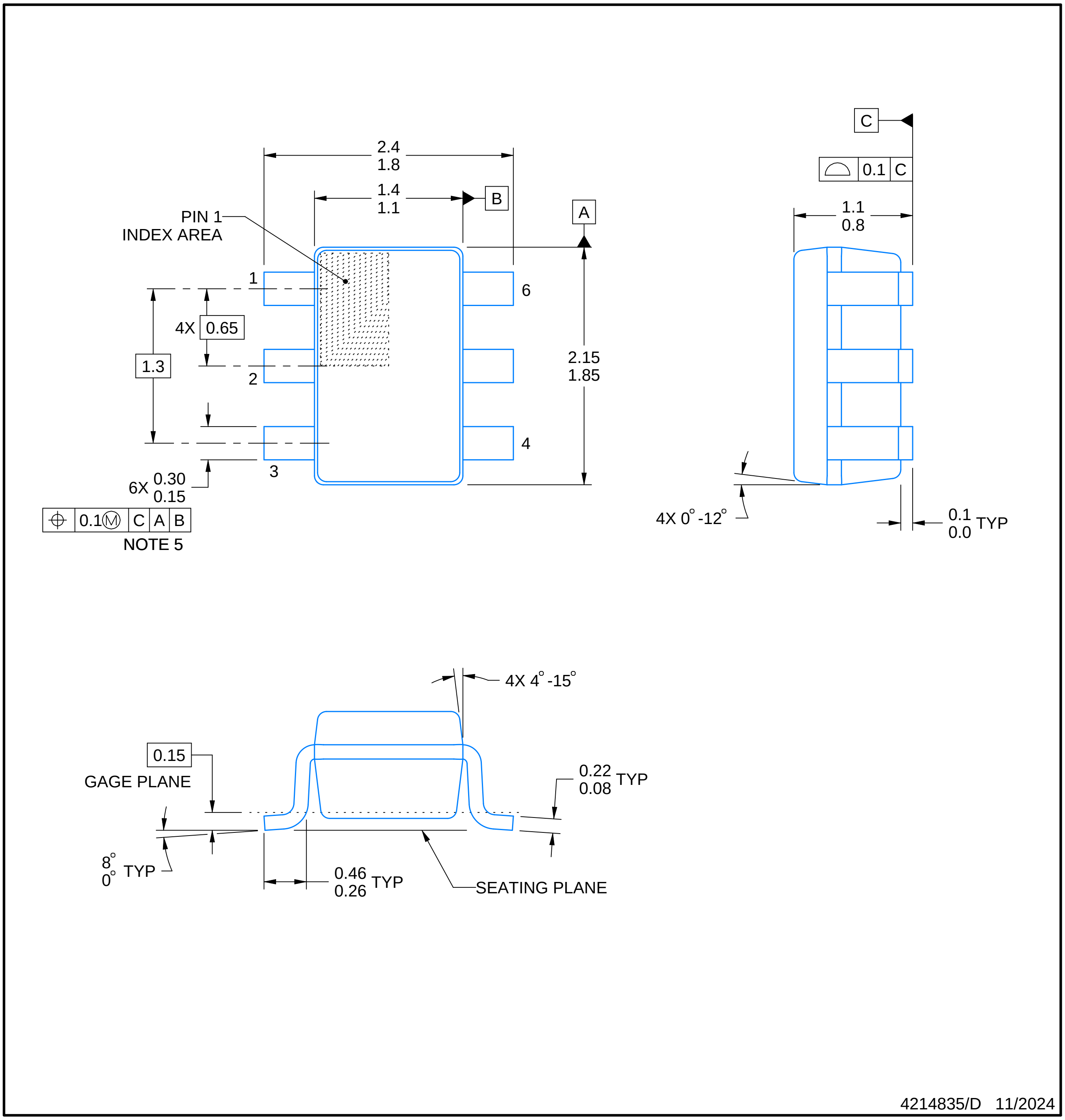
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

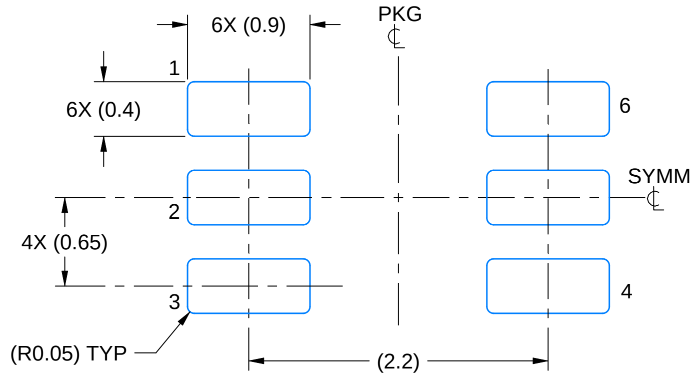
SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

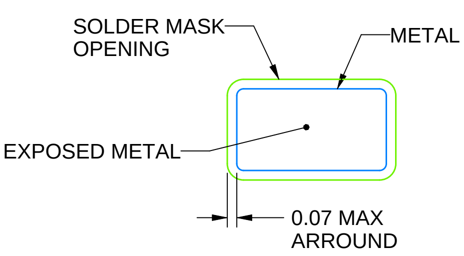


NOTES:

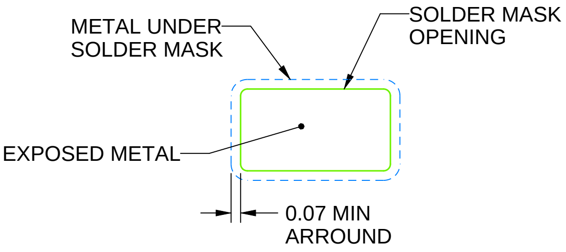
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

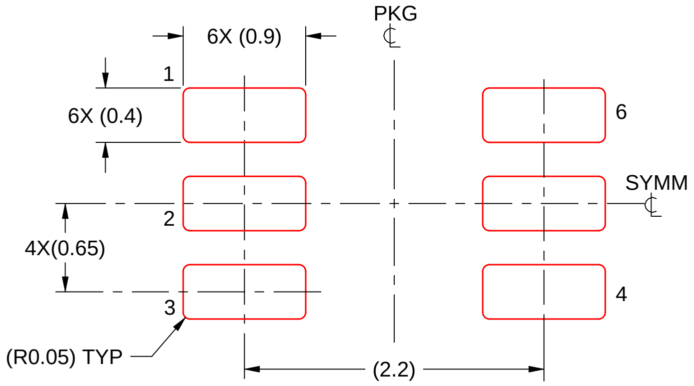


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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