SN74AVC4T234 4-Bit Dual-Supply Unidirectional Noninverting Voltage Translator

1 Features

- Wide operating V_{CC} range of 0.9 V to 3.6 V
- 3.6-V I/O Tolerant to support mixed-mode signal operation
- Max t_{pd} of 3.7 ns at 3.3 V
- Balanced propagation delays: $t_{PLH} = t_{PHL}$
- Low static-power consumption, 5-µA Max I_{CC}
- Outputs disabled if either V_{CC} goes to 0V
- ±3-mA Output drive at 1.8 V
- 26-Ω series resistor on A-side outputs
- I_{off} supports partial power-down-mode operation
- Input hysteresis allows slow input transition and better switching noise immunity at input
- Maximum data rates
  - 380 Mbps (1.8-V to 3.3-V translation)
  - 200 Mbps (<1.8-V to 3.3-V translation)
  - 200 Mbps (translate to 2.5 V or 1.8 V)
  - 150 Mbps (translate to 1.5 V)
  - 100 Mbps (translate to 1.2 V)
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 500-V charged-device model (C101)

2 Applications

- Personal electronics
- Industrial
- Enterprise
- Telecom

3 Description

This 4-bit non-inverting bus transceiver uses two separate configurable power-supply rails to enable asynchronous communication between B-port inputs and A-port outputs. The A port is designed to track V_{CCA} while the B port is designed to track V_{CCB}. Both V_{CCA} and V_{CCB} are configurable from 0.9 V to 3.6 V.

The SN74AVC4T234 solution offers the industry's low-power needs in battery-powered portable applications by ensuring both a very low static and dynamic power consumption across the entire V_{CC} range of 0.9 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity.

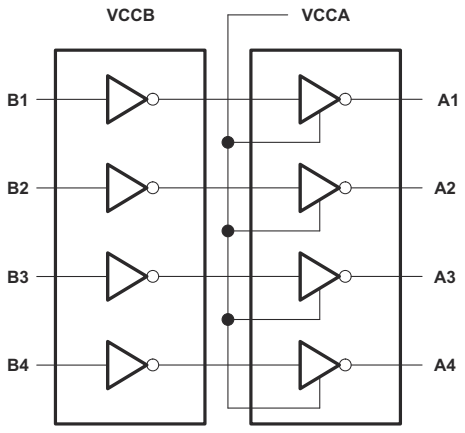
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then A-side ports are in the high-impedance state.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74AVC4T234ZSU	uCSP (11)	2.00 mm × 1.40 mm
SN74AVC4T234ZWA	NFBGA (11)	2.00 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2011) to Revision B (July 2020)	Page
• Format to new TI data sheet standard with additional information throughout	1
• Removed Feature "Input-Disabled Feature Allows Floating Input Conditions"	1
• Added Feature "Outputs Disabled if Either V_{CC} goes to 0V"	1
• Updated the numbering format for tables, figures and cross-references throughout the document	1
• Removed *Ordering Information* table	1
• Added ZWA package as orderable	1
• Added *ESD Ratings* table	4
• Added Thermal Information table	6
• Added Feature Description section.	10
• Added Device Functional Modes section	10
• Added Application and Implementation section	11
• Added Power Supply Recommendations section	12
• Added Layout section	12
• Added Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections.	13

5 Pin Configuration and Functions

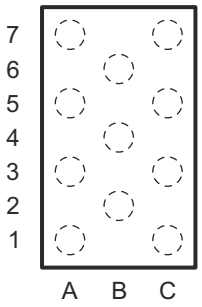


Figure 5-1. ZSU/ZWA Package 11-Pin uCSP Transparent Top View

Pin Functions

PIN	NO.	TYPE	DESCRIPTION
NAME	ZSU, ZWA		
B1	C7	I	Channel 1 Data input port
B2	C5	I	Channel 2 Data input port
B3	C3	I	Channel 3 Data input port
B4	C1	I	Channel 4 Data input port
A1	A7	O	Channel 1 Data output port
A2	A5	O	Channel 2 Data output port
A3	A3	O	Channel 3 Data output port
A4	A1	O	Channel 4 Data output port
V_{CCA}	B6	—	A-side output port power supply voltage (0.9 V to 3.6 V)
V_{CCB}	B4	—	B-side input port power supply voltage (0.9 V to 3.6 V)
GND	B2	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	Output ports (A port)	–0.5	4.6	V
		Input ports (B port)	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			V_{CCI} (1) (3)	V_{CCO} (2)	MIN	MAX	UNIT
V_{CCA}	Supply voltage				0.9	3.6	V
V_{CCB}	Supply voltage				0.9	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	0.9 V to 1.1 V		V_{CCI} × 0.8	3.6	V
			1.1 V to 1.4 V		V_{CCI} × 0.8	3.6	
			1.4 V to 1.95 V		V_{CCI} × 0.65	3.6	
			2.3 V to 2.7 V		V_{CCI} × 0.65	3.6	
			3 V to 3.6 V		V_{CCI} × 0.65	3.6	
V_{IL}	Low-level input voltage	Data inputs(4)	0.9 V to 1.1 V		0	V_{CCI} × 0.2	V
			1.1 V to 1.4 V		0	V_{CCI} × 0.2	
			1.1 V to 1.95 V		0	V_{CCI} × 0.35	
			2.3 V to 2.7 V		0	V_{CCI} × 0.35	
			3 V to 3.6 V		0	V_{CCI} × 0.35	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
I_{OH}	High-level output current			0.9 V to 1.1 V		–0.1	mA
				1.1 V to 1.3 V		–1	
				1.4 V to 1.6 V		–2	
				1.65 V to 1.95 V		–3	
				2.3 V to 2.7 V		–6	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			0.9 V to 1.1 V		0.1	mA
				1.1 V to 1.3 V		1	
				1.4 V to 1.6 V		2	
				1.65 V to 1.95 V		3	
				2.3 V to 2.7 V		6	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate			3 V to 3.6 V		10	ns/V
				2.3 V to 2.7 V		20	
				1.65 V to 1.95 V		50	
				1.4 V to 1.6 V		100	
				1.1 V to 1.3 V		100	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CCB} input port.
(2) V_{CCO} is the V_{CCA} output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V

6.4 Thermal Information

THERMAL METRIC[1]		SN74AVC4T234 ZSU (uCSP) 11 PINS	SN74AVC4T234 ZWA (NFBGA) 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	165.9	181.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.8	136.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	123.2	137.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.4	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	122.9	137.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER[1] [2]		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	0.9 V	0.9 V to 3.6 V	T_A = –40°C to 85°C	V_{CCA} – 0.1			V
		I_{OH} = –1 mA		1.1 V		T_A = –40°C to 85°C	0.88			
		I_{OH} = –2 mA		1.4 V		T_A = –40°C to 85°C	1.05			
		I_{OH} = –3 mA		1.65 V		T_A = –40°C to 85°C	1.2			
		I_{OH} = –6 mA		2.3V		T_A = –40°C to 85°C	1.75			
		I_{OH} = –12 mA		3 V		T_A = –40°C to 85°C	2.3			
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	0.9 V	0.9 V to 3.6 V	T_A = –40°C to 85°C			0.1	V
		I_{OL} = 1 mA		1.1 V		T_A = –40°C to 85°C			0.2	
		I_{OL} = 2 mA		1.4 V		T_A = –40°C to 85°C			0.2	
		I_{OL} = 3 mA		1.65 V		T_A = –40°C to 85°C			0.25	
		I_{OL} = 6 mA		2.3V		T_A = –40°C to 85°C			0.3	
		I_{OL} = 12 mA		3 V		T_A = –40°C to 85°C			0.55	
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V	T_A = 25°C		±0.1	±1	µA
						T_A = –40°C to 85°C			±5	
				0 V to 3.6 V	0 V	T_A = 25°C		±0.1	±1	
						T_A = –40°C to 85°C			±5	
I_{CCA}		V_{CCB} or GND, I_O = 0		0.8 V to 3.6 V	0.8 V to 3.6 V	T_A = –40°C to 85°C			8	µA
				0 V	0 V to 3.6 V	T_A = –40°C to 85°C			8	
				0 V to 3.6 V	0 V	T_A = –40°C to 85°C			8	
I_{CCB}		V_{CCB} or GND, I_O = 0		0.8 V to 3.6 V	0.8 V to 3.6 V	T_A = –40°C to 85°C			8	µA
				0 V	0 V to 3.6 V	T_A = –40°C to 85°C			8	
				0 V to 3.6 V	0 V	T_A = –40°C to 85°C			8	
$I_{CCA} + I_{CCB}$		V_{CCB} or GND, I_O = 0		0.8 V to 3.6 V	0.8 V to 3.6 V	T_A = –40°C to 85°C			16	µA
C_i	V_{CCB}	V_{CCB} = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		22		pF
C_{io}	A or B port	V_{CCA} = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		5		pF
						T_A = –40°C to 85°C			7	

(1) V_{CCI} is the V_{CCB} input port.
(2) V_{CCO} is the V_{CCA} output port.

6.6 Switching Characteristics, V_{CCB} = 1.1 V

over recommended operating free-air temperature range, V_{CCB} = 1.1 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	TYP	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V	5.5	ns
			V_{CCA} = 1.4 V	4.6	
			V_{CCA} = 1.65 V	4.2	
			V_{CCA} = 2.3 V	3.7	
			V_{CCA} = 3 V	3.9	
t_{PHL}	B	A	V_{CCA} = 1.1 V	4.7	ns
			V_{CCA} = 1.4 V	3.9	
			V_{CCA} = 1.65 V	3.4	
			V_{CCA} = 2.3 V	3	
			V_{CCA} = 3 V	3.1	

6.7 Switching Characteristics, V_{CCB} = 1.4 V

over recommended operating free-air temperature range, V_{CCB} = 1.4 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		4.7		ns
			V_{CCA} = 1.4 V	2		5	
			V_{CCA} = 1.65 V	1.5		3.8	
			V_{CCA} = 2.3 V	1.2		3.8	
			V_{CCA} = 3 V	1		3.8	
t_{PHL}	B	A	V_{CCA} = 1.1 V		4.2		ns
			V_{CCA} = 1.4 V	2		5	
			V_{CCA} = 1.65 V	1.5		3.9	
			V_{CCA} = 2.3 V	1.2		3	
			V_{CCA} = 3 V	1		3	

6.8 Switching Characteristics, V_{CCB} = 1.65 V

over recommended operating free-air temperature range, V_{CCB} = 1.65 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		4.3		ns
			V_{CCA} = 1.4 V	2		4.2	
			V_{CCA} = 1.65 V	1.5		4.1	
			V_{CCA} = 2.3 V	1.2		3.8	
			V_{CCA} = 3 V	1		3.7	
t_{PHL}	B	A	V_{CCA} = 1.1 V		2.6		ns
			V_{CCA} = 1.4 V	2		4.2	
			V_{CCA} = 1.65 V	1.5		4.1	
			V_{CCA} = 2.3 V	1.2		3.8	
			V_{CCA} = 3 V	1		3.7	

6.9 Switching Characteristics, V_{CCB} = 2.3 V

over recommended operating free-air temperature range, V_{CCB} = 2.3 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		2.7		ns
			V_{CCA} = 1.4 V	2		3.5	
			V_{CCA} = 1.65 V	1.5		3.1	
			V_{CCA} = 2.3 V	1.2		2.8	
			V_{CCA} = 3 V	0.2		4.1	
t_{PHL}	B	A	V_{CCA} = 1.1 V		2.4		ns
			V_{CCA} = 1.4 V	2		3.7	
			V_{CCA} = 1.65 V	1.5		3.7	
			V_{CCA} = 2.3 V	1.2		2.8	
			V_{CCA} = 3 V	0.2		3.5	

6.10 Switching Characteristics, V_{CCB} = 3 V

over recommended operating free-air temperature range, V_{CCB} = 3 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		3.9		ns
			V_{CCA} = 1.4 V	2		3.8	
			V_{CCA} = 1.65 V	1.5		3.6	
			V_{CCA} = 2.3 V	0.5		3.6	
			V_{CCA} = 3 V	0.2		3.6	
t_{PHL}	B	A	V_{CCA} = 1.1 V		3.9		ns
			V_{CCA} = 1.4 V	2		3.7	
			V_{CCA} = 1.65 V	1.5		3.1	
			V_{CCA} = 2.3 V	0.5		3.5	
			V_{CCA} = 3 V	0.2		3	

6.11 Operating Characteristics

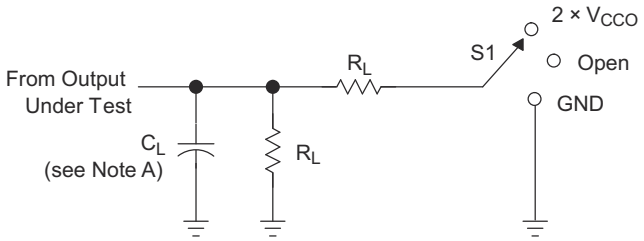
T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}, V_{CCB}	TYP	UNIT
C_{pdA} (1)	B to A	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.1 V	18.5	pF
				V_{CCA} = V_{CCB} = 1.4 V		
				V_{CCA} = V_{CCB} = 1.65 V		
				V_{CCA} = V_{CCB} = 2.3 V		
				V_{CCA} = V_{CCB} = 3 V		

(1) Power dissipation capacitance per transceiver

7 Parameter Measurement Information

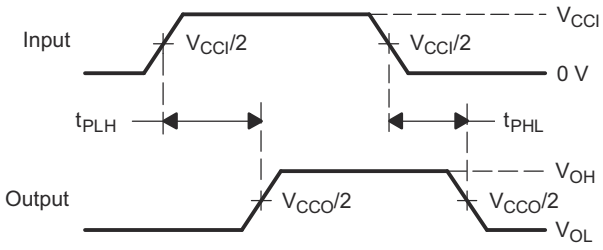
7.1 Load Circuit and Voltage Waveforms



TEST	S1
t_{pd}	Open

LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	30 pF	0.5 kΩ	0.1 V
1.5 V ± 0.1 V	30 pF	0.5 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	0.5 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	0.5 kΩ	0.15 V
3.3 V ± 0.3 V	30 pF	0.5 kΩ	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is V_{CCB}.
F. V_{CCO} is V_{CCA}.

Figure 7-1. Load and Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AVC4T234 is a 4-bit, dual-supply noninverting voltage level translation device. The B input port pins are referenced to the V_{CCB} supply, and the A output port pins are referenced to the V_{CCA}. The B port is able to accept I/O voltages ranging from 0.9 V to 3.6 V.

8.2 Functional Block Diagram

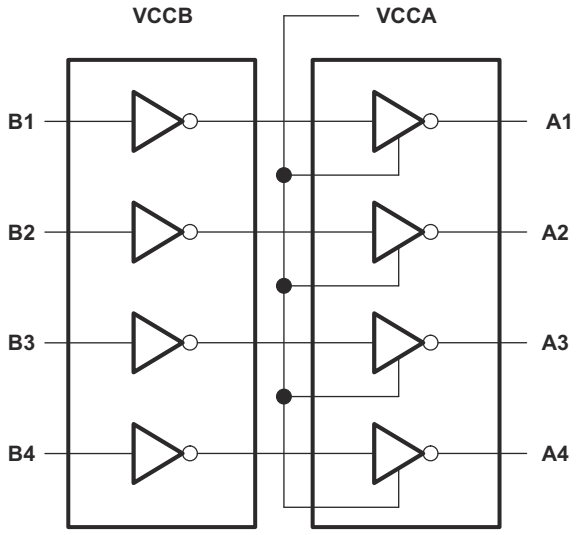


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 0.9-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 0.9 V and 3.6 V; thus, making the device suitable for translating between any of the low voltage nodes (0.9, 1.05 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Supports High Speed Translation

The SN74AVC4T234 device can support high data rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS	OUTPUTS
Bx	Ax
L	L
H (referenced to V_{CCB})	H (referenced to V_{CCA})

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AVC4T234 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T234 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

9.2 Typical Application

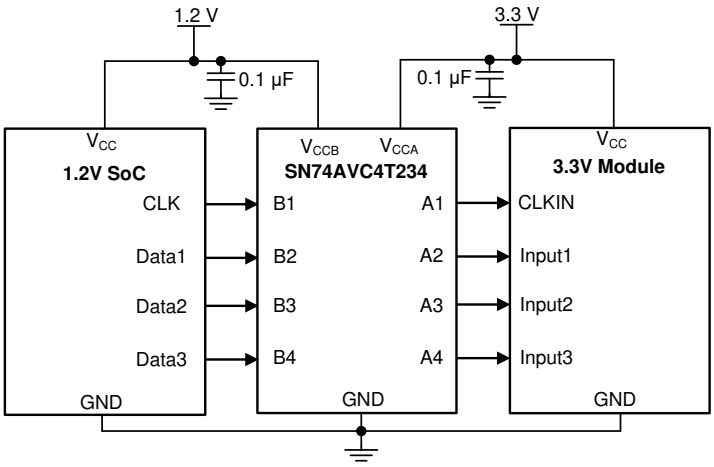


Figure 9-1. Typical Application Diagram

9.2.1 Design Requirements

For the design example shown in *Typical Application,* use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T234 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T234 device is driving to determine the output voltage range.

9.2.3 Application Curves

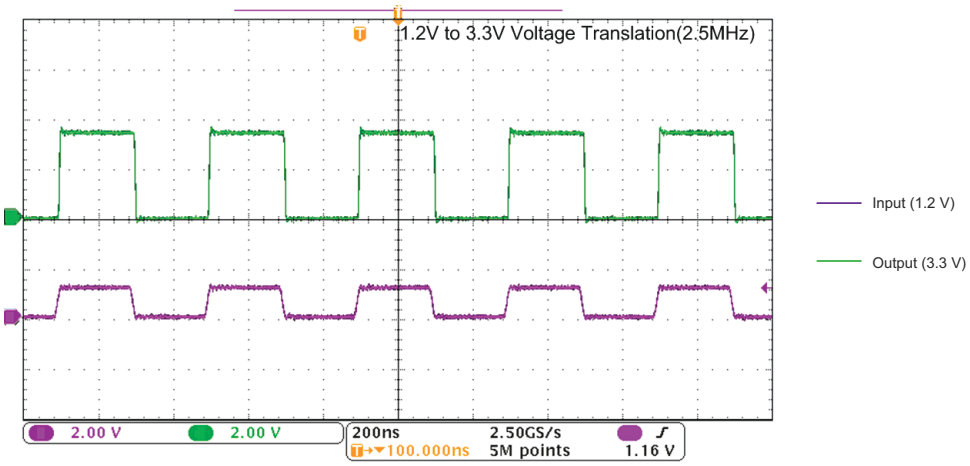


Figure 9-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

The SN74AVC4T234 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V and V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 0.9-V, 1.05-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

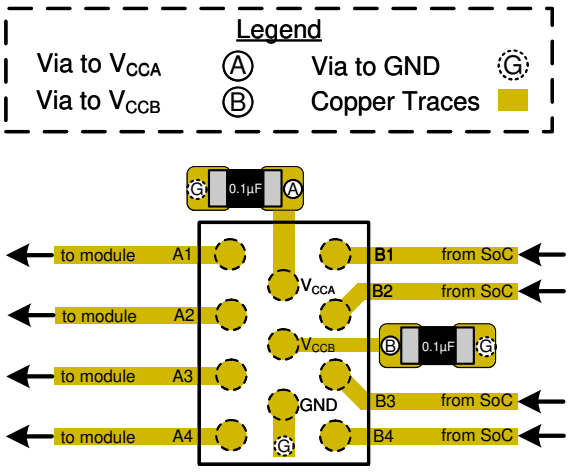
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

11.2 Layout Example



12 Device and Documentation Support

12.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments Incorporated.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AVC4T234ZWAR	Active	Production	NFBGA (ZWA) | 11	2500 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	1G2
SN74AVC4T234ZWAR.B	Active	Production	NFBGA (ZWA) | 11	2500 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	1G2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

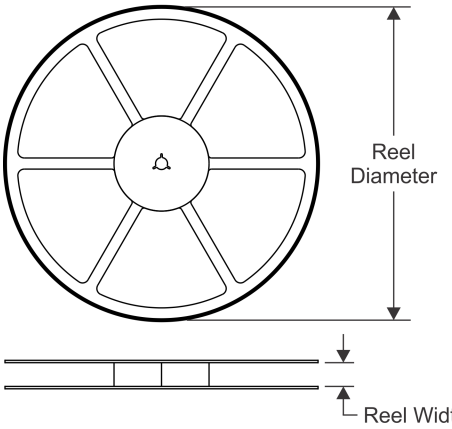
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

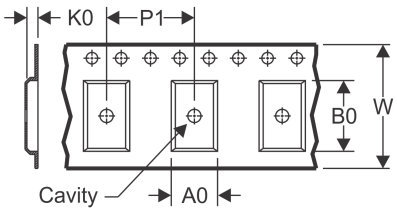
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

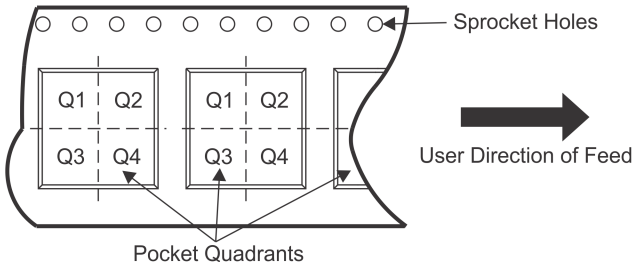


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

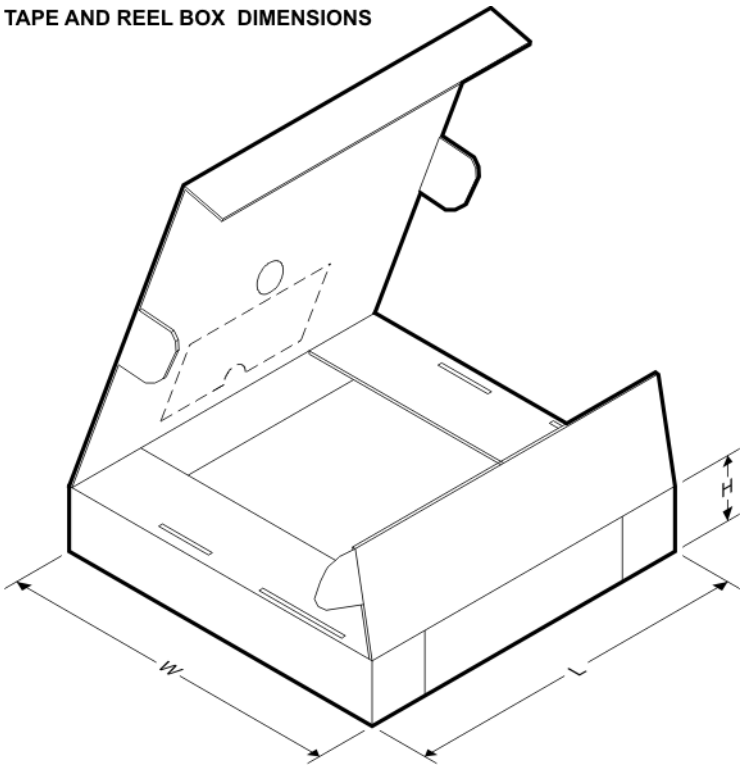
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC4T234ZWAR	NFBGA	ZWA	11	2500	330.0	8.4	1.6	2.2	0.55	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

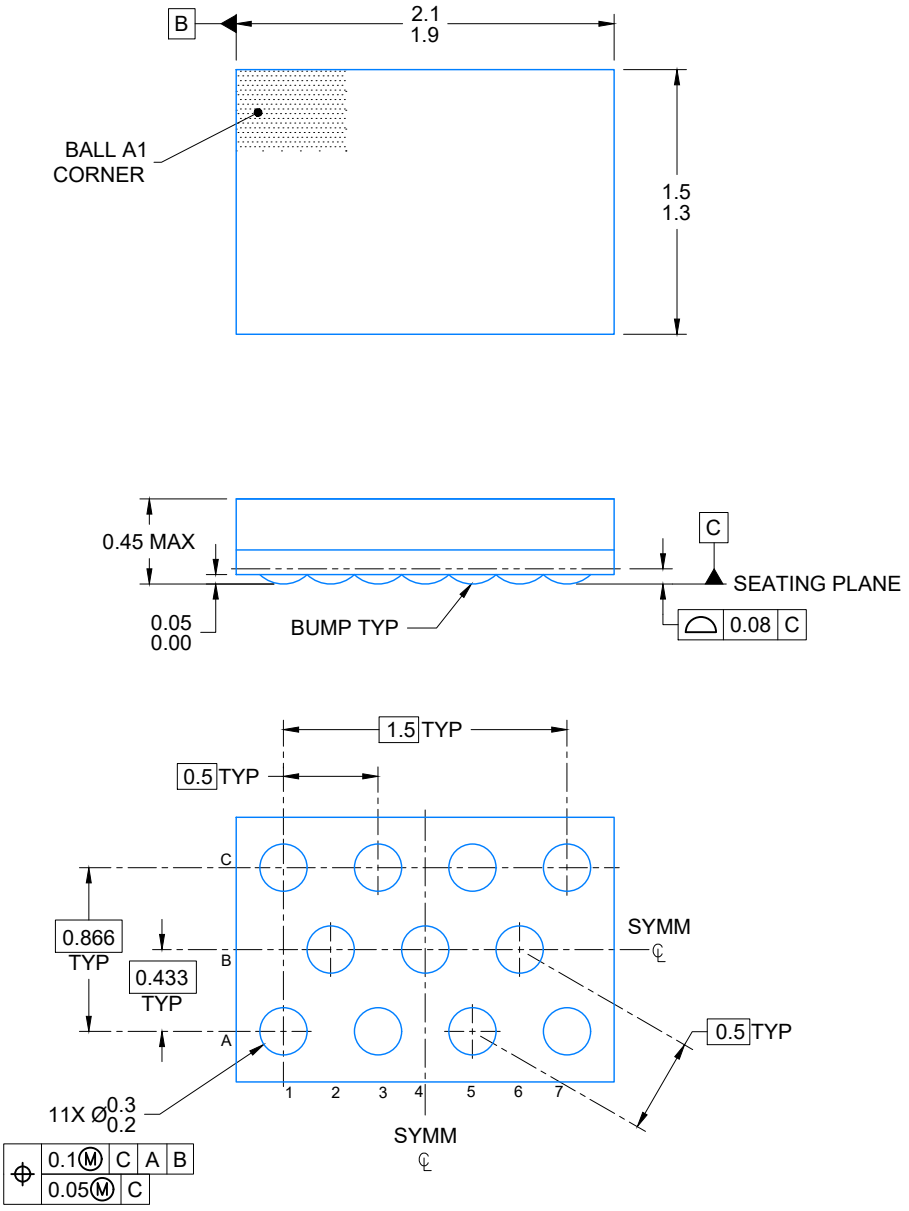
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC4T234ZWAR	NFBGA	ZWA	11	2500	338.1	338.1	20.6

PACKAGE OUTLINE

ZWA0011A

NFBGA - 0.45 mm max height

MICRO CHIP SCALE PACKAGE

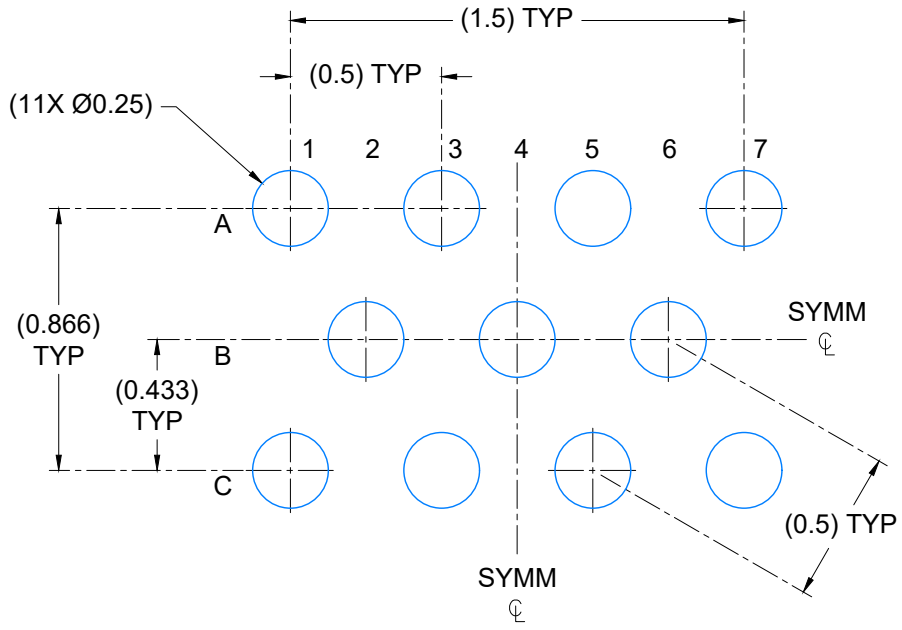


4224717/A 12/2018

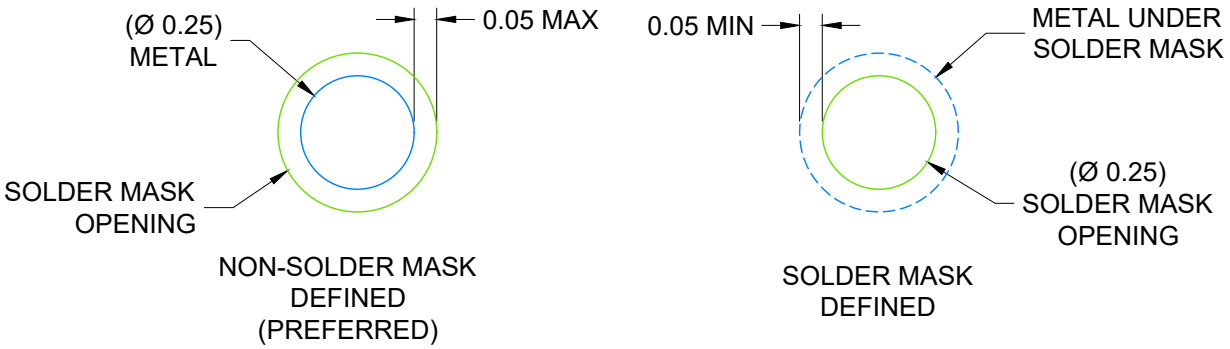
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224717/A 12/2018

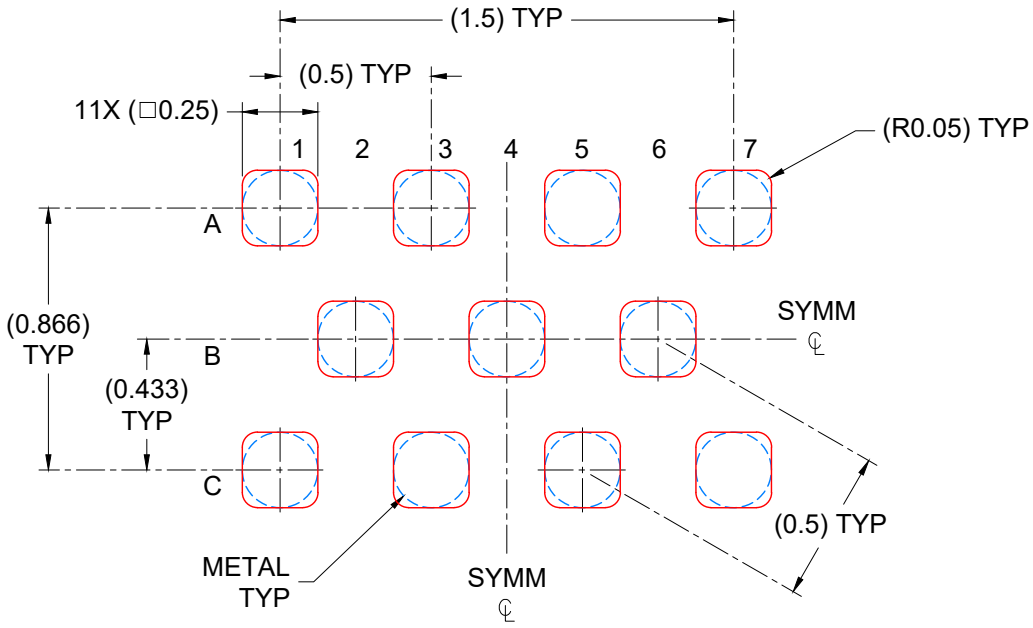
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

NFBGA - 0.45 mm max height

MICRO CHIP SCALE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4224717/A 12/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265