

SN74AVC2T45 2-Bit, Dual Supply, Bus Transceiver with Configurable Level-Shifting and Translation

1 Features

- Available in the Texas Instruments NanoFree™ Package
- V_{CC} Isolation Feature: If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- **Dual Supply Rail Design**
- I/Os Are 4.6V Over Voltage Tolerant
- I_{off} Supports Partial-Power-Down Mode Operation
- Max Data Rates
 - 500Mbps (1.8V to 3.3V)
 - 320Mbps (<1.8V to 3.3V)
 - 320Mbps (Level-Shifting to 2.5V or 1.8V)
 - 280Mbps (Level-Shifting to 1.5V)
 - 240Mbps (Level-Shifting to 1.2V)
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22

2 Applications

- **Smartphones**
- Servers
- Desktop PCs and notebooks
- Other portable devices

3 Description

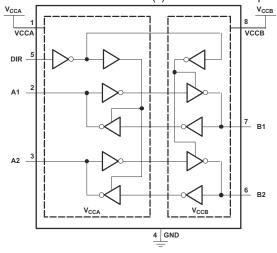
This 2-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The A ports are designed to track V_{CCA} and accepts any supply voltage from 1.2V to 3.6V. The B ports are designed to track V_{CCB} and accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR pin) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess leakage current on the internal CMOS structure.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74AVC2T45DCT	DCT, (SSOP, 8)	2.95mm × 2.80mm
SN74AVC2T45DCU	DCU (VSSOP, 8)	2.30mm × 2.00mm
SN74AVC2T45YZP	YZP (DSBGA, 8)	1.89mm × 0.89mm
SN74AVC2T45DDF	DDF (SOT-23, 8)	2.90mm × 1.60mm

For all available packages, see Section 11. (1)



Pin numbers are for the DCT and DCU packages only.

Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

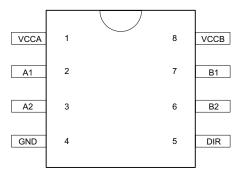


Figure 4-1. DCT or DCU Package 8-Pin SM8 or VSSOP Top View

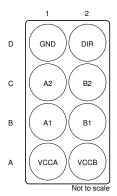


Figure 4-2. YZP Package 8-Pin DSBGA Bottom View

Pin Functions

	PIN			
NAME	VSSOP) (DSBGA)			DESCRIPTION
VCCA	1	A1	_	Supply Voltage A
VCCB	8	A2	_	Supply Voltage B
GND	4	D1	_	Ground
A1	2	B1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA} .
A2	3	C1	I/O	Output or input depending on state of DIR. Output level depends on V _{CCA} .
B1	7	B2	I/O	Output or input depending on state of DIR. Output level depends on V _{CCB} .
B2	6	C2	I/O	Output or input depending on state of DIR. Output level depends on V _{CCB} .
DIR	5	D2	I	Direction Pin, Connect to GND or to VCCA

(1) I = Input; O = Output; I/O = Input or Output



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CCA} V _{CCB}	Supply voltage		-0.5	4.6	V
		IO ports (A port)	-0.5	4.6	
VI	Input voltage ⁽²⁾	IO ports (B port)	-0.5	4.6	V
		Control inputs	-0.5	4.6	
V	Voltage applied to any output in the high-impedance or power-	A port	-0.5	4.6	V
Vo	off state ⁽²⁾	B port	-0.5	4.6	V
V	Valtage applied to any output in the high or law state(2) (3)	A port	-0.5	V _{CCA} + 0.5	V
Vo	Voltage applied to any output in the high or low state ^{(2) (3)}	B port	-0.5	V _{CCB} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		– 50	mA
I _{OK}	Output clamp current	V _O < 0		– 50	mA
Io	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

- The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
- The output positive-voltage rating can be exceeded up to 4.6 V maximum if the output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT	
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000		
V _(ESD)	Electrostatic discharge	trostatic discharge Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾			
		Machine Model (MM), Per JEDEC specification JESD22-A115-A	±200		

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- JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

See(3) (4) (5)

			V _{CCI} ⁽¹⁾	V _{CCO} (2)	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}	Supply voltage				1.2	3.6	V
			1.2V to 1.95V		V _{CCI} ⁽¹⁾ × 0.65		
V_{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.95V to 2.7V		1.6		V
	input voltage		2.7 V to 3.6 V		2		
			1.2V to 1.95V		V	CCI (1) × 0.35	
V_{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.95V to 2.7V			0.7	V
	input voltage		2.7V to 3.6V			0.8	
			1.2V to 1.95V		V _{CCA} × 0.65		
V_{IH}	High-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.95V to 2.7V		1.6		V
	input voltage	(Totoronood to VCCA)	2.7V to 3.6V		2		
			1.2V to 1.95V			V _{CCA} × 0.35	
V_{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.95V to 2.7V			0.7	V
	input voltage	(referenced to veca)	2.7V to 3.6V			0.8	
VI	Input voltage				0	3.6	V
V	Output valtage	Active state			0	V _{CCO} (2)	V
Vo	Output voltage	3-state			0	3.6	V
				1.2V		-3	
				1.4V to 1.6V		-6	
I _{OH}	High-level output	current		1.65V to 1.95V		-8	mA
				2.3V to 2.7V		-9	
				3V to 3.6V		-12	
				1.2V		3	
				1.4V to 1.6V		6	
I_{OL}	Low-level output of	urrent		1.65V to 1.95V		8	mA
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δν	Input transition rise	e or fall rate				5	ns/V
T _A	Operating free-air	temperature			-40	85	°C

⁽¹⁾ V_{CCI} is the voltage associated with the input port supply VCCA or VCCB.

⁽²⁾ V_{CCO} is the voltage associated with the output port supply VCCA or VCCB.

⁽³⁾ All unused data inputs of the device must be held at V_{CCI} or GND to provide proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

⁽⁴⁾ For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.

⁽⁵⁾ For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7V$, V_{IL} max = $V_{CCA} \times 0.3V$.



5.4 Thermal Information

	THERMAL METRIC (1)	DCT (SM8)	DCU (VSSOP)	DDF (SOT-23)	YZP (DSBGA)	UNIT
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183.1	246.9	203.2	105.8	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	101.5	95.2	121.5	1.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	111.0	158.4	99.8	10.8	°C/W
ΨЈТ	Junction-to-top characterization parameter	27.6	34.1	21.4	3.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	109.2	157.5	99.5	10.8	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

DADA	METER	TEST COND	NTIONS	V	V		T _A = 25°C		-40°C to +85°	C	UNIT
PARA	INIETEK	TEST CONL	IIIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	MIN	MAX	UNIT
		I _{OH} = -100μA		1.2V to 3.6V	1.2V to 3.6V				V _{CCO} - 0.2V		
		I _{OH} = -3mA		1.2V	1.2V		0.95				
V _{OH} (3)		I _{OH} = -6mA	V _I = V _{IH}	1.4V	1.4V				1.05		V
VOH (I _{OH} = -8mA	VI – VIH	1.65V	1.65V				1.2		V
		I _{OH} = -9mA		2.3V	2.3V				1.75		
		I _{OH} = -12mA		3V	3V				2.3		
		I _{OL} = 100μA		1.2V to 3.6V	1.2V to 3.6V					0.2	
		I _{OL} = 3mA		1.2V	1.2V		0.25				
V _{OL} (3)		I _{OL} = 6mA	$V_{I} = V_{IL}$	1.4V	1.4V					0.35	V
VOL (I _{OL} = 8mA	V - V L	1.65V	1.65V					0.45	V
		I _{OL} = 9mA		2.3V	2.3V					0.55	
		I _{OL} = 12mA		3V	3V					0.7	
I _I	DIR	V _I = V _{CCA} or GND		1.2V to 3.6V	1.2V to 3.6V		±0.025	±0.25		±1	μA
	A port	V _I or V _O = 0 to 3.6V		0V	0 to 3.6 V		±0.1	±1		±5	
I _{off}	B port	V_1 or $V_0 = 0$ to 3.6	O V	0 to 3.6V	0V		±0.1	±1		±5	μA
I _{OZ} (3)	B port	V _O = V _{CCO} or GNI	Ο,	0V	3.6V		±0.5	±2.5		±5	μA
IOZ (A port	$V_I = V_{CCI}$ or GND		3.6V	0V		±0.5	±2.5		±5	μА
				1.2V to 3.6V	1.2V to 3.6V					10	
I _{CCA} (3)		$V_I = V_{CCI}$ or GND,	I _O = 0	0V	3.6V					-2	μΑ
				3.6V	0V					10	
				1.2V to 3.6V	1.2V to 3.6V					10	
I _{CCB} (3)		$V_I = V_{CCI}$ or GND,	$I_O = 0$	0V	3.6V					10	μA
				3.6V	0V					-2	
I _{CCA} + I _{cca} (see Tal		V _I = V _{CCI} or GND,	I _O = 0	1.2V to 3.6V	1.2V to 3.6V					20	μA
Cı	Control inputs	V _I = 3.3V or GND		3.3V	3.3V		2.5				pF
C _{io}	A or B port	V _O = 3.3V or GNE)	3.3V	3.3V		6				pF

 V_{CCO} is the voltage associated with the output port supply VCCA or VCCB. (1)

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⁽²⁾

 V_{CCI} is the voltage associated with the input port supply VCCA or VCCB. V_{OH} : Output High Voltage; V_{OL} : Output Low Voltage; I_{OZ} : Hi-Z Output Current; I_{CCA} : Supply A Current; I_{CCB} : Supply B Current

5.6 Switching Characteristics: V_{CCA} = 1.2V

over recommended operating free-air temperature range, V_{CCA} = 1.2V (see Figure 6-1)

PARAMETER	FROM	то	V _{CCB} = 1.2V	V _{CCB} = 1.5V	V _{CCB} = 1.8V	V _{CCB} = 2.5V	V _{CCB} = 3.3V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	TYP	TYP	TYP	TYP	TYP	ONIT
t _{PLH} (2)	А	В	3.1	2.6	2.4	2.2	2.2	ns
t _{PHL} (2)	A	ь	3.1	2.6	2.4	2.2	2.2	115
t _{PLH} (2)	В	А	3.4	3.1	3	2.9	2.9	20
t _{PHL} (2)	Б	A	3.4	3.1	3	2.9	2.9	ns
t _{PHZ} (2)	DIR	А	5.2	5.2	5.1	5	4.8	ns
t _{PLZ} (2)	DIK	A	5.2	5.2	5.1	5	4.8	115
t _{PHZ} ⁽²⁾	DIR	В	5	4	3.8	2.8	3.2	ns
t _{PLZ} (2)	DIK	ь	5	4	3.8	2.8	3.2	115
t _{PZH} ⁽²⁾ ⁽¹⁾	DIR	А	8.4	7.1	6.8	5.7	6.1	ns
t _{PZL} ^{(2) (1)}	DIK	A	8.4	7.1	6.8	5.7	6.1	115
t _{PZH} ⁽²⁾ ⁽¹⁾	DIR	В	8.3	7.8	7.5	7.2	7	ns
t _{PZL} ⁽²⁾ ⁽¹⁾	אוט	ם	8.3	7.8	7.5	7.2	7	115

- (1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.
- (2) t_{PLH}: Low-to-high Propagation Delay; t_{PHZ}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PZL}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

5.7 Switching Characteristics: V_{CCA} = 1.5V ±0.1V

over recommended operating free-air temperature range, $V_{CCA} = 1.5V \pm 0.1V$ (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V		V _{CCB} = 1.8V ± 0.15V		V _{CCB} = 2.5V ± 0.2V		V _{CCB} = 3.3V ± 0.3V		UNIT				
	(IIVFO1)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
t _{PLH} ⁽²⁾	Α	В	2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	ns			
t _{PHL} ⁽²⁾		Б	2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	115			
t _{PLH} ⁽²⁾	В	Α	2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	ns			
t _{PHL} ⁽²⁾	Б	Α	2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	115			
t _{PHZ} ⁽²⁾	DIR	Α	3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	no			
t _{PLZ} (2)	אוט	A	3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	ns			
t _{PHZ} ⁽²⁾	DIR	В	4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	no			
t _{PLZ} (2)	אוט	Б	4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	ns			
t _{PZH} ⁽²⁾ ⁽¹⁾	NID	۸	7.4		12.4		12.1		11.8		11.8	ns			
t _{PZL} ⁽²⁾ ⁽¹⁾	DIR	DIR A	7.4		12.4		12.1		11.8		11.8	115			
t _{PZH} ⁽²⁾ ⁽¹⁾	DIB	В	6.7		13.9	-	12.4		11.4		11.1	no			
t _{PZL} ⁽²⁾ ⁽¹⁾	DIR	DIR	DIR	DIR	В	6.7		13.9		12.4		11.4		11.1	ns

- (1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.
- (2) t_{PLH}: Low-to-high Propagation Delay; t_{PHZ}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay

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5.8 Switching Characteristics: V_{CCA} = 1.8V ±0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO V _{CCB} = 1.2V		V _{CCB} = ± 0.		V _{CCB} = 1.8V ± 0.15V		V _{CCB} = 2.5V ± 0.2V		V _{CCB} = 3.3V ± 0.3V		UNIT
		(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH} (2)	А	В	2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	ns
t _{PHL} (2)	Α	Б	2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	115
t _{PLH} ⁽²⁾	В	А	2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	ns
t _{PHL} ⁽²⁾	Б	^	2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	115
t _{PHZ} ⁽²⁾	DIR	А	3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	no
t _{PLZ} (2)	אוט	A	3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	ns
t _{PHZ} ⁽²⁾	DIR	В	4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	ns
t _{PLZ} (2)	DIK	Б	4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	115
t _{PZH} ⁽²⁾ ⁽¹⁾	DIR	А	6.8		10.5		10.3		9.7		9.7	ns
t _{PZL} ^{(2) (1)}	DIR	^	6.8		10.5		10.3		9.7		9.7	115
t _{PZH} ⁽²⁾ ⁽¹⁾	DIR	В	6.4		13.3		11.2		8.7		8.3	no
t _{PZL} ⁽²⁾ ⁽¹⁾	אוט	D	6.4		13.3		11.2		8.7		8.3	ns

- (1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.
- (2) t_{PLH}: Low-to-high Propagation Delay; t_{PLZ}: High-to-Low Propagation Delay; t_{PLZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PLZ}: Hi-Z-to-High Propagation Delay; t_{PLZ}: Hi-Z-to-Low Propagation Delay

5.9 Switching Characteristics: V_{CCA} = 2.5V ±0.2V

over recommended operating free-air temperature range, $V_{CCA} = 2.5V \pm 0.2V$ (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = ± 0.		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT					
		(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX						
t _{PLH} ⁽²⁾	Α	В	2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	ns					
t _{PHL} ⁽²⁾	A	ь	2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	115					
t _{PLH} (2)	В	Α	2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	no					
t _{PHL} ⁽²⁾	Б	A	2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	ns					
t _{PHZ} ⁽²⁾	DIR	А	2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	no					
t _{PLZ} (2)	אוט	A	2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	ns					
t _{PHZ} ⁽²⁾	DIR	D	3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	no					
t _{PLZ} (2)	אוט	В	В	В	В	В	В	3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	ns
t _{PZH} ⁽²⁾ ⁽¹⁾	DIB	Α	5.9		8.5		7.7		7.2		6.9	no					
t _{PZL} ^{(2) (1)}	DIR	DIR	A	5.9		8.5		7.7		7.2		6.9	ns				
t _{PZH} ⁽²⁾ ⁽¹⁾	DIR	В	5		12.8		10.4		8		6.9	ne					
t _{PZL} ⁽²⁾ ⁽¹⁾	אוט	O O	5		12.8		10.4		8		6.9	ns					

- (1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.
- (2) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PZ}: Low-to-Hi-Z Propagation Delay; t_{PZ}: Hi-Z-to-Low Propagation Delay

Product Folder Links: SN74AVC2T45

5.10 Switching Characteristics: V_{CCA} = 3.3V ±0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = ± 0.		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT
	(INFOT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH} (2)	Α	В	2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	ns
t _{PHL} ⁽²⁾		ь	2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	115
t _{PLH} (2)	В	А	2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	ns
t _{PHL} (2)	ь	^	2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	115
t _{PHZ} ⁽²⁾	DIR	А	2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	ns
t _{PLZ} (2)	אוט	A	2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	115
t _{PHZ} (2)	DIR	В	3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	ns
t _{PLZ} (2)	DIK	ь	3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	115
t _{PZH} ⁽²⁾ ⁽¹⁾	DIR	А	5.5		10.2		8.7		7.2		6.6	ns
t _{PZL} ⁽²⁾ ⁽¹⁾	DIK	^	5.5		10.2		8.7		7.2		6.6	115
t _{PZH} ^{(2) (1)}	DIR	В	5.4		12.7	-	10.3		7.5		6.4	no
t _{PZL} ⁽²⁾ ⁽¹⁾	אוע	D	5.4		12.7		10.3		7.5		6.4	ns

- (1) The enable time is a calculated value, derived using the formula shown in the section.
- (2) t_{PLH}: Low-to-high Propagation Delay; t_{PLZ}: High-to-Low Propagation Delay; t_{PLZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PLZ}: Hi-Z-to-Low Propagation Delay

5.11 Operating Characteristics

 $T_{\Lambda} = 25^{\circ}C$

P	ARAMETER	TEST CONDITIONS	V _{CCA} = V _{CCB} = 1.2V	V _{CCA} = V _{CCB} = 1.5V	$V_{CCA} = V_{CCB} = 1.8V$	V _{CCA} = V _{CCB} = 2.5V	V _{CCA} = V _{CCB} = 3.3V	UNIT
		CONDITIONS	TYP	TYP	TYP	TYP	TYP	
C (1)	A-port input, B-port output	C _L = 0, f = 10MHz,	3	3	3	3	4	pF
C _{pdA} (1)	B-port input, A-port output	$t_r^{(2)} = t_f^{(2)} = 1$ ns	12	13	13	14	15	ρi
C (1)	A-port input, B-port output	C _L = 0, f = 10MHz,	12	13	13	14	15	, F
C _{pdB} (1)	B-port input, A-port output	$t_r^{(2)} = t_f^{(2)} = 1$ ns	3	3	3	3	4	pF

- (1) Power-dissipation capacitance per transceiver
- (2) t_r: Rise time; t_f: Fall time



5.12 Typical Characteristics

Table 5-1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

	· · · · J					007 00		
V	V _{CCA}							
V _{CCB}	0V	1.2V	1.5V	1.8V	2.5V	3.3V	UNIT	
0V	0	<0.5	<0.5	<0.5	<0.5	<0.5		
1.2V	<0.5	<1	<1	<1	<1	1		
1.5V	<0.5	<1	<1	<1	<1	1		
1.8V	<0.5	<1	<1	<1	<1	<1	μA	
2.5V	<0.5	1	<1	<1	<1	<1		
3.3V	<0.5	1	<1	<1	<1	<1		

5.12.1 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.2V

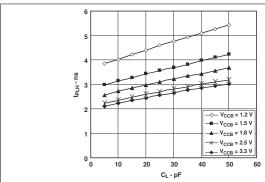


Figure 5-1. Typical A-to-B Propagation Delay, Low to High

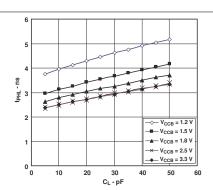


Figure 5-2. Typical A-to-B Propagation Delay, High to Low

5.12.2 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.5V

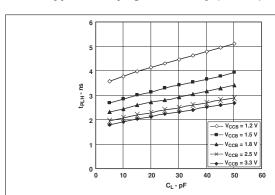


Figure 5-3. Typical A-to-B Propagation Delay, Low to High

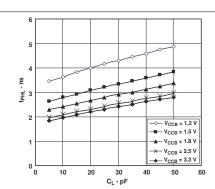


Figure 5-4. Typical A-to-B Propagation Delay, High to Low

5.12.3 Typical Propagation Delay (A-to-B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.8V

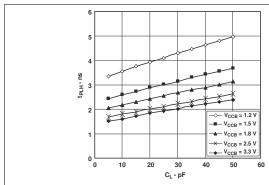


Figure 5-5. Typical A-to-B Propagation Delay, Low to High

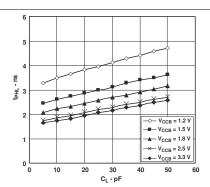


Figure 5-6. Typical A-to-B Propagation Delay, High to Low

5.12.4 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 2.5V

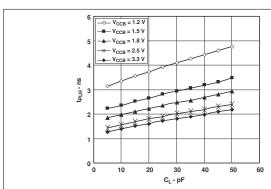


Figure 5-7. Typical A-to-B Propagation Delay, Low to High

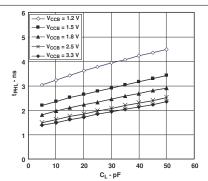


Figure 5-8. Typical A-to-B Propagation Delay, High to Low

5.12.5 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A = 25$ °C, $V_{CCA} = 3.3$ V

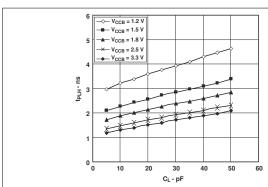


Figure 5-9. Typical A-to-B Propagation Delay, Low to High

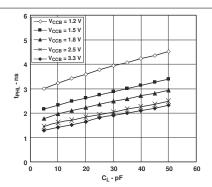
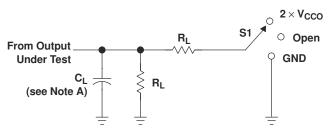


Figure 5-10. Typical A-to-B Propagation Delay, High to Low



VCCA

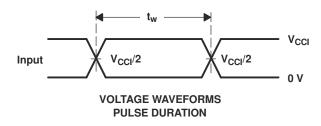
6 Parameter Measurement Information

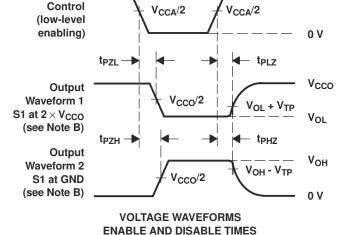


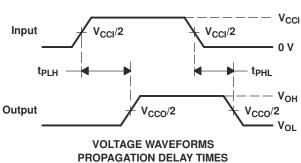
TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	$2 \times V_{CCO}$
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V _{CCO}	CL	R _L	V _{TP}
1.2 V	15 pF	2 k Ω	0.1 V
1.5 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V







NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

Output

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq$ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

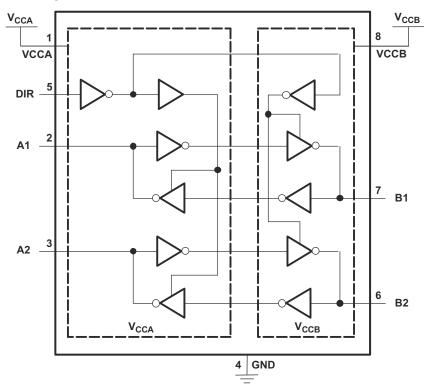
The device is designed so that the DIR input is powered by supply voltage from VCCA.

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

The V_{CC} isolation feature makes sure that if either VCC input is at GND, both ports are put in a high-impedance state. This action prevents a false high or low logic being presented at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

7.2 Functional Block Diagram



Pin numbers are for the DCT and DCU packages only.

7.3 Feature Description

7.3.1 VCC Isolation

The V_{CC} isolation feature make sure that if either V_{CCA} or V_{CCB} are at GND, both ports are in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This action prevents false logic levels from being presented to either bus.

7.3.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range.

7.3.3 IO Ports are 4.6-V Tolerant

The IO ports are up to 4.6 V tolerant.

7.3.4 Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when the device is powered down.

7.4 Device Functional Modes

Table 7-1 shows the functional modes of the SN74AVC2T45-Q1.

Table 7-1. Function Table (Each Transceiver)

INPUT DIR	OPERATION
L	B data to A bus
Н	A data to B bus

Product Folder Links: SN74AVC2T45

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

Figure 8-1 is an example circuit of the SN74AVC2T45 used in a unidirectional logic level-shifting application.

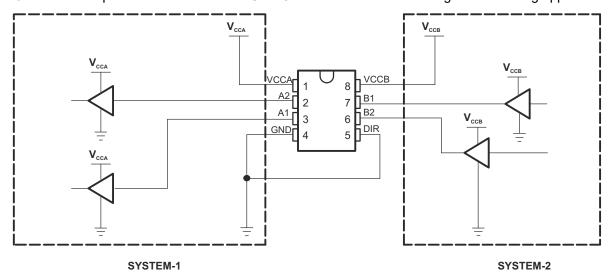


Figure 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

Table 8-1 lists the pins and pin descriptions of the SN74AVC2T45 connections with SYSTEM-1 and SYSTEM-2.

Table 8-1. SN74AVC2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	DESCRIPTION
1	VCCA	SYSTEM-1 supply voltage (1.2V to 3.6V)
2	A1	Output level depends on V _{CCA} .
3	A2	Output level depends on V _{CCA} .
4	GND	Device GND
5	DIR	The GND (low-level) determines B-port to A-port direction.
6	B2	Input threshold value depends on V _{CCB} .
7	B1	Input threshold value depends on V _{CCB} .
8	VCCB	SYSTEM-2 supply voltage (1.2V to 3.6V)

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8.2.1.2 Detailed Design Procedure

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground.

8.2.1.3 Application Curve

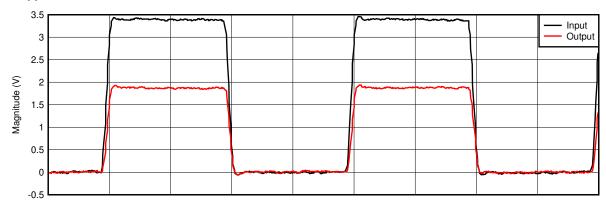


Figure 8-2. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave

8.2.2 Bidirectional Logic Level-Shifting Application

Figure 8-3 shows the SN74AVC2T45 used in a bidirectional logic level-shifting application.

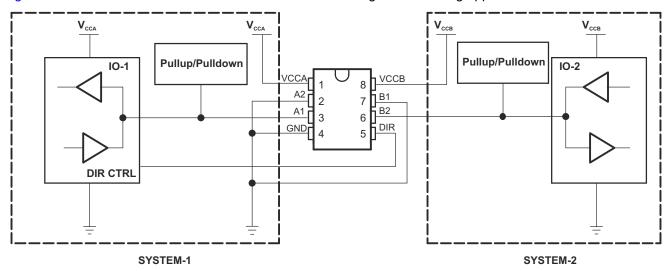


Figure 8-3. Bidirectional Logic Level-Shifting Application

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8.2.2.1 Design Requirements

The SN74AVC2T45 does not have an output-enable (OE) pin, the system designer must take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

8.2.2.2 Detailed Design Procedure

Table 8-2 shows a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Tak	ole 8-2.	Data	Transmi	ission	Sequence	

STATE	DIR CTRL	IO-1	IO-2	DESCRIPTION
1	Н	Output	Input	SYSTEM-1 data to SYSTEM-2
2	Н	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
3	L	Hi-Z	Hi-Z	DIR bit is flipped. IO-1 and IO-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
4	L	Input	Output	SYSTEM-2 data to SYSTEM-1

⁽¹⁾ SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2.1 Enable Times

Calculate the enable times for the SN74AVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting the device with an input. After the B port has been disabled, an input signal applied to the port appears on the corresponding A port after the specified propagation delay.

8.3 Power Supply Recommendations

A proper power-up sequence must always be followed to avoid excessive current on the supply pin, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

- 1. Connect ground before any supply voltage is applied.
- 2. Power up V_{CCA}.
- 3. V_{CCB} can be ramped up along with or after V_{CCA} .

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8.4 Layout

8.4.1 Layout Guidelines

To verify the reliability of the device, follow common printed-circuit board layout guidelines.

- Bypass capacitors can be used on power supplies. Place the capacitors as close as possible to the VCCA,
 VCCB pin and GND pin.
- Short trace lengths can be used to avoid excessive loading.

8.4.2 Layout Example

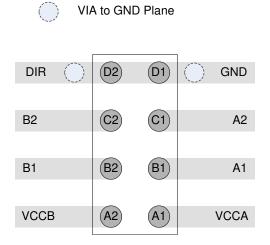


Figure 8-4. Layout Example for YZP Package

Product Folder Links: SN74AVC2T45

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

· Texas Instruments, Implications of Slow or Floating CMOS Inputs

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	hanges from Revision M (September 2024) to Revision N (February 2025)	Page
•	Updated DCT and DDF Thermal Information	6

Cha	anges from Revision L (May 2017) to Revision M (September 2024)	Page
• (Updated the numbering format for tables, figures, and cross-references throughout the document	1
• /	Added DDF package	1
• [Deleted the Community Resources section	19
• /	Added the Support Resources, Receiving Notification of Documentation Updates, Electrostatic Dischart Statement, and Glossary sections	ge

Product Folder Links: SN74AVC2T45



Changes from Revision K (April 2015) to Revision L (May 2017)	Page
Changed data sheet title	1
Changed YZP package pinout diagram to bottom view	
Added Type column to Pin Functions table	3
Added Junction temperature, T _J	
Observed from Decision 17 has 0007) to Decision 17 (April 0045)	
Changes from Revision J (June 2007) to Revision K (April 2015)	Page

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74AVC2T45

www.ti.com

31-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AVC2T45DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTR.A	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTRE4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTRG4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT2 Z
SN74AVC2T45DCTRG4.A	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT2 Z
SN74AVC2T45DCTRG4.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT2 Z
SN74AVC2T45DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCTT.B	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z
SN74AVC2T45DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ
SN74AVC2T45DCUR.A	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ
SN74AVC2T45DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ
SN74AVC2T45DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCURG4.A	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUTG4	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DCUTG4.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R
SN74AVC2T45DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A2T45

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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN744VC2T45DDER 4	Activo	Production	SOT-23-THIN (DDE) I 8	3000 LLAPGE T&P	Voc	SN	Level-1-260C-LINILIM	-40 to 125	A2T45

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AVC2T45DDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A2T45
SN74AVC2T45YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TDN
SN74AVC2T45YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TDN

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AVC2T45:

Automotive: SN74AVC2T45-Q1

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	-
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T45DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTRG4	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4.0	8.0	Q3
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T45DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AVC2T45DCTRG4	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AVC2T45DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74AVC2T45DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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