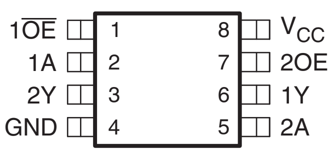
LOW-POWER DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

Check for Samples: SN74AUP2G241

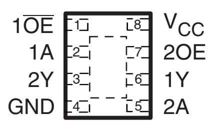
FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 μA Maximum)**
- **Low Dynamic-Power Consumption (C_{pd} = 4.2 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typical)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 9.9 ns Maximum at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

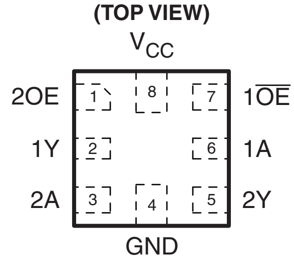
DCU PACKAGE (TOP VIEW)



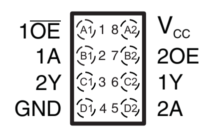
DQE PACKAGE (TOP VIEW)



RSE PACKAGE (TOP VIEW)



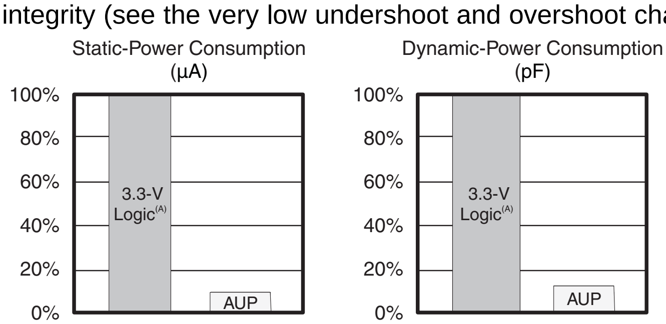
YFP PACKAGE (TOP VIEW)



See mechanical drawings for dimensions.

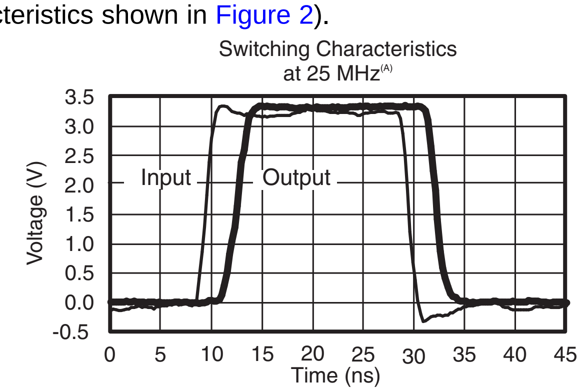
DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).



(A) Single, dual, and triple gates

Figure 1. AUP – The Lowest-Power Family



(A) SN74AUP2Gxx data at C_L = 15 pF.

Figure 2. Excellent Signal Integrity

The SN74AUP2G241 is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G241YFPR	_ _ H Q _
	uQFN – DQE	Reel of 5000	SN74AUP2G241DQER	HQ
	QFN – RSE	Reel of 5000	SN74AUP2G241RSER	HQ
	SSOP – DCU	Reel of 3000	SN74AUP2G241DCUR	H41_

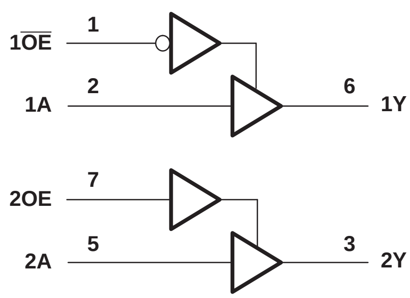
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for DCU and DQE packages.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DCU package		220	°C/W
		DQE package		261	
		RSE package		253	
		YFP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = –40°C to 85°C MIN	T_A = –40°C to 85°C MAX	UNIT
V_{OH}	I_{OH} = –20 μA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
	I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
	I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
	I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
	I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
	I_{OH} = –3.1 mA		1.9			1.85		
	I_{OH} = –2.7 mA	3 V	2.72			2.67		
	I_{OH} = –4 mA		2.6			2.55		
V_{OL}	I_{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
	I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
	I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
	I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
	I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
	I_{OL} = 3.1 mA				0.44		0.45	
	I_{OL} = 2.7 mA	3 V			0.31		0.33	
	I_{OL} = 4 mA				0.44		0.45	
I_I A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}	V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{CC}	V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}	V_I = V_{CC} – 0.6 V[(1)], I_O = 0	3.3 V			40		50	μA
C_i	V_I = V_{CC} or GND	0 V		1.5				pF
		3.6 V		1.5				
C_o	V_O = GND	0 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	TYP	MAX	T_A = –40°C to 85°C MIN	MAX	UNIT
t_{pd}	A	Y	0.8 V		19.2				ns
			1.2 V ± 0.1 V	0.5	7.5	17.9	0.5	18.7	
			1.5 V ± 0.1 V	0.6	5.2	10.8	0.5	12.4	
			1.8 V ± 0.15 V	0.8	4.1	8.1	0.5	9.7	
			2.5 V ± 0.2 V	1.1	2.9	5	0.5	6.5	
			3.3 V ± 0.3 V	0.5	3	9.5	0.5	9.9	
t_{en}	$\overline{OE}$	Y	0.8 V		32.5				ns
			1.2 V ± 0.1 V	0.5	8.5	21.7	0.5	23.1	
			1.5 V ± 0.1 V	0.7	5.5	11.6	0.5	14.2	
			1.8 V ± 0.15 V	1.0	4.3	8.6	0.5	11.1	
			2.5 V ± 0.2 V	1.3	3.0	5.4	0.5	7.6	
			3.3 V ± 0.3 V	1.3	2.4	4.0	0.5	5.8	
t_{dis}	$\overline{OE}$	Y	0.8 V		13.0				ns
			1.2 V ± 0.1 V	1.8	5.0	9.8	1.5	10.2	
			1.5 V ± 0.1 V	0.5	3.6	7.3	0.5	7.6	
			1.8 V ± 0.15 V	0.5	3.3	5.9	0.5	6.3	
			2.5 V ± 0.2 V	0.5	2.2	3.7	0.5	4.1	
			3.3 V ± 0.3 V	1.5	2.6	4.3	1.1	4.6	
t_{en}	OE	Y	0.8 V		19.6				ns
			1.2 V ± 0.1 V	0.5	8.4	20.8	0.5	21.8	
			1.5 V ± 0.1 V	0.5	5.6	11.8	0.5	13.7	
			1.8 V ± 0.15 V	0.7	4.3	8.8	0.5	10.6	
			2.5 V ± 0.2 V	0.9	2.9	5.4	0.5	7	
			3.3 V ± 0.3 V	0.5	2.8	8.8	0.5	9.3	
t_{dis}	OE	Y	0.8 V		12.1				ns
			1.2 V ± 0.1 V	0.6	5.2	10.9	0.5	11.1	
			1.5 V ± 0.1 V	1.1	3.8	7	0.9	7.1	
			1.8 V ± 0.15 V	1.9	3.5	5.6	1.6	5.8	
			2.5 V ± 0.2 V	0.9	2.5	3.9	0.8	4.2	
			3.3 V ± 0.3 V	0.5	3.5	9.3	0.5	9.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		23				ns
			1.2 V ± 0.1 V	0.5	8.7	20.6	0.5	21.3	
			1.5 V ± 0.1 V	1.2	6	12.2	0.5	13.7	
			1.8 V ± 0.15 V	1.4	4.8	9.2	0.5	10.8	
			2.5 V ± 0.2 V	1.5	3.4	5.8	0.5	7.2	
			3.3 V ± 0.3 V	0.5	3.4	8.9	0.5	9.4	
t_{en}	$\overline{OE}$	Y	0.8 V		35.7				ns
			1.2 V ± 0.1 V	0.5	9.6	23.8	0.5	25.1	
			1.5 V ± 0.1 V	1.5	6.4	12.9	0.5	15.5	
			1.8 V ± 0.15 V	1.5	5.0	9.8	0.5	12.2	
			2.5 V ± 0.2 V	1.6	3.5	9.6	0.5	12.3	
			3.3 V ± 0.3 V	1.6	2.9	4.7	0.5	6.4	
t_{dis}	$\overline{OE}$	Y	0.8 V		14.5				ns
			1.2 V ± 0.1 V	0.9	5.8	11.2	0.8	11.5	
			1.5 V ± 0.1 V	0.5	4.1	9.0	0.5	9.2	
			1.8 V ± 0.15 V	1.3	4.4	7.5	1.1	7.8	
			2.5 V ± 0.2 V	1.2	2.9	4.7	1.0	5.0	
			3.3 V ± 0.3 V	1.9	3.8	6.1	1.7	6.3	
t_{en}	OE	Y	0.8 V		21.9				ns
			1.2 V ± 0.1 V	0.5	9.7	23.1	0.5	24	
			1.5 V ± 0.1 V	1	6.4	13.2	0.5	15	
			1.8 V ± 0.15 V	1	5	9.9	0.5	11.7	
			2.5 V ± 0.2 V	1.2	3.4	10.4	0.5	12	
			3.3 V ± 0.3 V	0.5	3.2	8.1	0.5	8.7	
t_{dis}	OE	Y	0.8 V		13.4				ns
			1.2 V ± 0.1 V	0.8	6.2	12.6	0.6	12.7	
			1.5 V ± 0.1 V	2.1	4.6	7.9	1.9	8.1	
			1.8 V ± 0.15 V	1.7	4.7	8.2	1.5	8.3	
			2.5 V ± 0.2 V	1	3.3	5.1	0.9	5.3	
			3.3 V ± 0.3 V	1.2	4.5	7.8	1.1	7.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	TYP	MAX	T_A = –40°C to 85°C MIN	MAX	UNIT
t_{pd}	A	Y	0.8 V		26.2				ns
			1.2 V ± 0.1 V	0.5	9.7	22.7	0.5	23.4	
			1.5 V ± 0.1 V	1.7	4.6	13.6	0.5	15	
			1.8 V ± 0.15 V	1.7	5.4	10.2	0.5	11.7	
			2.5 V ± 0.2 V	1.7	3.9	6.5	0.5	7.9	
			3.3 V ± 0.3 V	0.5	3.7	8.4	0.5	8.9	
t_{en}	$\overline{OE}$	Y	0.8 V		38.9				ns
			1.2 V ± 0.1 V	0.5	10.7	24.7	0.5	26.0	
			1.5 V ± 0.1 V	1.7	7.2	14.1	0.5	16.5	
			1.8 V ± 0.15 V	2.0	5.6	10.3	0.5	12.7	
			2.5 V ± 0.2 V	2.0	4.0	6.8	0.5	8.9	
			3.3 V ± 0.3 V	1.9	3.3	5.2	0.5	6.8	
t_{dis}	$\overline{OE}$	Y	0.8 V		14.8				ns
			1.2 V ± 0.1 V	0.5	6.3	13.7	0.5	14.0	
			1.5 V ± 0.1 V	0.5	4.6	8.8	0.5	9.1	
			1.8 V ± 0.15 V	0.7	4.9	8.1	0.6	8.4	
			2.5 V ± 0.2 V	1.1	3.7	6.5	1.0	6.7	
			3.3 V ± 0.3 V	1.3	4.8	7.6	1.2	7.7	
t_{en}	OE	Y	0.8 V		23				ns
			1.2 V ± 0.1 V	0.5	10.5	24.8	0.5	25.6	
			1.5 V ± 0.1 V	1.5	7.1	14.3	0.5	16	
			1.8 V ± 0.15 V	1.4	5.6	10.8	0.5	12.4	
			2.5 V ± 0.2 V	1.6	3.9	6.8	0.5	8.3	
			3.3 V ± 0.3 V	0.5	3.6	7.6	0.5	8.3	
t_{dis}	OE	Y	0.8 V		13.6				ns
			1.2 V ± 0.1 V	1.1	6.5	12.7	1	12.8	
			1.5 V ± 0.1 V	0.5	4.8	9.1	0.5	9.2	
			1.8 V ± 0.15 V	1.8	5.4	9.2	1.7	9.3	
			2.5 V ± 0.2 V	1.6	3.7	5.5	1.5	5.7	
			3.3 V ± 0.3 V	2.8	5.3	7.9	2.7	7.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

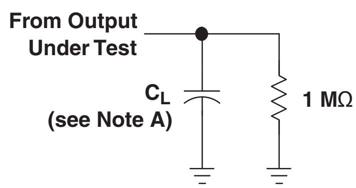
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		36.4				ns
			1.2 V ± 0.1 V	0.5	13	30.8	0.5	31.2	
			1.5 V ± 0.1 V	2.7	9.1	18	1.1	19.1	
			1.8 V ± 0.15 V	2.6	7.2	13.6	1	14.8	
			2.5 V ± 0.2 V	2.6	5.3	8.6	1.3	9.9	
			3.3 V ± 0.3 V	1.4	4.8	7.9	0.7	8.6	
t_{en}	$\overline{OE}$	Y	0.8 V		49.9				ns
			1.2 V ± 0.1 V	0.5	14.1	31.7	0.5	32.8	
			1.5 V ± 0.1 V	2.7	9.6	17.8	0.6	20.0	
			1.8 V ± 0.15 V	2.5	7.5	13.2	0.5	15.4	
			2.5 V ± 0.2 V	2.9	5.5	8.6	1.2	10.6	
			3.3 V ± 0.3 V	2.7	4.6	6.7	1.4	8.3	
t_{dis}	$\overline{OE}$	Y	0.8 V		17.9				ns
			1.2 V ± 0.1 V	0.5	8.7	17.4	0.5	17.6	
			1.5 V ± 0.1 V	0.5	6.5	14.0	0.5	14.0	
			1.8 V ± 0.15 V	2.4	8.1	12.9	2.3	13.0	
			2.5 V ± 0.2 V	1.8	5.7	10.4	1.7	10.6	
			3.3 V ± 0.3 V	3.9	8.6	13.5	3.8	13.6	
t_{en}	OE	Y	0.8 V		32.8				ns
			1.2 V ± 0.1 V	0.5	14.4	32.4	0.5	33.1	
			1.5 V ± 0.1 V	2.5	9.7	18.5	1.1	19.9	
			1.8 V ± 0.15 V	2.3	7.6	14.3	0.8	15.7	
			2.5 V ± 0.2 V	2.4	5.3	9	1.2	10.3	
			3.3 V ± 0.3 V	2.8	4.6	7.2	1.7	8.2	
t_{dis}	OE	Y	0.8 V		20.1				ns
			1.2 V ± 0.1 V	0.5	10.3	19.3	0.5	19.3	
			1.5 V ± 0.1 V	1.9	7.6	14.5	1.8	14.5	
			1.8 V ± 0.15 V	3	8.8	14.9	2.8	14.9	
			2.5 V ± 0.2 V	2.9	6.5	10	2.9	10.1	
			3.3 V ± 0.3 V	0.5	8.2	17.9	0.5	17.9	

OPERATING CHARACTERISTICS

T_A = 25°C

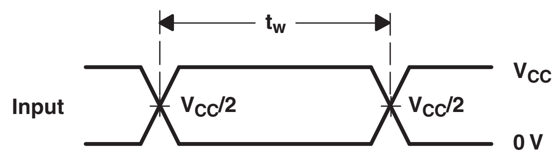
PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	4	pF
				1.2 V ± 0.1 V	3.9	
				1.5 V ± 0.1 V	3.9	
				1.8 V ± 0.15 V	3.9	
				2.5 V ± 0.2 V	4	
				3.3 V ± 0.3 V	4.2	
		Outputs disabled		0.8 V	0	
				1.2 V ± 0.1 V	0	
				1.5 V ± 0.1 V	0	
				1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

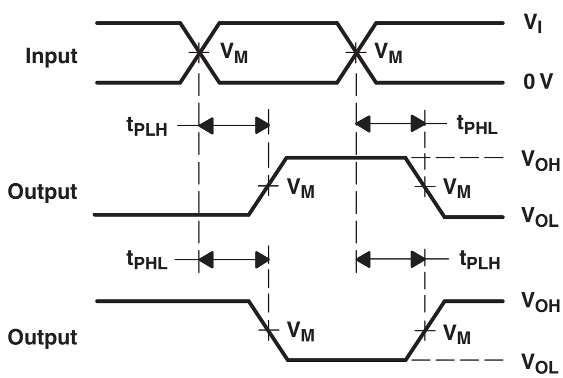


LOAD CIRCUIT

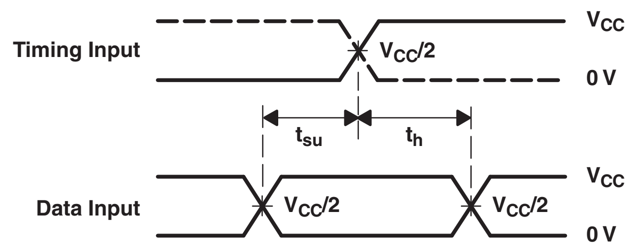
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, for propagation delays t_r/t_f = 3 ns, for setup and hold times and pulse width t_r/t_f = 1.2 ns.

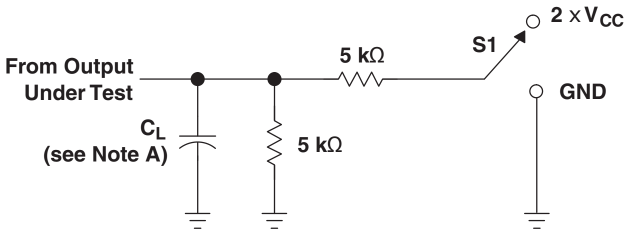
D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

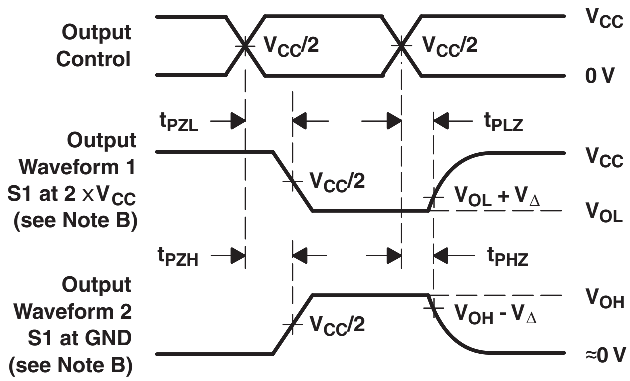
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
1B2G241DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H41R
1B2G241DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H41R
SN74AUP2G241DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H41R
SN74AUP2G241DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H41R
SN74AUP2G241DQER	Active	Production	X2SON (DQE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HQ
SN74AUP2G241DQER.B	Active	Production	X2SON (DQE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HQ
SN74AUP2G241RSER	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HQ
SN74AUP2G241RSER.B	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HQ
SN74AUP2G241YFPR	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HQN
SN74AUP2G241YFPR.B	Active	Production	DSBGA (YFP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HQN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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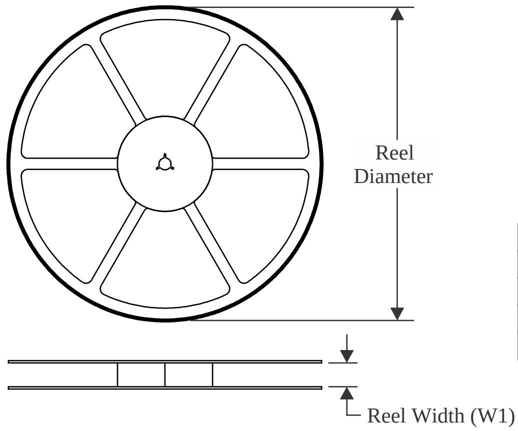
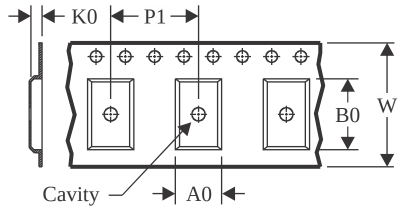
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

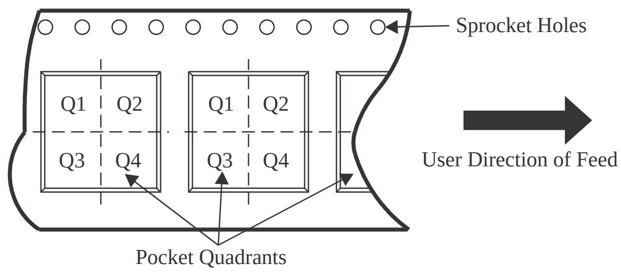


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

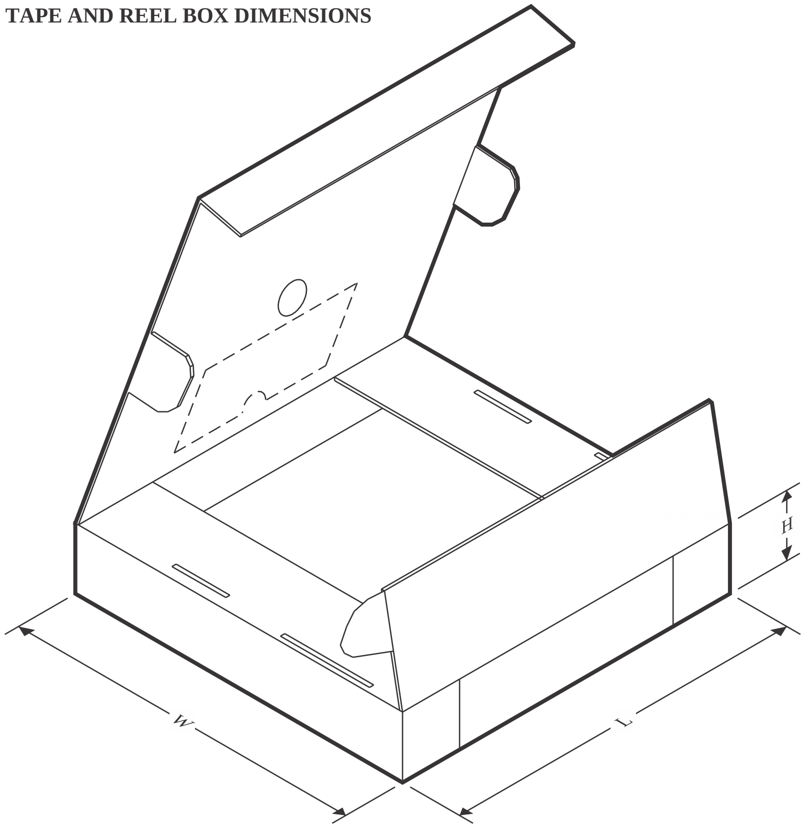
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

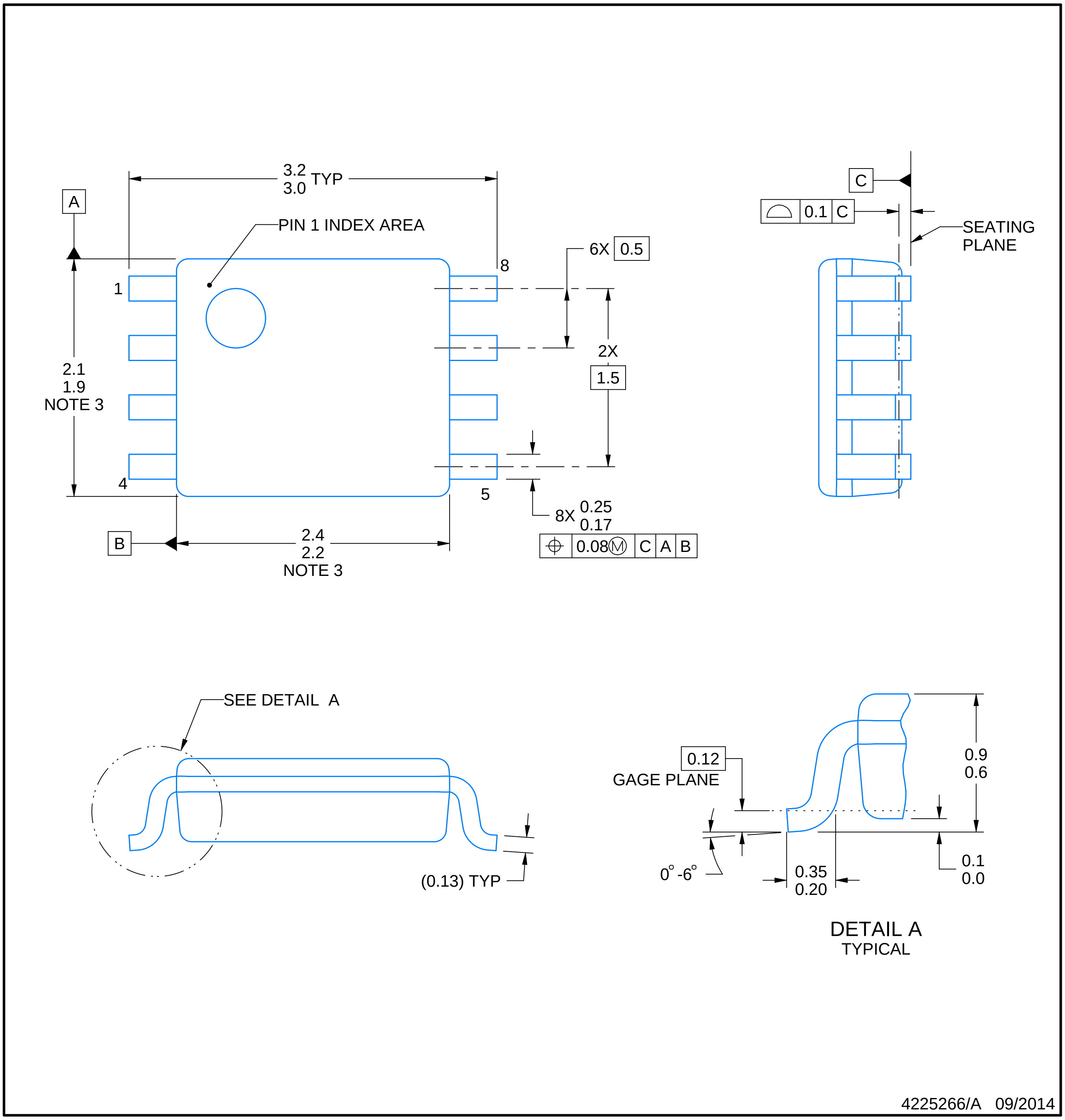
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1B2G241DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G241DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G241DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G241RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP2G241YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



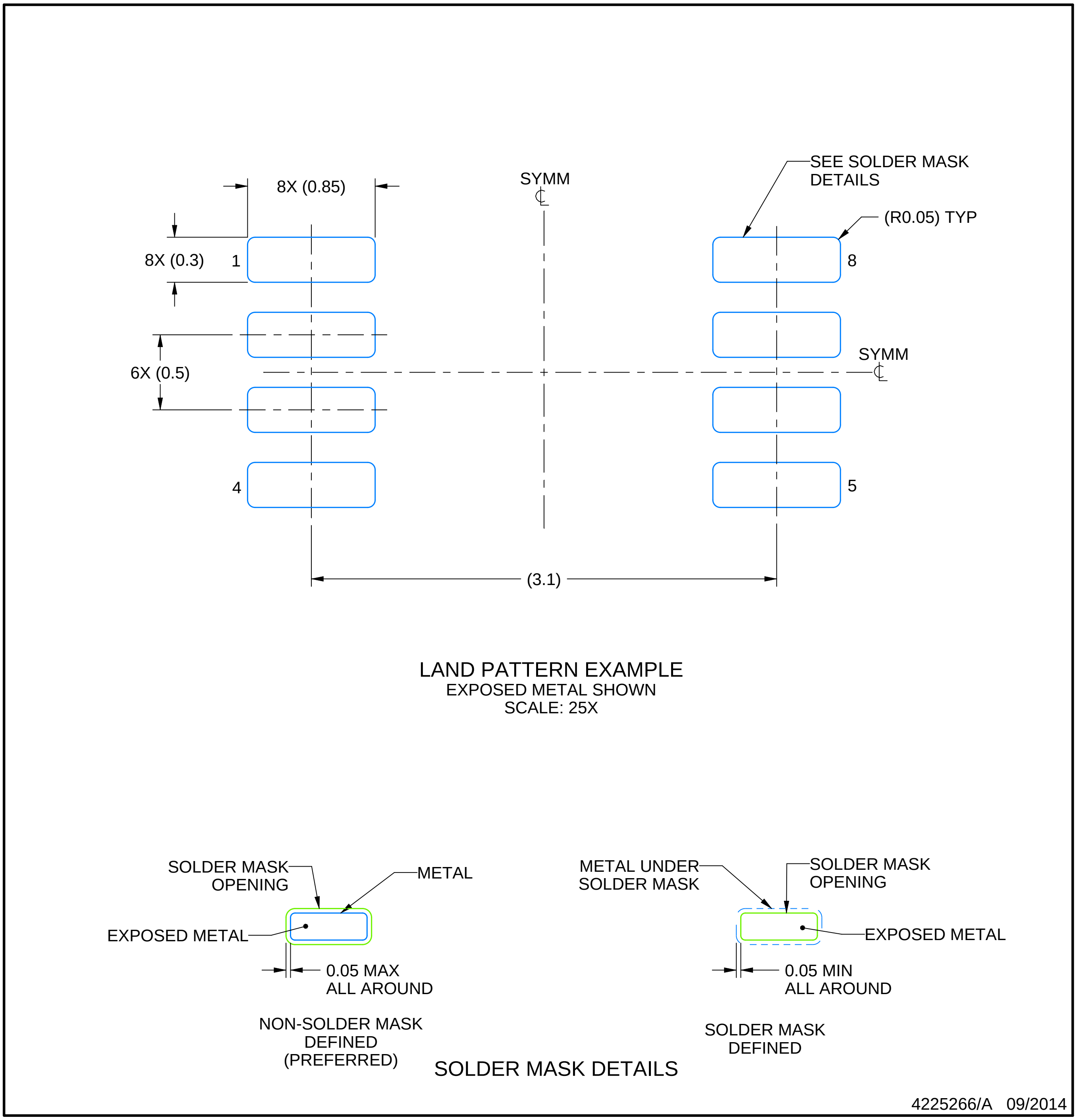
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1B2G241DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G241DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G241DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G241RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP2G241YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0



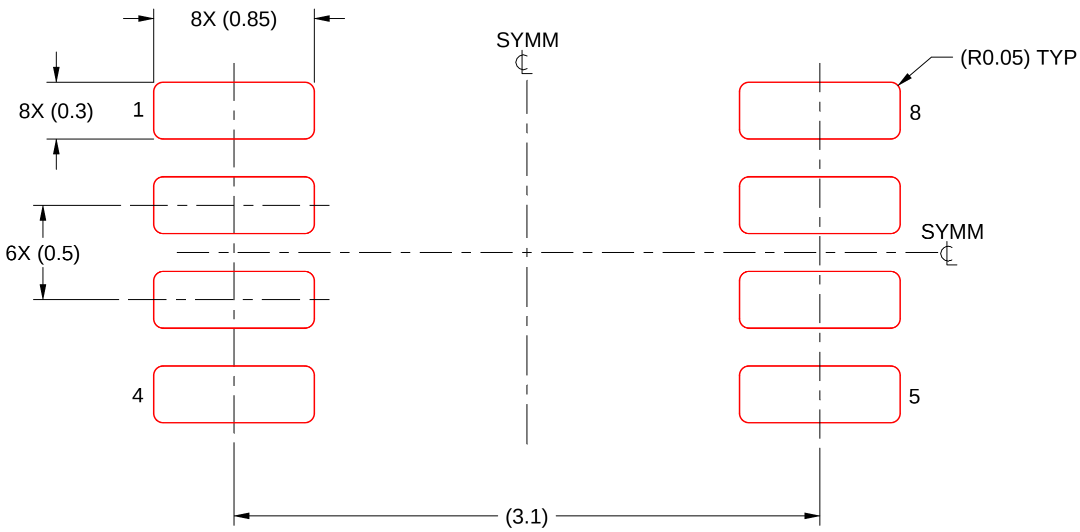
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

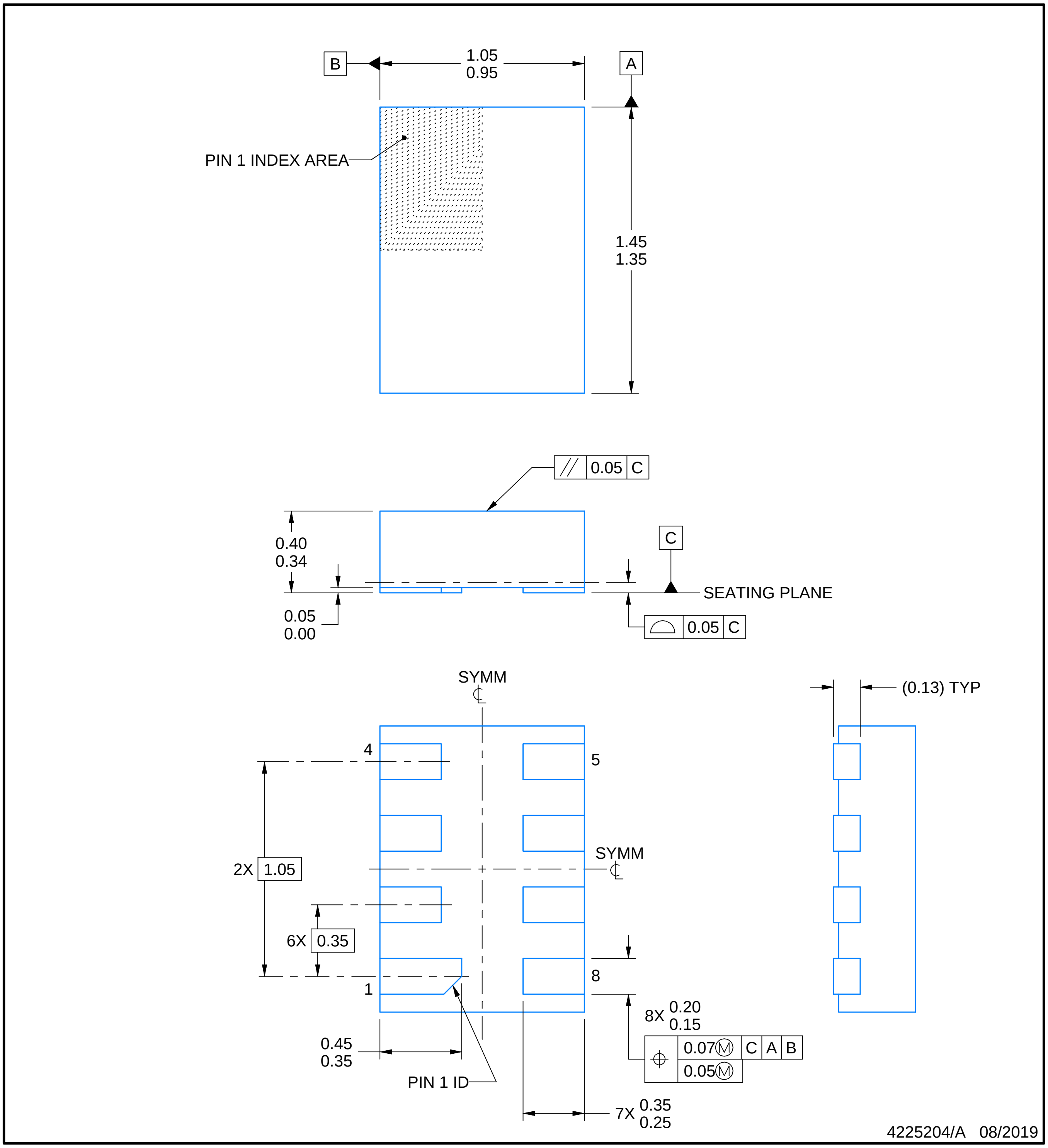


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

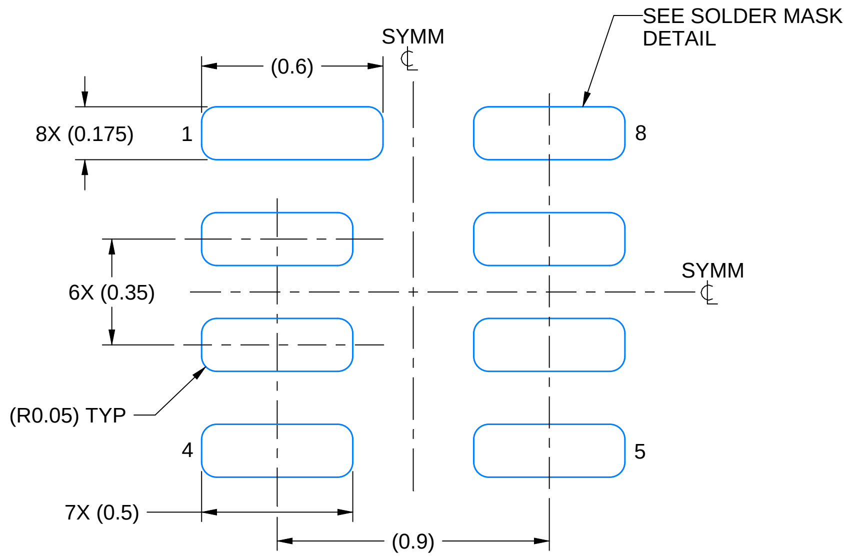
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

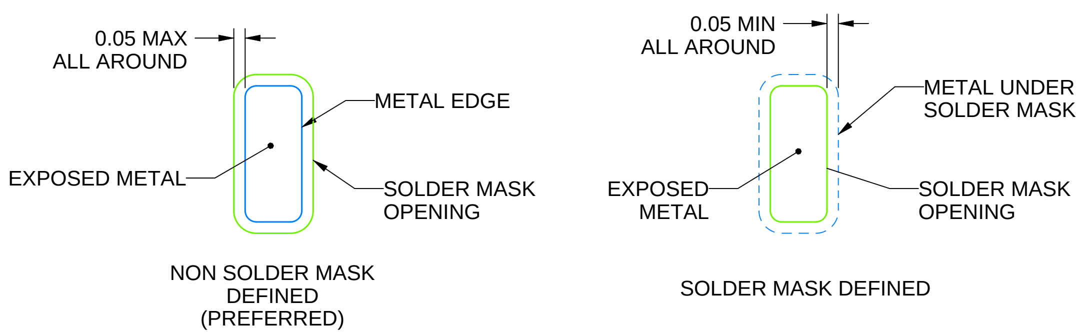


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

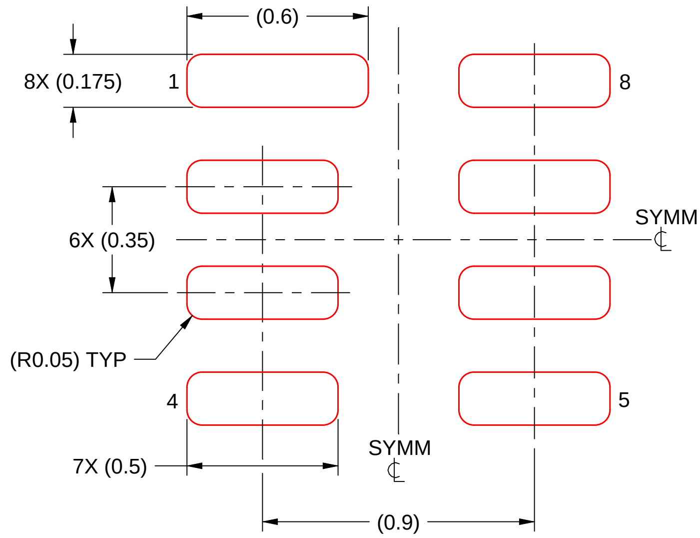


SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

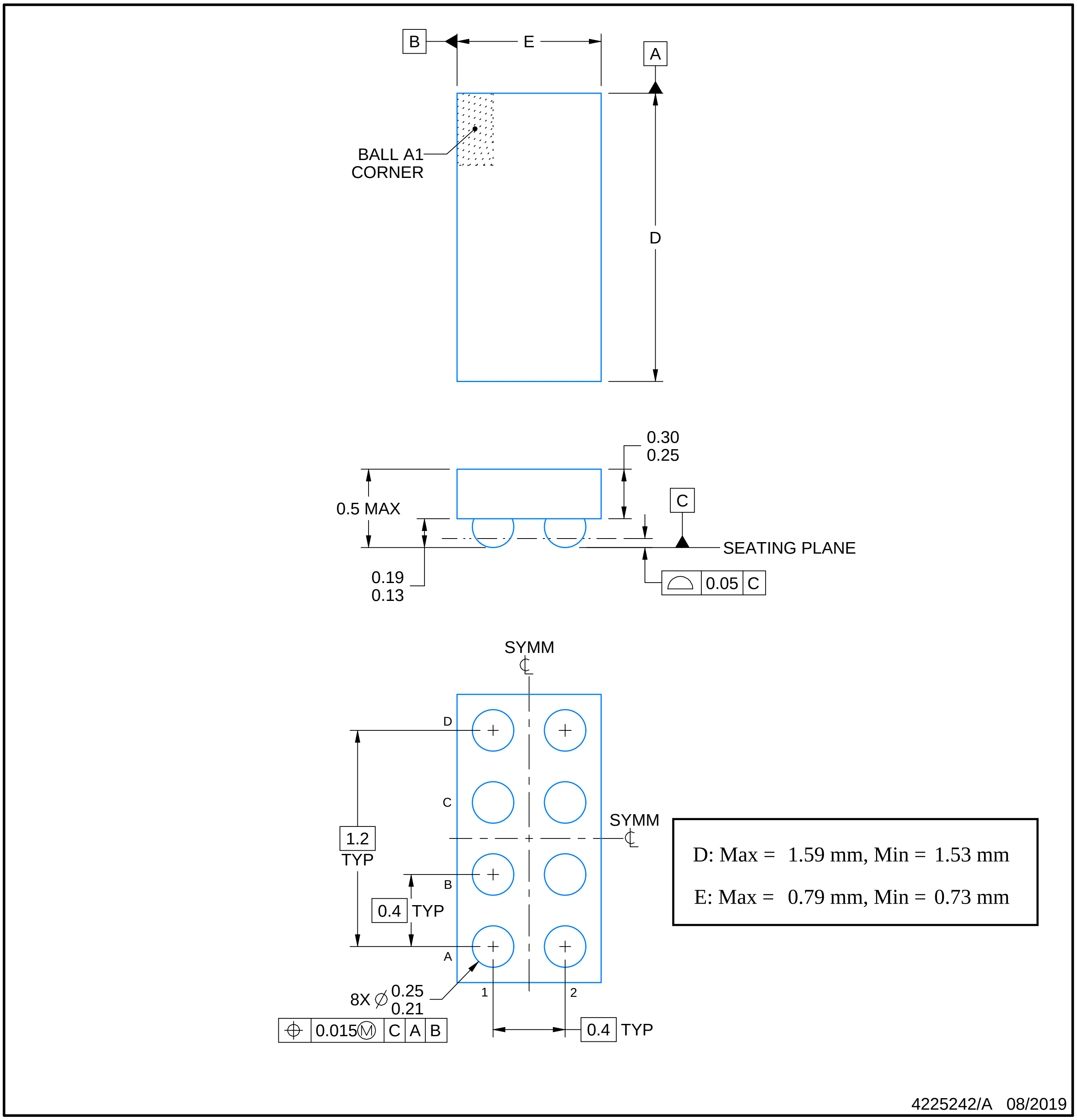


SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

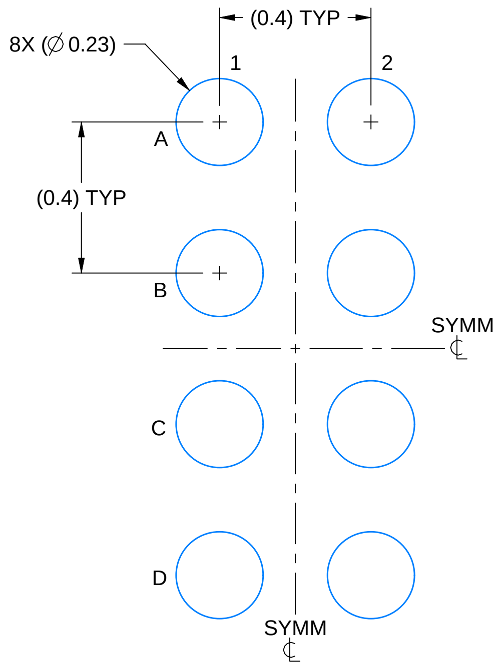
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

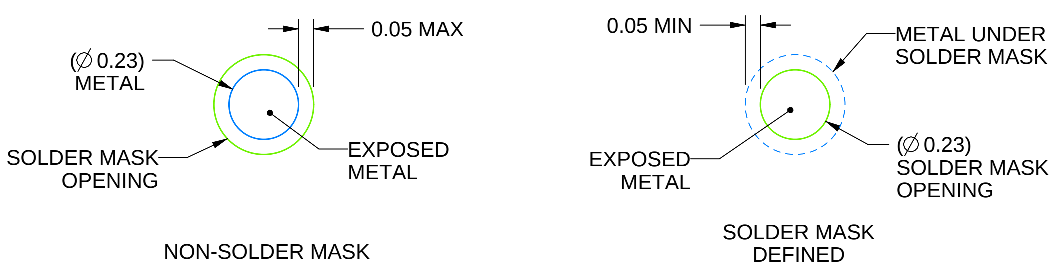


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

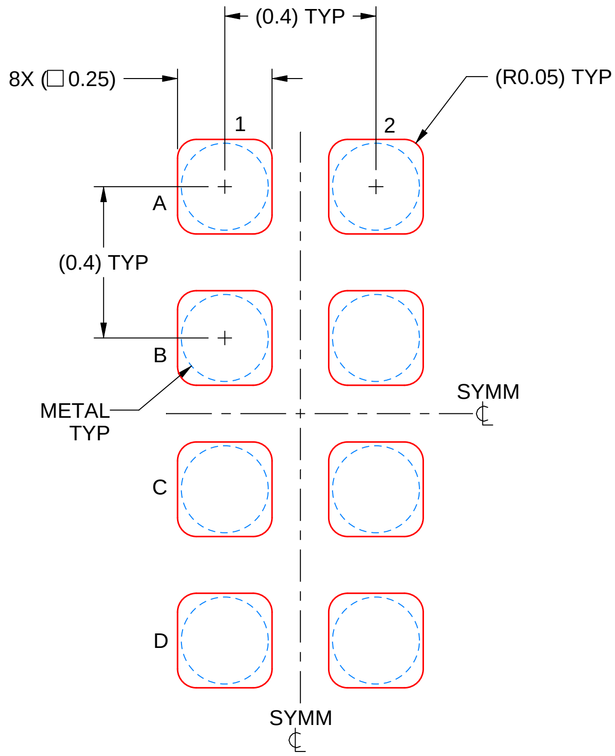


SOLDER MASK DETAILS
NOT TO SCALE

4225242/A 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4225242/A 08/2019

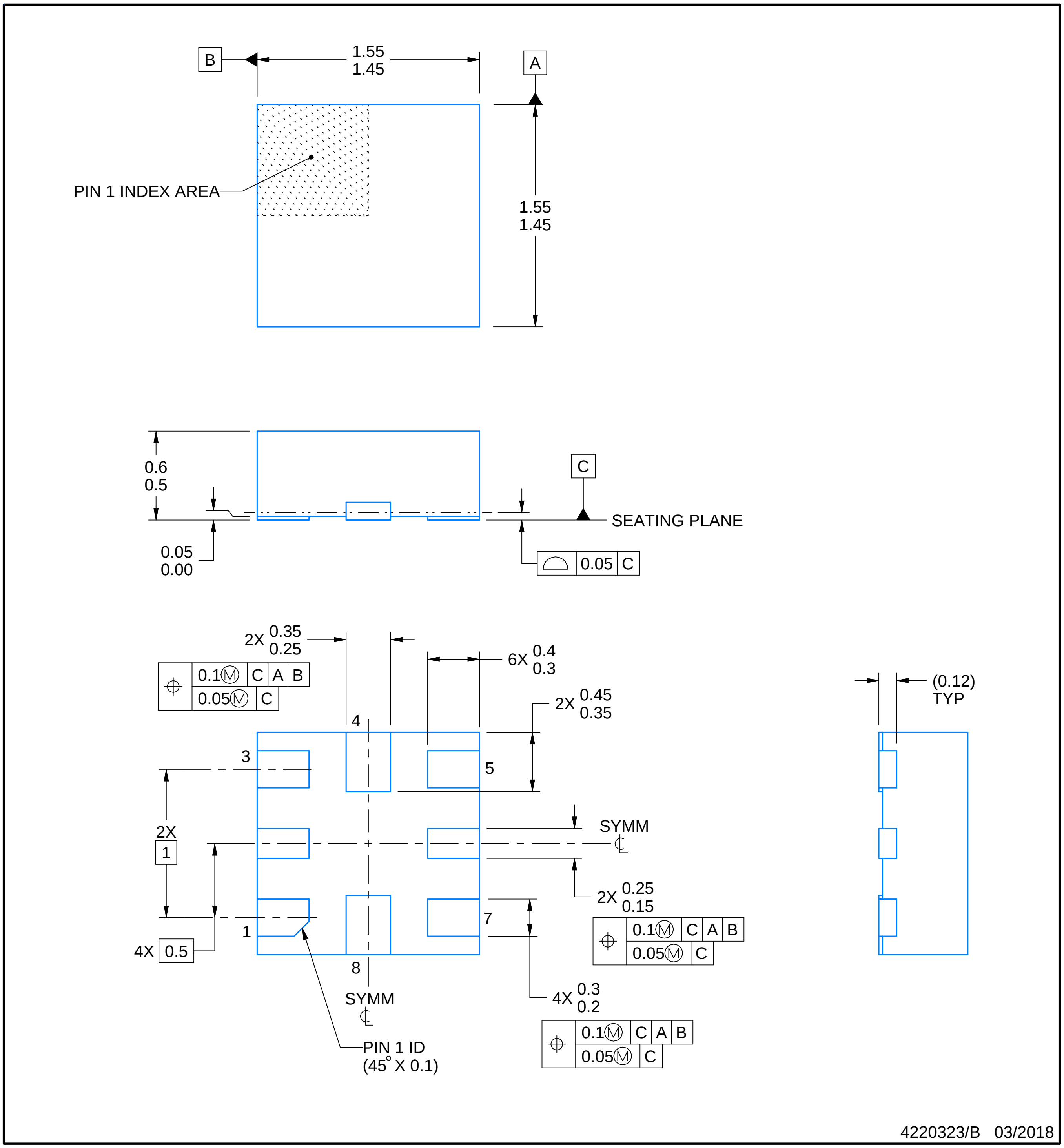
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

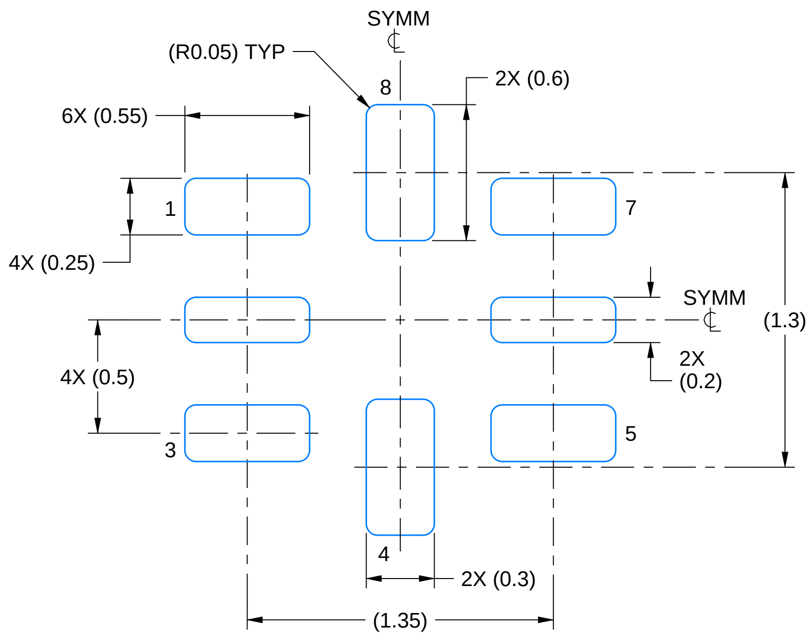
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

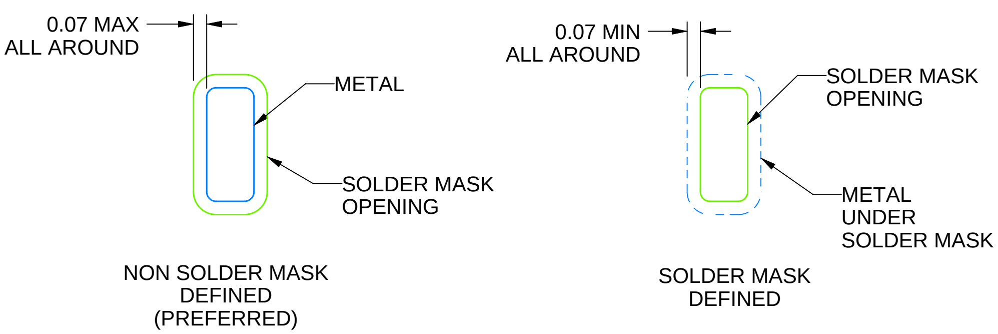


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

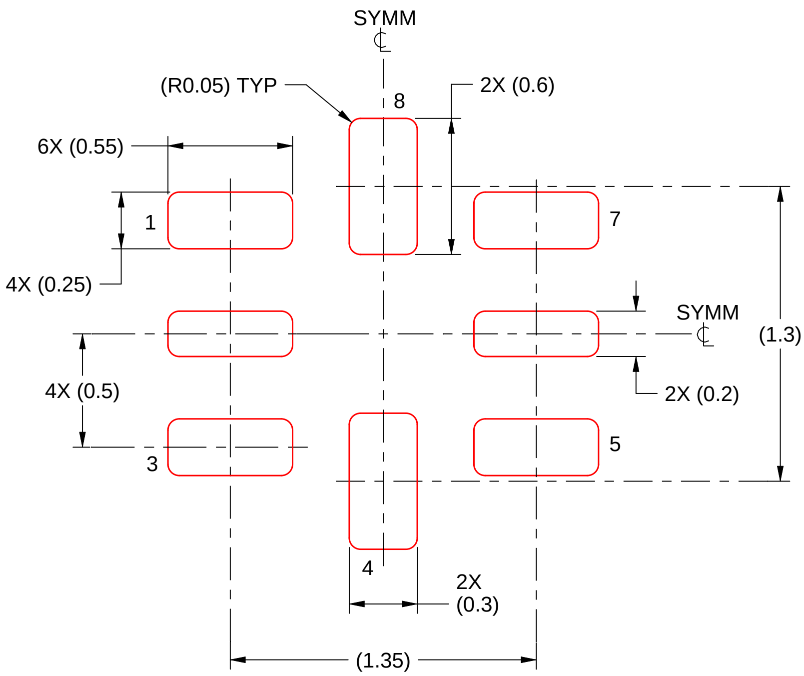


SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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