

SN74AUP2G14 Low-Power Dual Schmitt-Trigger Inverter

1 Features

- Available in the Texas Instruments NanoStar™ package
- Low static-power consumption $(I_{CC} = 0.9 \mu A \text{ maximum})$
- Low dynamic-power consumption $(C_{pd} = 4.3pF \text{ typical at } 3.3V)$
- Low input capacitance ($C_i = 1.5pF$ typical)
- Low noise overshoot and undershoot <10% of V_{CC}
- I_{off} supports partial-power-down mode operation
- Wide operating V_{CC} range of 0.8V to 3.6V
- Optimized for 3.3V operation
- 3.6V I/O tolerant to support mixed-mode signal
- t_{pd} = 4.3ns maximum at 3.3V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100mA Per JESD 78, Class II
- ESD performance tested per JESD 22
 - 2000V human-body model (A114-B, Class II)
 - 1000V charged-device model (C101)

2 Applications

- Body control modules
- Engine control modules
- Servers and high-performance computing
- EPOS, ECR, and cash drawer
- Routers
- Desktop PC

3 Description

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8V to 3.6V, resulting in increased battery life (see Figure 5-1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 5-2).

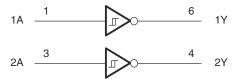
The SN74AUP2G14 contains two inverters and performs the Boolean function $Y = \overline{A}$. The device functions as two independent inverters, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going $(V_{T_{-}})$ signals.

NanoStar™ package technology is breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information

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PART NUMBER	PACKAGE	BODY SIZE (NOM)		
SN74AUP2G14DCK	SC70 (6)	2.00mm × 1.25mm		
SN74AUP2G14DRY	SON (6)	1.45mm × 1.00mm		
SN74AUP2G14DSF	SON (6)	1.00mm × 1.00mm		
SN74AUP2G14YFP	DSBGA (6)	1.00mm × 1.40mm		



Logic Diagram (Positive Logic)

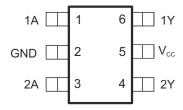


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4 Pin Configuration and Functions



See mechanical drawings for dimensions.

Figure 4-1. DCK Package 6 -Pin SC70 Top View

$$\begin{array}{c|ccccc}
1A & \boxed{\boxed{1}} & \boxed{\boxed{6}} & 1Y \\
GND & \boxed{\boxed{2}} & \boxed{\boxed{5}} & V_{cc} \\
2A & \boxed{\boxed{3}} & \boxed{\boxed{4}} & 2Y
\end{array}$$

Figure 4-2. DRY Package 6-Pin USON Top View

Figure 4-3. DSF Package 6-Pin X2SON Top View

Figure 4-4. YFP Package 6-Pin DSBGA Top View

Table 4-1. Pin Functions

		PIN			I/O	DESCRIPTION			
NAME	DCK	DRY	DSF	YFP	"0	DESCRIPTION			
1A	1	1	1	A1	II	Gate 1 logic signal			
GND	2	2	2	B1	_	Ground			
2A	3	3	3	C1	I	Gate 2 logic signal			
1Y	6	6	6	A2	0	Gate 1 inverted signal			
V _{CC}	5	5	5	B2	_	Supply/Power Pin			
2Y	4	4	4	C2	0	Gate 2 inverted signal			

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	4.6	V
VI	Input voltage ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-im	npedance or power-off state ⁽²⁾	-0.5	4.6	V
Vo	Output voltage range in the high or low state ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	·		±20	mA
	Continuous current through V _{CC} or GND			±50	mA
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.



5.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT		
V _{CC}	Supply voltage		0.8	3.6	V		
VI	Input voltage		0	3.6	V		
Vo	Output voltage		0	V _{CC}	V		
		V _{CC} = 0.8V		-20	μA		
		V _{CC} = 1.1V		-1.1			
	High level output ourrent	V _{CC} = 1.4V		-1.7			
I _{OH}	High-level output current	V _{CC} = 1.65V		-1.9	mA		
		V _{CC} = 2.3V		-3.1			
		V _{CC} = 3V		-4			
		V _{CC} = 0.8V		20	μA		
		V _{CC} = 1.1V		1.1			
	Low level output ourrent	V _{CC} = 1.4V		1.7			
I _{OL}	Low-level output current	V _{CC} = 1.65V		1.9	mA		
		V _{CC} = 2.3V		3.1			
		V _{CC} = 3V		4			
T _A	Operating free-air temperature		-40	85	°C		

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

		SN74AUP2G14						
	THERMAL METRIC ⁽¹⁾		DSF (SON)	YFP (DSBGA)	DCK (SC70)	UNIT		
		PINS	PINS	PINS	PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	234	300	132	252	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	TA	= 25°C	T _A = -40°C	to 85°C	UNIT	
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP MAX	MIN	MAX	UNII	
		0.8V	0.3	0.6	0.3	0.6		
/_		1.1V	0.53	0.9	0.53	0.9		
/ _{T+} Positive-going		1.4V	0.74	1.11	0.74	1.11	V	
nput threshold oltage		1.65V	0.91	1.29	0.91	1.29	V	
701lage		2.3V	1.37	1.77	1.37	1.77		
		3V	1.88	2.29	1.88	2.29		
		0.8V	0.1	0.6	0.1	0.6		
.,		1.1V	0.26	0.65	0.26	0.65		
/ _T _ Negative-going		1.4V	0.39	0.75	0.39	0.75	V	
nput threshold		1.65V	0.47	0.84	0.47	0.84	V	
/oltage		2.3V	0.69	1.04	0.69	1.04		
		3V	0.88	1.24	0.88	1.24		
		0.8V	0.07	0.5	0.07	0.5		
		1.1V	0.08	0.46	0.08	0.46		
ΔV _T		1.4V	0.18	0.56	0.18	0.56		
Hysteresis [V _{T+} – V _{T–})		1.65V	0.27	0.66	0.27	0.66	V	
1-7		2.3V	0.53	0.92	0.53	0.92		
		3V	0.79	1.31	0.79	1.31		
	I _{OH} = -20μA	0.8V to 3.6V	V _{CC} - 0.1		V _{CC} - 0.1			
	I _{OH} = -1.1mA	1.1V	0.75 × V _{CC}		0.7 × V _{CC}			
Ī	$I_{OH} = -1.7 \text{mA}$	1.4V	1.11		1.03			
	$I_{OH} = -1.9 \text{mA}$	1.65V	1.32		1.3			
/ _{OH}	$I_{OH} = -2.3$ mA		2.05		1.97		V	
	$I_{OH} = -3.1 \text{mA}$	2.3V	1.9		1.85			
	$I_{OH} = -2.7 \text{mA}$		2.72		2.67			
	$I_{OH} = -4mA$	3V	2.6		2.55			
	I _{OL} = 20μA	0.8 V to 3.6V		0.1		0.1		
	I _{OL} = 1.1mA	1.1V		0.3 × V _{CC}		0.3 × V _{CC}		
	I _{OL} = 1.7mA	1.4V		0.31		0.37		
	I _{OL} = 1.9mA	1.65V		0.31		0.35		
/ _{OL}	I _{OL} = 2.3mA			0.31		0.33	V	
	I _{OL} = 3.1mA	2.3V		0.44		0.45		
	I _{OL} = 2.7mA			0.31		0.33		
	I _{OL} = 4mA	3V		0.44		0.45		
A or B input	V _I = GND to 3.6V	0V to 3.6V		0.1		0.5	μA	
off	$V_1 \text{ or } V_0 = 0V \text{ to } 3.6V$	0V		0.2		0.6	<u>.</u> μΑ	
ΔI _{off}	V_1 or $V_0 = 0V$ to 3.6V	0V to 0.2V		0.2		0.6	<u>.</u> μΑ	
cc	V _I = GND or (V _{CC} to 3.6V), I _O = 0	0.8V to 3.6V		0.5		0.9	μA	
7l ^{CC}	$V_1 = V_{CC} - 0.6V^{(1)}, I_O = 0$	3.3V		40		50	μΑ	
<u></u>	$V_1 = V_{CC}$ or GND	0V		1.5			pF	
		3.6V		1.5			P'	
Co	V _O = GND	0V		3			pF	

⁽¹⁾ One input at V_{CC} – 0.6V, other input at V_{CC} or GND.



5.6 Switching Characteristics

over recommended operating free-air temperature range, Switching Characteristics: $C_L = 5pF$ (unless otherwise noted) (see Figure 6-3 and Figure 6-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
PARAMETER				MIN	TYP	MAX	MIN	MAX	ONII
			0.8V		18				
	А	Y	1.2V ± 0.1V	2.6	7.3	12.8	2.1	15.6	
			1.5V ± 0.1V	1.4	5.2	8.7	0.9	10.3	
ι _{pd}			1.8V ± 0.15V	1	4.2	6.6	0.5	8.2	ns
			2.5V ± 0.2V	1	3	4.4	0.5	5.5	
			3.3V ± 0.3V	1	2.4	3.5	0.5	4.3	

5.7 Switching Characteristics

over recommended operating free-air temperature range, Switching Characteristics $C_L = 10pF$ (unless otherwise noted) (see Figure 6-3 and Figure 6-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
PARAWETER				MIN	TYP	MAX	MIN	MAX	
	А		0.8V		18.4				
		Y	1.2V ± 0.1V	4.6	7.9	13.4	1.3	16.7	
			1.5V ± 0.1V	4	6	9.6	2.2	11.8	
L _{pd}			1.8V ± 0.15V	3.6	5	7.9	2.4	9.5	ns
			2.5V ± 0.2V	3.2	4	5.5	2.3	6.8	
			3.3V ± 0.3V	2.9	3.5	4.6	2.1	5.6	

5.8 Switching Characteristics

over recommended operating free-air temperature range, Switching Characteristics C_L = 15pF (unless otherwise noted) (see Figure 6-3 and Figure 6-4)

PARAMETER	FROM	TO (OUTPUT)	V	T _A = 25°C			T _A = -40°C to 85°C		UNIT
PARAWEIER	(INPUT)		V _{cc}	MIN	TYP	MAX	MIN	MAX	UNII
			0.8V		24				
		Y	1.2V ± 0.1V	3.6	9.9	16.3	3.1	19.9	
			1.5V ± 0.1V	2.3	7.2	11.1	1.8	13.2	20
t _{pd}	A		1.8V ± 0.15V	1.6	5.8	8.7	1.1	10.6	ns
			2.5V ± 0.2V	1	4.3	5.9	0.5	7.3	
			3.3V ± 0.3V	1	3.4	4.8	0.5	5.9	



5.9 Switching Characteristics

over recommended operating free-air temperature range, Switching Characteristics $C_L = 30pF$ (unless otherwise noted) (see Figure 6-3 and Figure 6-4)

PARAMETER	FROM	TO (OUTPUT)	Voc	T _A = 25°C			T _A = -40°C t	UNIT	
PARAMETER	(INPUT)		V _{cc}	MIN	TYP	MAX	MIN	MAX	CIVIT
			0.8V		32.8				
			1.2V ± 0.1V	4.9	13.1	20.9	4.4	25.5	
	A	Y	1.5V ± 0.1V	3.4	9.5	14.2	2.9	16.9	
ι _{pd}	A	Y	1.8V ± 0.15V	2.5	7.7	11	2	13.5	ns
			2.5V ± 0.2V	1.8	5.7	7.6	1.3	9.4	
			3.3V ± 0.3V	1.5	4.7	6.2	1	7.5	

5.10 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT
			0.8V	4	
	Power dissipation capacitance		1.2V ± 0.1V	4	pF
		f = 10MHz	1.5V ± 0.1V	4	
C _{pd}		I - TOWITIZ	1.8V ± 0.15V	4	
			2.5V ± 0.2V	4.1	
			3.3V ± 0.3V	4.3	

5.11 Typical Characteristics

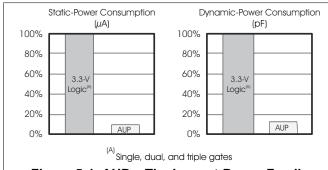
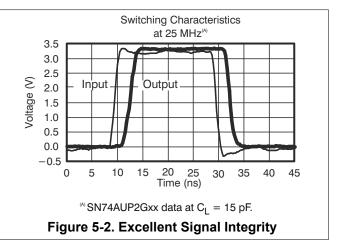


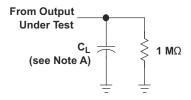
Figure 5-1. AUP - The Lowest-Power Family



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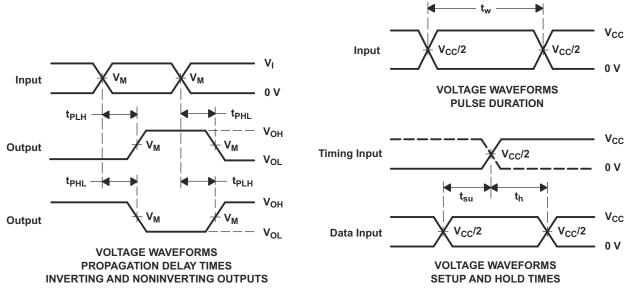
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6 Parameter Measurement Information



LOAD CIRCUIT

	V _{CC} = 0.8 V	$V_{CC} = 1.2 \text{ V} $ $V_{CC} = 1.5 \text{ V} $ $\pm 0.1 \text{ V} $		V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}



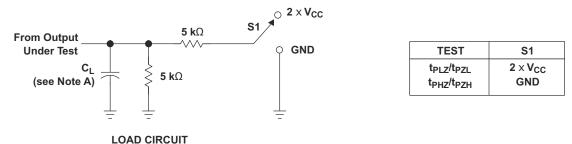
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10MHz, $Z_O = 50\Omega$, for propagation delays $t_r/t_f = 3$ ns, for setup and hold times and pulse width $t_r/t_f = 1.2$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd}.
- F. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

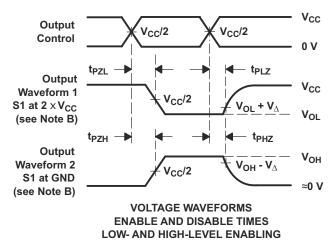
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	V _{CC} = 0.8 V	$V_{CC} = 1.2 \text{ V}$ $V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$		V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V_{CC} = 3.3 V \pm 0.3 V	
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	
V _∆	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V	

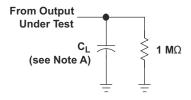


- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10MHz, $Z_0 = 50\Omega$, $t_r/t_f = 3$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

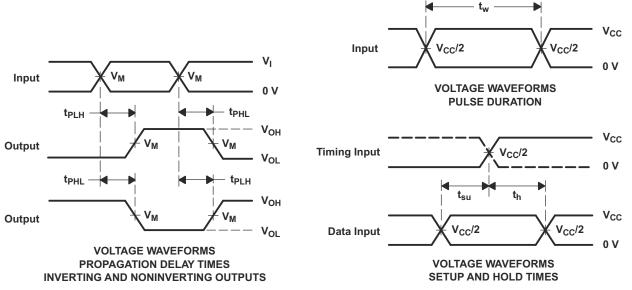


6.1 Propagation Delays, Setup and Hold Times, and Pulse Width



LOAD CIRCUIT

	V _{CC} = 0.8 V	$_{C} = 0.8 \text{ V}$ $V_{CC} = 1.2 \text{ V}$ $V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$		V_{CC} = 1.8 V \pm 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, for propagation delays $t_r/t_f = 3$ ns, for setup and hold times and pulse width $t_r/t_f = 1.2$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. All parameters and waveforms are not applicable to all devices.

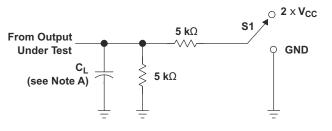
Figure 6-3. Load Circuit and Voltage Waveforms

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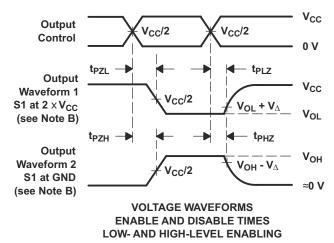
6.2 Enable and Disable Times



TEST	S1
t_{PLZ}/t_{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V_{CC} = 3.3 V \pm 0.3 V
CL	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
\mathbf{v}_{M}	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V_{I}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
$\mathbf{V}_{\!\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_t/t_f = 3$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PLH} and t_{PHL} are the same as t_{pd}.

Submit Document Feedback

G. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AUP2G14 contains two inverters and performs the Boolean function Y = A. The device functions as two independent inverters, but because of Schmitt action, it may have different input threshold levels for positivegoing (VT+) and negative-going (VT-) signals.

This device is fully specified for partial-power-down applications using loff. The loff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

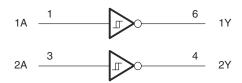


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

As the inputs are 5.5V tolerant, the device can be used as a down translator. When the input voltage exceeds VT+ (Max), the output will follow VCC, performing down-translation if the input voltage exceeds VCC.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of SN74AUP2G14.

Table 7-1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AUP2G14 contains two inverters and performs the Boolean function $Y = \overline{A}$. The device functions as two independent inverters, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

8.2 Typical Application

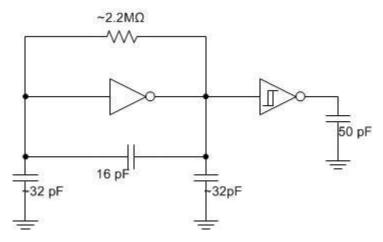


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the Section 5.3 table.
 - Specified high and low levels. See (V_{IH} and V_{II}) in the Section 5.3 table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Section 5.3 table at any valid V_{CC} .
- 2. Recommend Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the Section 5.1 table.
 - Outputs should not be pulled above V_{CC}.

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the table. Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a $0.1\mu F$ capacitor. If there are multiple VCC pins, then TI recommends a $0.01\mu F$ or $0.022\mu F$ capacitor for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- · Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - · Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

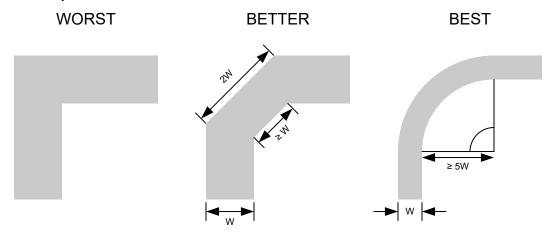


Figure 8-2. Example Trace Corners for Improved Signal Integrity



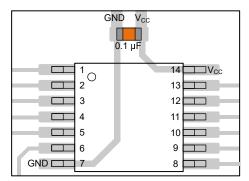


Figure 8-3. Example Bypass Capacitor Placement for TSSOP and Similar Packages

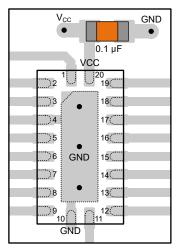


Figure 8-4. Example Bypass Capacitor Placement for WQFN and Similar Packages

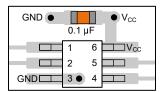


Figure 8-5. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages



Figure 8-6. Example Damping Resistor Placement for Improved Signal Integrity

Product Folder Links: SN74AUP2G14

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and C_{pd} Calculation application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2012) to Revision D (June 2025)

Page

- Added Package Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Device Functional Modes, Application and Implementation section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section
- Updated operating temperature to 125°C and respective values in Electrical Characteristics table,
 Recommended Operating Conditions table, and Switching Characteristics tables......

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Cł	hanges from Revision B (March 2012) to Revision C (February 2012)	Page
•	Updated ORDERING INFORMATION table.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	. ,	``				(4)	(5)		
SN74AUP2G14DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(H65, H6F)
SN74AUP2G14DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(H65, H6F)
SN74AUP2G14DCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H65, H6F)
SN74AUP2G14DCKRG4.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H65, H6F)
SN74AUP2G14DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DSF2	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DSF2.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H6
SN74AUP2G14YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HFN
SN74AUP2G14YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HFN

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G14DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP2G14DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP2G14DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP2G14DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G14DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G14DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP2G14DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G14DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G14YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1



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*All dimensions are nominal

All difficultions are norminal							
Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G14DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AUP2G14DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP2G14DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G14DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G14DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G14DSF2	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G14DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G14DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G14YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



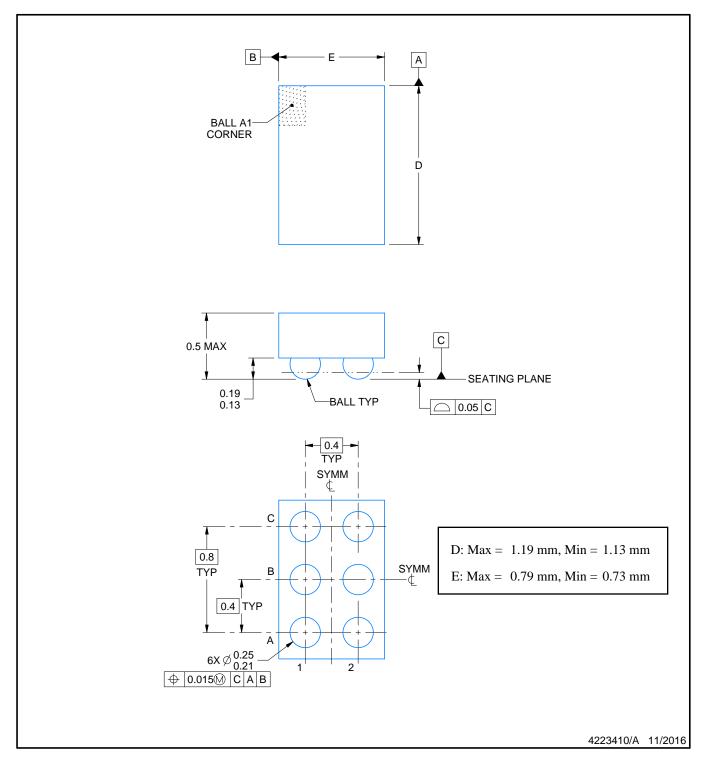


4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





DIE SIZE BALL GRID ARRAY

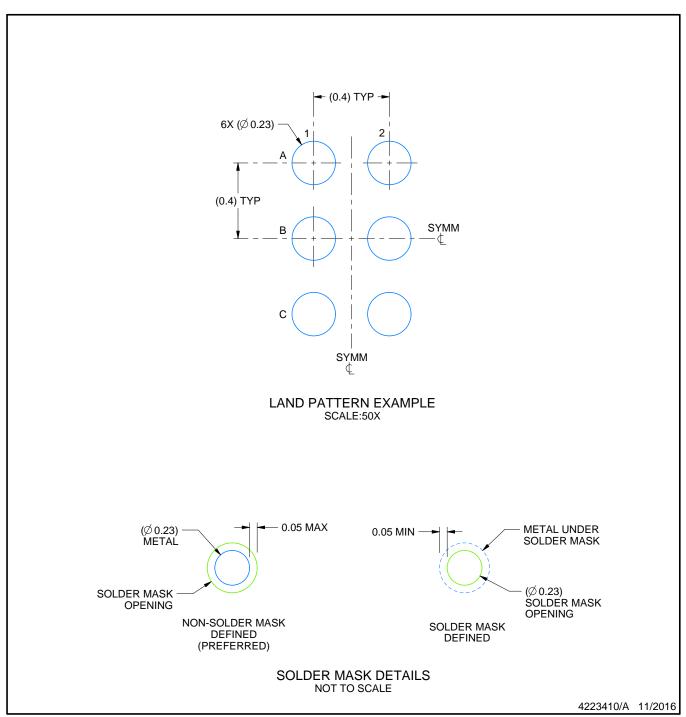


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY

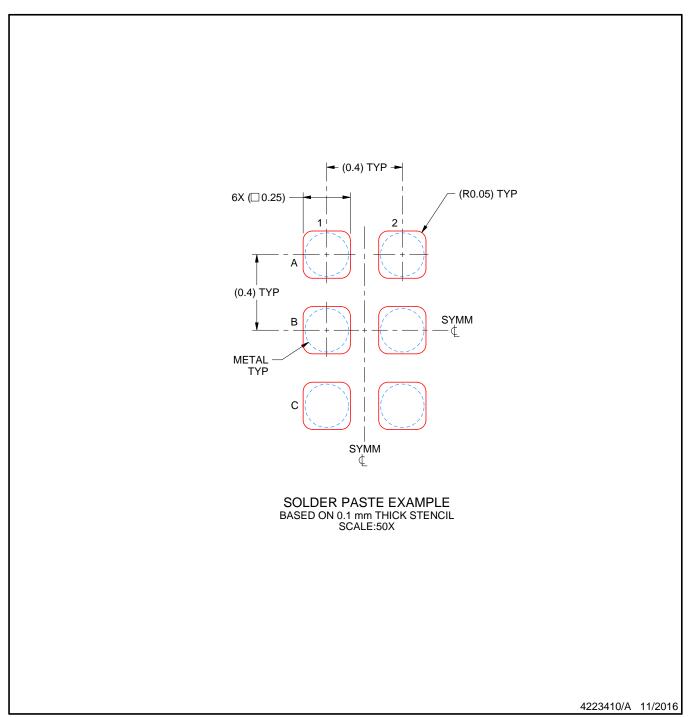


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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