









SN74AUP2G07 SCES748E - SEPTEMBER 2009 - REVISED OCTOBER 2021

SN74AUP2G07 Low-Power Dual Buffer/Driver With Open-Drain Outputs

1 Features

- Low static-power consumption $(I_{CC} = 0.9 \mu A \text{ maximum})$
- Low dynamic-power consumption $(C_{pd} = 1 pF typical at 3.3 V)$
- Low input capacitance ($C_i = 1.5 \text{ pF typical}$)
- Low noise overshoot and undershoot <10% of V_{CC}
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Input hysteresis allows slow input transition and better switching noise immunity at the input $(V_{hvs} = 250 \text{ mV typical at } 3.3 \text{ V})$
- Wide operating V_{CC} range of 0.8 V to 3.6 V
- Optimized for 3.3 V operation
- 3.6-V I/O tolerant to support mixed-mode signal operation
- t_{pd} = 3.3 ns maximum at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22
 - 4500-V human-body model
 - 1500-V charged-device model

2 Applications

- Active noise cancellation (ANC)
- Barcode scanners
- Blood pressure monitors
- **CPAP** machines
- Cable solutions
- DLP 3D machine vision, hyperspectral imaging, optical networking, and spectroscopy
- E-books and smartphones
- **Embedded PCs**
- Field transmitters: temperature or pressure sensor
- Fingerprint biometrics
- HVAC: heating, ventilating, and air conditioning
- Network-attached storage (NAS)
- Server motherboards and PSUs
- Software defined radios (SDR)
- TVs: high-definition (HDTV), LCD, and digital
- Video communication systems
- Wireless data access cards, headsets, keyboards, mice, and LAN cards
- X-ray: baggage scanners, medical, and dental

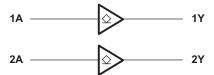
3 Description

The SN74AUP2G07 device is a dual buffer gate with open drain output that operates from 0.8 V to 3.6 V.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)		
	SC70 (6)	3.00 mm × 1.25 mm		
SN74AUP2G07	SON (6)	1.45 mm × 1.00 mm		
SN/4AUF2GU/	SON (6)	1.00 mm × 1.00 mm		
	DSBGA (6)	1.16 mm × 0.76 mm		

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram



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4 Revision History NOTE: Page numbers for previous revisions may of the control	evisi	on E (October 2021)	Page
BGA pin numbers in the <i>Pin Functions</i> table, ch <i>Functions</i> table and added footnote to the <i>Pin F</i> Changed maximum output voltage in the low sta 	ange <i>uncti</i> ate in	ed overlapping letters in YZP package drawing, country V _{CC} and GND pin TYPE From: "—" To: "P" in the constable to define pin types	e <i>Pin</i> 3 4
 Updated R_{0JA} values to more accurately reflect DRY 234 to 338, DSF 300 to 372.5, added stan 	devid dard	ble from 'V _{CC} ' to '3.6'ee characteristics: YFP 132 to 125.4, DCK 252 to 3 thermal characteristics for all packages ($R_{\theta JC(top)}$,	802.4, R _{θJB} ,
Changes from Revision C (November 2014) to F	Revis	ion D (February 2016)	Page

Deleted V_{OH} PARAMETER from the Section 6.5 table, these specifications do not pertain to open drain devices.

C	hanges from Revision B (September 2009) to Revision C (November 2014)	Page
•	Removed Ordering Information table	1
	Added Applications, Device Information table, Pin Functions table, Handling Ratings table, Thermal	
	Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application	cation
	and Implementation section, Power Supply Recommendations section, Layout section, Device and	
	Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Updated I _{off} in <i>Features</i> .	1

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5 Pin Configuration and Functions

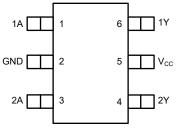


Figure 5-1. DCK Package 6-Pin SC70 Top View

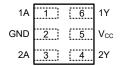


Figure 5-3. DSF Package 6-Pin SON Transparent Top View

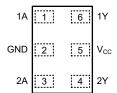


Figure 5-2. DRY Package 6-Pin SON Transparent Top View

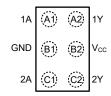


Figure 5-4. YFP Package 6-Pin DSBGA Transparent Top View

See the mechanical drawings for dimensions.

Table 5-1. Pin Functions

	PIN			
NAME	DCK, DSF, DRY, YFP	(BGA) YFP	TYPE (1)	DESCRIPTION
1A	1	A1	I	Input 1
1Y	6	A2	0	Output 1
2A	3	C1	I	Input 2
2Y	4	C2	0	Output 2
GND	2	B1	Р	Ground
V _{CC}	5	B2	Р	Power Pin

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽¹⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-imped	lance or power-off state ⁽¹⁾	-0.5	4.6	V
Vo	Output voltage range in the low state ⁽¹⁾		-0.5	4.6	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	•		±20	mA
	Continuous current through V _{CC} or GND			±50	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4500	
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

Product Folder Links: SN74AUP2G07

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		,	MIN	MAX	UNIT		
V _{CC}	Supply voltage		0.8	3.6	V		
		V _{CC} = 0.8 V	V _{CC}				
V	High level input veltage	V_{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		V		
V_{IH}	High-level input voltage Low-level input voltage Input voltage Output voltage Low-level output current	V_{CC} = 2.3 V to 2.7 V	1.6		V		
		V _{CC} = 3 V to 3.6 V	2				
		V _{CC} = 0.8 V		0			
.,	High-level input voltage Low-level input voltage Input voltage Output voltage Low-level output current	V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}	.,		
V_{IL}		V_{CC} = 2.3 V to 2.7 V		0.7	V		
		V _{CC} = 3 V to 3.6 V		0.9			
VI	Input voltage		0	3.6	V		
Vo	Output voltage		0	3.6	V		
		V _{CC} = 0.8 V		20	μA		
		V _{CC} = 1.1 V		1.1			
	Lour lovel output ourrent	V _{CC} = 1.4 V		1.7			
l _{OL}	Low-level output current	V _{CC} = 1.65 V		1.9	mA		
		V _{CC} = 2.3 V		3.1			
		V _{CC} = 3 V		4			
Δt/Δν	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V		
T _A	Operating free-air temperature		-40	85	°C		

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	YFP	DCK	DRY	DSF	UNIT
I HERMAL METRIC(*)		6 PINS	6 PINS	6 PINS	6 PINS	UNII
R _{0JA}	Junction-to-ambient thermal resistance	125.4	302.4	338.0	372.5	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	1.9	219.5	228.9	179.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	106.7	203.5	231.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	84.2	62.4	28.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.5	106.0	203.6	230.9	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	T _A = 25°C	T _A = -40°C to 85°C	LINUT	
PARAMETER	TEST CONDITIONS	V _{CC}	MIN TYP MAX	MIN MAX	UNIT	
	I _{OL} = 20 μA	0.8 V to 3.6 V	0.1	0.1		
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}	0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V	0.31	0.37	V	
V	I _{OL} = 1.9 mA	1.65 V	0.31	0.35	V	
V_{OL}	I _{OL} = 2.3 mA	221/	0.31	0.33	V	
	I _{OL} = 3.1 mA	2.3 V	0.44	0.45	·	
	I _{OL} = 2.7 mA	3 V	0.31	0.33		
	I _{OL} = 4 mA	3 V	0.44	0.45		
I _I A or B input	V _I = GND to 3.6 V	0 V to 3.6 V	0.1	0.5	μA	
I _{off}	V_{I} or $V_{O} = 0 \text{ V to } 3.6 \text{ V}$	0 V	0.2	0.6	μA	
Δl _{off}	V_{I} or $V_{O} = 0 \text{ V to } 3.6 \text{ V}$	0 V to 0.2 V	0.2	0.6	μA	
Icc	$V_I = GND \text{ or } (V_{CC} \text{ to } 3.6 \text{ V}),$ $I_O = 0$	0.8 V to 3.6 V	0.5	0.9	μΑ	
ΔI _{CC}	$V_1 = V_{CC} - 0.6 V^{(1)}, I_O = 0$	3.3 V	40	50	μA	
C	V = V or CND	0 V	1.5		nE	
C _i	$V_I = V_{CC}$ or GND	3.6 V	1.5		pF	
Co	V _O = GND	0 V	3		pF	

⁽¹⁾ One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.



6.6 Switching Characteristics, $C_L = 5 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER FROM (INPUT) (O	-	TO (OUTPUT)	V _{CC}	V _{CC} T _A = 25°C			T _A = -4 to 85	UNIT												
	(001701)		MIN	TYP	MAX	MIN	MAX													
			0.8 V		12.2															
		V	V	Y		V	1.2 V ± 0.1 V	3.4	5.1	7.5	1.5	14.7								
	A						V	V	V	V	V	V	V	V	V	V	V	V	1.5 V ± 0.1 V	2.3
t _{pd}	A	ī	1.8 V ± 0.15 V	2.4	3.1	4	1	6.3	ns											
			2.5 V ± 0.2 V	1.5	2.1	2.9	0.9	4.1												
			3.3 V ± 0.3 V	1.8	2.2	2.8	1.1	3.3												

6.7 Switching Characteristics, $C_L = 10 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER FROM TO (OUTP)		_	V _{cc}	T _A = 25°C			T _A =	UNIT												
	(001701)		MIN	TYP	MAX	MIN	MAX													
			0.8 V		15															
		Y	Y	Y	Y	Y	Y	V	V	V	V	V	V	1.2 V ± 0.1 V	4	6.2	9	2.4	16.2	
	Δ													V	V	V	1.5 V ± 0.1 V	3.1	4.4	6.1
t _{pd}	Α							1.8 V ± 0.15 V	3.3	3.9	4.8	1.6	7.1	ns						
						2.5 V ± 0.2 V	2.1	2.8	3.5	1.3	4.8									
			3.3 V ± 0.3 V	2.3	3	4	1.4	4.5												

6.8 Switching Characteristics, $C_L = 15 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	T _A = 25°C			T _A =		UNIT																
	(INPOT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX																	
			0.8 V		18.2																				
		Y	Y	Y	Y	Y	Y	1.2 V ± 0.1 V	4.9	7.3	10.4	3.2	17.6												
	Δ.							Υ	Υ	Υ	V	V	V	V	V	V	V	V	1.5 V ± 0.1 V	3.8	5.2	6.8	2.6	10.2	
t _{pd}	A										1.8 V ± 0.15 V	3.4	4.8	6.7	2.2	7.9	ns								
						2.5 V ± 0.2 V	2.4	3.4	4.5	1.9	5.3														
			3.3 V ± 0.3 V	2.2	3.7	5.4	1.8	6.1																	

6.9 Switching Characteristics, $C_L = 30 pF$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	T _A = 25°C			T _A = -		UNIT	
	(INFOT)	(OUTFUT)		MIN	TYP	MAX	MIN	MAX		
	A	Y	0.8 V		26.5					
			1.2 V ± 0.1 V	8.1	10.7	14.4	4.5	21.9		
			1.5 V ± 0.1 V	6.5	7.7	9.4	3.8	13		
t _{pd}			1.8 V ± 0.15 V	5.8	7.5	9.7	3.2	11		
				2.5 V ± 0.2 V	4.5	5.4	6.7	3	7.1	
				3.3 V ± 0.3 V	3.9	6.3	9.7	2.8	10.4	

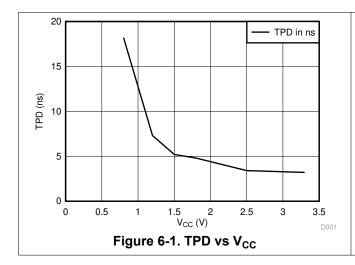


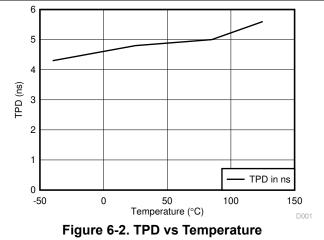
6.10 Operating Characteristics

T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT	
C. Baura			0.8 V	4		
			1.2 V ± 0.1 V	4	- pF	
	Power dissipation capacitance	f = 10 MHz	1.5 V ± 0.1 V	4		
C _{pd}			1.8 V ± 0.15 V	4		
			2.5 V ± 0.2 V	4.1		
			3.3 V ± 0.3 V	4.3		

6.11 Typical Characteristics





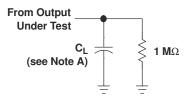
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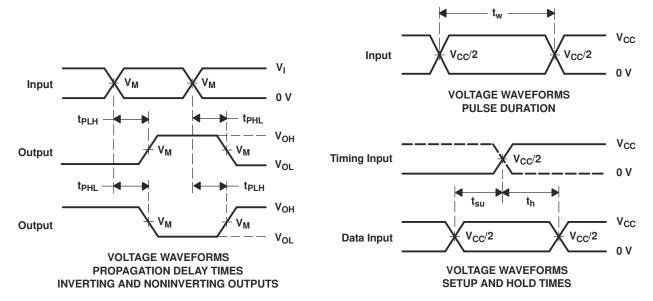
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Duration



LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V_{CC} = 3.3 V \pm 0.3 V
C _L V _M	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}



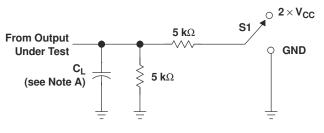
NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f = 3$ ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- $\begin{array}{ll} \text{D.} & t_{PLH} \text{ and } t_{PHL} \text{ are the same as } t_{pd}. \\ \text{E.} & \text{All parameters and waveforms are not applicable to all devices.} \end{array}$

Figure 7-1. Load Circuit and Voltage Waveforms



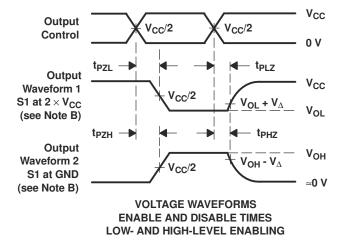
7.2 Enable and Disable Times



TEST	S1
t _{PLZ} /t _{PZL}	2 × V _{CC} GND
7112 7211	

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _∆	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f = 3$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 7-2. Load Circuit and Voltage Waveforms



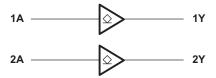
8 Detailed Description

8.1 Overview

The SN74AUP2G07 device is a dual buffer gate with open-drain outputs that operate from 0.8 V to 3.6 V. The output of this dual buffer/driver is open-drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The I_{off} feature also allows for live insertion.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- · Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- · Low noise due to slower edge rates

8.4 Device Functional Modes

Table 8-1 is the function table for SN74AUP2G07.

Table 8-1. Function Table

INPUT ⁽¹⁾	OUTPUT ⁽²⁾ Y
Н	Z
L	L

- (1) L = Input low, H = Input high
- (2) L = Output low, Z = High impedance

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The AUP family is Tl's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in, allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

9.2 Typical Application

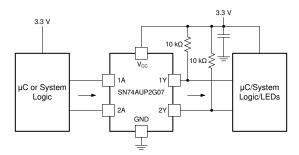


Figure 9-1. Typical Application Schematic

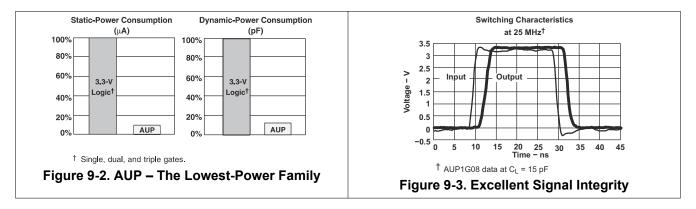
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the Section 6.3 table.
 - For specified high and low levels. See V_{IH} and V_{II} in the Section 6.3 table.
 - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}.
- 2. Recommend Output Conditions:
 - · Load currents should not exceed 20 mA on the output and 50 mA total for the part.

9.2.3 Application Curves



The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Section 6.3 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 buffer gates are used.

Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

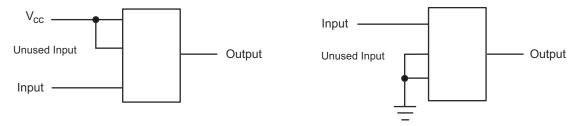


Figure 11-1. Layout Diagram



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74AUP2G07

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AUP2G07DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(H55, H5F)
SN74AUP2G07DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(H55, H5F)
SN74AUP2G07DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H5
SN74AUP2G07YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HVN
SN74AUP2G07YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HVN

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G07DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP2G07DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP2G07DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G07DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP2G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G07YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1



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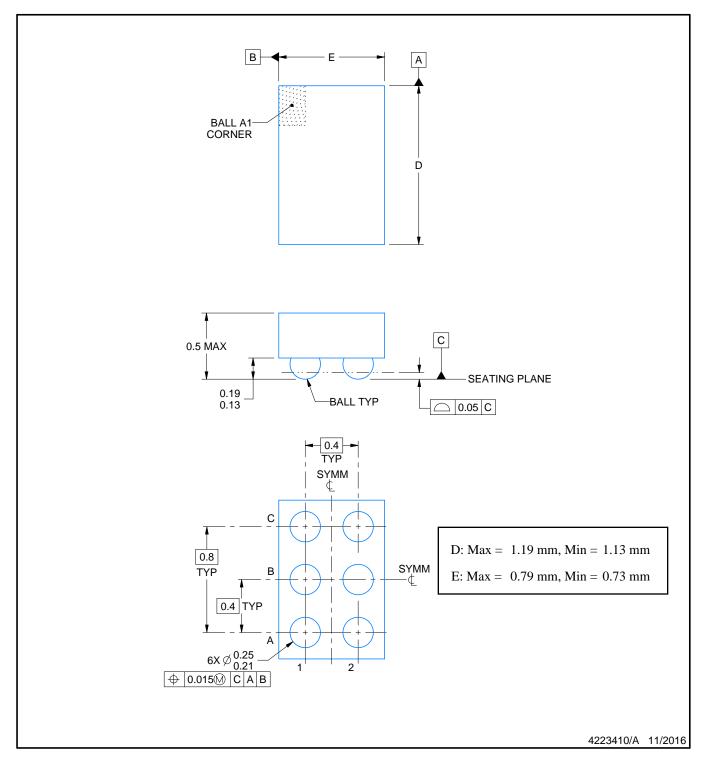


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G07DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP2G07DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AUP2G07DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G07DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP2G07DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G07DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP2G07YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0



DIE SIZE BALL GRID ARRAY

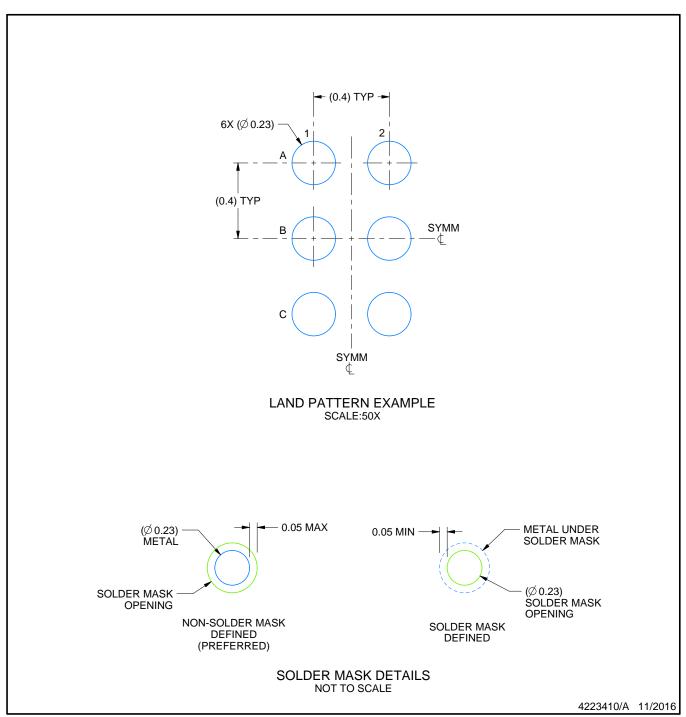


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY

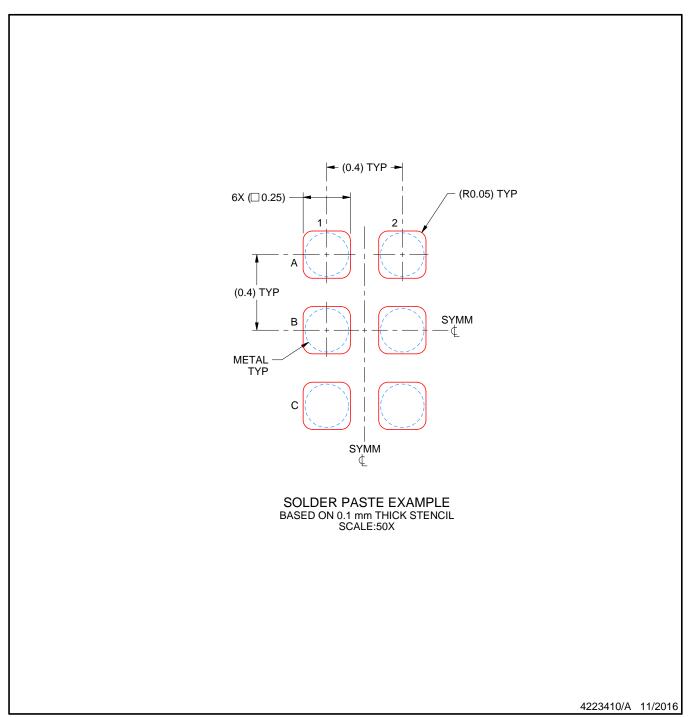


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.





SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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