

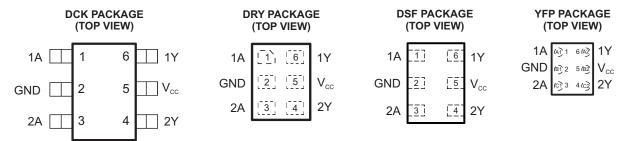
LOW-POWER DUAL INVERTER GATE

Check for Samples: SN74AUP2G04

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption:
 I_{CC} = 0.9 μA Max
- Low Dynamic-Power Consumption:
 C_{pd} = 4.3 pF Typ at 3.3 V
- Low Input Capacitance: C_i = 1.5 pF Typ
- Low Noise: Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V

- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.3 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

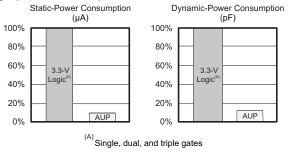


N.C. - No internal connection

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).



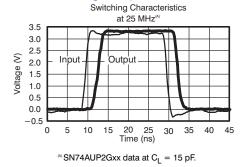


Figure 1. AUP - The Lowest-Power Family

Figure 2. Excellent Signal Integrity

The SN74AUP2G04 performs the Boolean function $Y = \overline{A}$ in positive logic.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



NanoStar[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G04YFPR	HC_
-40°C to 85°C	QFN – DRY	Reel of 5000	SN74AUP2G04DRYR	H4
	uQFN – DSF	Reel of 5000	SN74AUP2G04DSFR	H4
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP2G04DCKR	H4_

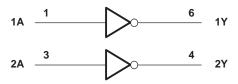
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

 YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

FUNCTION TABLE (Each Inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

LOGIC DIAGRAM (POSITIVE LOGIC)





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage range	Supply voltage range			V	
VI	Input voltage range ⁽²⁾		-0.5	4.6	V	
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state ⁽²⁾	-0.5	4.6	V	
Vo	Output voltage range in the high or low stat	re ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA	
lok	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current			±20	mA	
	Continuous current through V _{CC} or GND			±50	mA	
		DCK package		252		
0	Deal - 1 (3)	DRY package		234	0000	
θ_{JA}	Package thermal impedance (3)	DSF package		300	°C/W	
		YFP package		132		
T _{stg}	Storage temperature range		-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		0.8	3.6	V	
		V _{CC} = 0.8 V	V _{CC}			
V	High level input valtage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		V	
V _{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6		V	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 0.8 \text{ V}$		0		
V	Low lovel input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}	V	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.9		
VI	Input voltage		0	3.6	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 0.8 V		-20	μΑ	
		V _{CC} = 1.1 V		-1.1		
	Himb lavel autout average	V _{CC} = 1.4 V		-1.7		
I _{OH}	High-level output current	V _{CC} = 1.65		-1.9	mA	
		$V_{CC} = 2.3 \text{ V}$		-3.1	1	
		$V_{CC} = 3 V$		-4	İ	
		$V_{CC} = 0.8 \text{ V}$		20	μΑ	
		V _{CC} = 1.1 V		1.1		
	Low lovel output ourrent	$V_{CC} = 1.4 \text{ V}$		1.7 1.9 3.1 4		
l _{OL}	Low-level output current	V _{CC} = 1.65 V				
		V _{CC} = 2.3 V				
		V _{CC} = 3 V				
Δt/Δν	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow of Floating CMOS Inputs, literature number SCBA004.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	T _A	= 25°C	$T_A = -40^{\circ}$	C to 85°C	LINUT		
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP MAX	MIN	MAX	UNIT		
	$I_{OH} = -20 \mu A$	0.8 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1				
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}		$0.7 \times V_{CC}$				
	$I_{OH} = -1.7 \text{ mA}$	1.4 V	1.11		1.03				
	I _{OH} = -1.9 mA	1.65 V	1.32		1.3		V		
V _{OH}	$I_{OH} = -2.3 \text{ mA}$	2.3 V	2.05		1.97		V		
	I _{OH} = -3.1 mA	2.3 V	1.9		1.85				
	$I_{OH} = -2.7 \text{ mA}$	2.1/	2.72		2.67				
	$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55				
	I _{OL} = 20 μA	0.8 V to 3.6 V		0.1		0.1			
	I _{OL} = 1.1 mA	1.1 V		0.3 × V _C	;	$0.3 \times V_{CC}$			
	I _{OL} = 1.7 mA	1.4 V		0.3		0.37	V		
.,	I _{OL} = 1.9 mA	1.65 V		0.3		0.35			
V _{OL}	$I_{OL} = 2.3 \text{ mA}$	2.3 V		0.3		0.33			
	I _{OL} = 3.1 mA	2.3 V		0.44		0.45			
	I _{OL} = 2.7 mA	3 V		0.3		0.33			
	I _{OL} = 4 mA	- 3 V		0.44	Į .	0.45			
A or B input	$V_I = GND \text{ to } 3.6 \text{ V}$	0 V to 3.6 V		0.1		0.5	μА		
off	V_I or $V_O = 0 V$ to 3.6 V	0 V		0.2	2	0.6	μΑ		
ΔI _{off}	V_I or $V_O = 0$ V to 3.6 V	0 V to 0.2 V		0.2	2	0.6	μА		
lcc	$V_I = GND \text{ or } (V_{CC} \text{ to } 3.6 \text{ V}),$ $I_O = 0$	0.8 V to 3.6 V		0.5	5	0.9	μΑ		
ΔI _{CC}	$V_I = V_{CC} - 0.6 V^{(1)}, I_O = 0$	3.3 V		40)	50	μА		
<u> </u>	V – V or CND	0 V		1.5			n.E		
C _i	$V_I = V_{CC}$ or GND	3.6 V		1.5			pF		
C _o	V _O = GND	0 V		3			pF		

⁽¹⁾ One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5 pF$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T,	չ = 25°C	;	$T_A = -40$ °C t	o 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNIT
			0.8 V		18				
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
	A or D	Y	1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
t _{pd}	A or B	Ť	1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	ns
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

Product Folder Link(s): SN74AUP2G04



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T,	4 = 25°C	;	T _A = -40°C t	o 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{cc}	MIN	TYP	MAX	MIN	MAX	UNIT
			0.8 V		21				
			1.2 V ± 0.1 V	1.5	8.5	14.7	1	17.2	
	A == D		1.5 V ± 0.1 V	1	6.2	10	0.5	11.3	20
t _{pd}	A or B	Y	1.8 V ± 0.15 V	1	5	7.7	0.5	9	ns
			2.5 V ± 0.2 V	1	3.6	5.2	0.5	6.1	
			3.3 V ± 0.3 V	1	2.9	4.2	0.5	4.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V _{CC}	T,	4 = 25°C	;	T _A = -40°C t	o 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	UNII
			0.8 V		24				
			1.2 V ± 0.1 V	3.6	9.9	16.3	3.1	19.9	
	A or B		$1.5 \text{ V} \pm 0.1 \text{ V}$	2.3	7.2	11.1	1.8	13.2	20
t _{pd}	AOIB	Ť	1.8 V ± 0.15 V	1.6	5.8	8.7	1.1	10.6	ns
			2.5 V ± 0.2 V	1	4.3	5.9	0.5	7.3	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	3.4	4.8	0.5	5.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V _{cc}	T,	(= 25°C		$T_A = -40$ °C to	85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	UNIT
	0.8 V		32.8						
		Y	1.2 V ± 0.1 V	4.9	13.1	20.9	4.4	25.5	
			1.5 V ± 0.1 V	3.4	9.5	14.2	2.9	16.9	20
t _{pd}	A or B		1.8 V ± 0.15 V	2.5	7.7	11	2	13.5	ns
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.8	5.7	7.6	1.3	9.4	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	4.7	6.2	1	7.5	

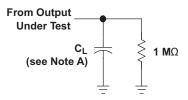
OPERATING CHARACTERISTICS

 $T_{\Delta} = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
			0.8 V	4	
			1.2 V ± 0.1 V	4	
_	Dower discinction conscitones	f = 10 MHz	1.5 V ± 0.1 V	4	~F
C _{pd}	Power dissipation capacitance	T = 10 Min2	1.8 V ± 0.15 V	4	pF
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

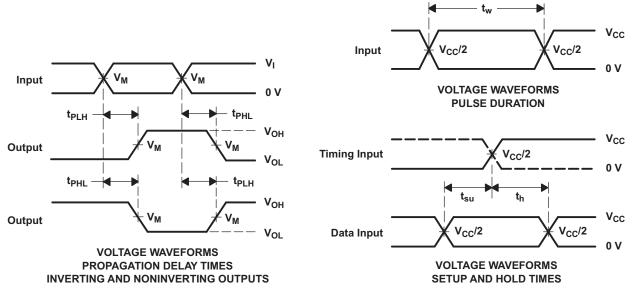


PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V
$egin{array}{c} \mathbf{C_L} \\ \mathbf{V_M} \\ \mathbf{V_I} \end{array}$	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}

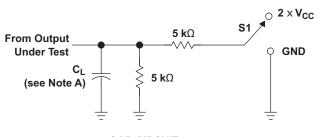


- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, for propagation delays $t_t/t_f = 3$ ns, for setup and hold times and pulse width $t_t/t_f = 1.2$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



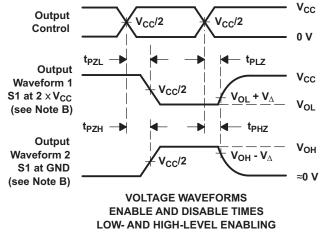
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V \pm 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _∧	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r/t_f = 3$ ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	. ,				. , ,	(4)	(5)		. ,
SN74AUP2G04DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(H45, H4F)
SN74AUP2G04DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(H45, H4F)
SN74AUP2G04DCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4F
SN74AUP2G04DCKRG4.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4F
SN74AUP2G04DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H4
SN74AUP2G04YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HCN
SN74AUP2G04YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HCN

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G04DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP2G04DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUP2G04DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP2G04DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G04DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G04DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G04DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G04YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1



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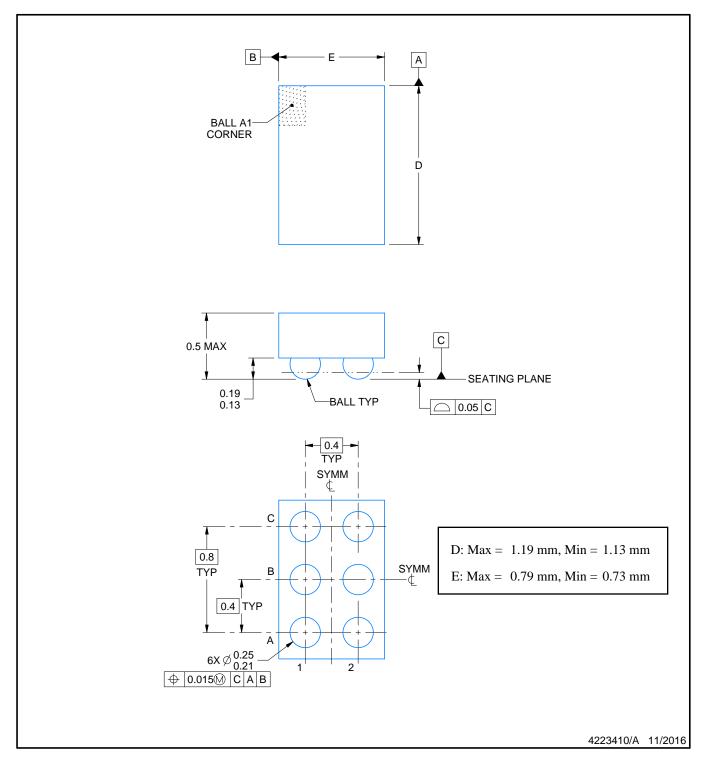


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G04DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AUP2G04DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP2G04DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G04DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G04DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G04DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G04YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0



DIE SIZE BALL GRID ARRAY

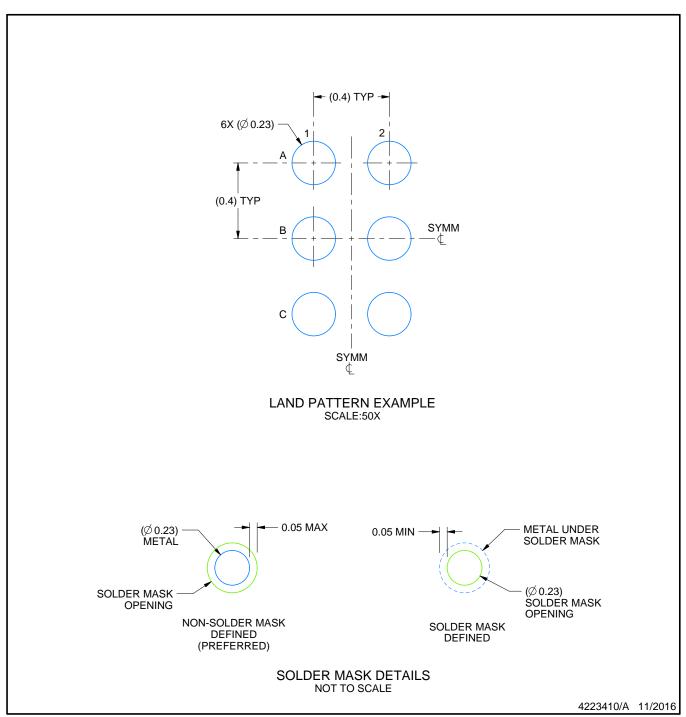


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY

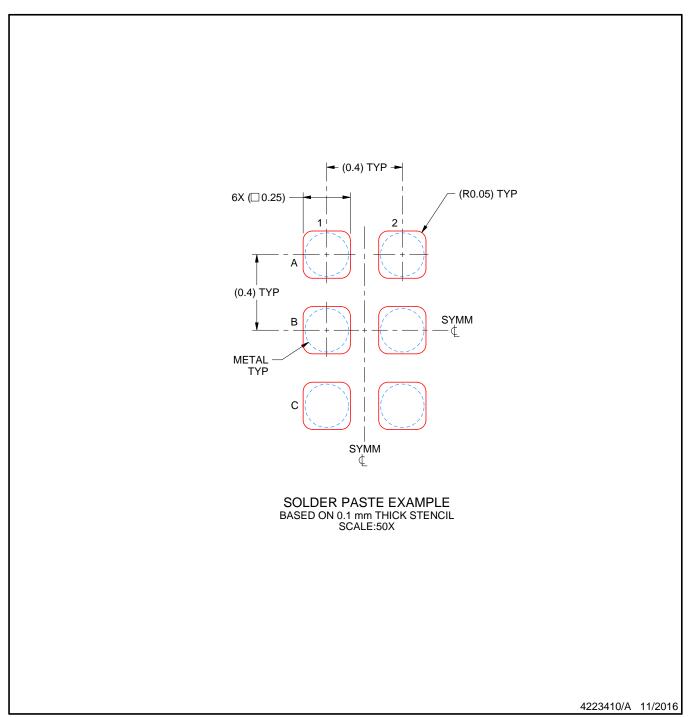


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.





SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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Last updated 10/2025