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SCES614I - OCTOBER 2004-REVISED MAY 2013

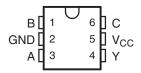
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

Check for Samples: SN74AUP1T98

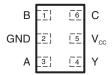
FEATURES

- Available in the Texas Instruments NanoStar™ Packages
- Single-Supply Voltage Translator
- 1.8 V to 3.3 V (at V_{CC} = 3.3 V)
- 2.5 V to 3.3 V (at V_{CC} = 3.3 V)
- 1.8 V to 2.5 V (at V_{CC} = 2.5 V)
- 3.3 V to 2.5 V (at V_{CC} = 2.5 V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial-Power-Down Mode With Low Leakage Current (0.5 μA)
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SOT-23 (DBV), SC-70 (DCK), and WCSP (NanoStar)
- Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Related Devices: SN74AUP1T97, SN74AUP1T57, and SN74AUP1T58

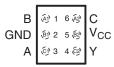
DBV OR DCK PACKAGE (TOP VIEW)



DRY OR DSF PACKAGE (TOP VIEW)



YFP OR YZP PACKAGE (TOP VIEW)



DESCRIPTION

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T98 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply.

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ($\Delta V_T = 210$ mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T98 can be easily configured to perform a required gate function by connecting A, B, and C inputs to V_{CC} or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.

 I_{off} is a feature that allows for powered-down conditions ($V_{\text{CC}} = 0 \text{ V}$) and is important in portable and mobile applications. When $V_{\text{CC}} = 0 \text{ V}$, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

M

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.



The SN74AUP1T98 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	5
2-input NAND gate	6
2-input NOR gate with one inverted input	7
2-input NAND gate with one inverted input	7
2-input NAND gate with one inverted input	8
2-input NOR gate with one inverted input	8
2-input NOR gate	9
Inverter	10
Noninverted buffer	11

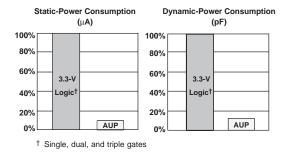


Figure 1. AUP - The Lowest-Power Family

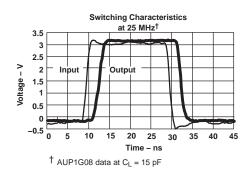


Figure 2. Excellent Signal Integrity



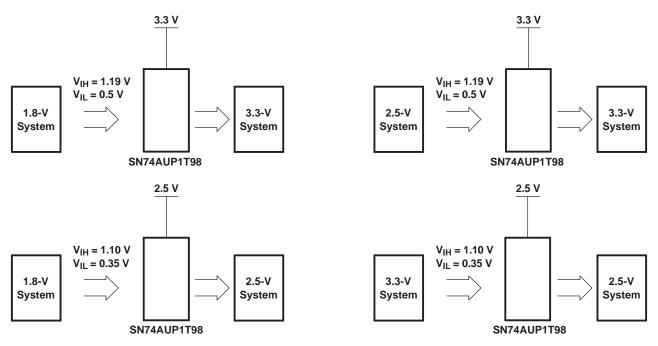


Figure 3. Possible Voltage-Translation Combinations

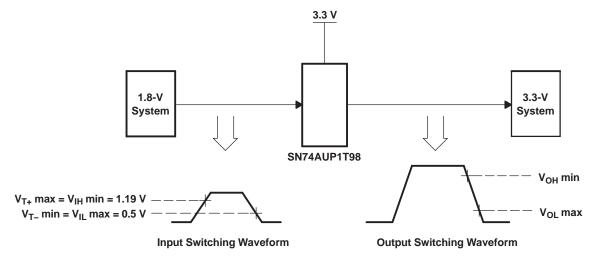


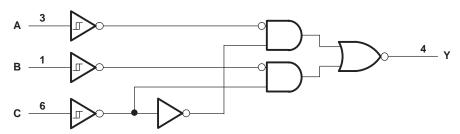
Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation



FUNCTION TABLE

	INPUTS		OUTPUT
С	В	Α	Υ
L	L	L	Н
L	L	Н	Н
L	Н	L	L
L	Н	Н	L
Н	L	L	Н
Н	L	Н	L
Н	Н	L	Н
Н	Н	Н	L

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC CONFIGURATIONS

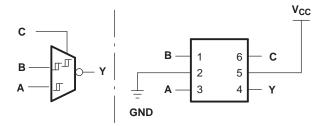


Figure 5. 157+04: 2-to-1 Data Selector With Inverted Output When C is L, Y = $\frac{B}{A}$ When C is H, Y = $\frac{A}{A}$

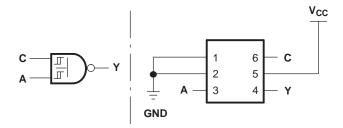


Figure 6. 00: 2-Input NAND Gate



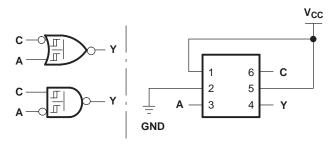


Figure 7. 14+02/14+08: 2-Input NOR Gate With One Inverted Input 2-Input NAND Gate With One Inverted Input

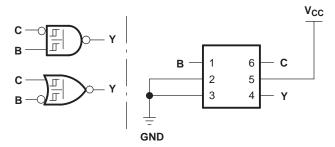


Figure 8. 14+00/14+32: 2-Input NAND Gate With One Inverted Input 2-Input NOR Gate With One Inverted Input

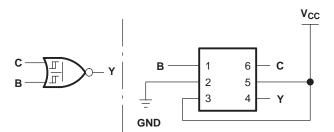


Figure 9. 32: 2-Input NOR Gate

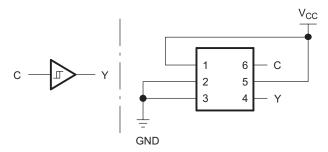


Figure 10. 17/34: Noninverted Buffer

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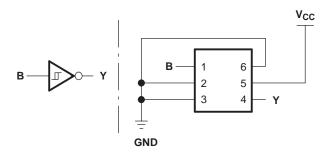


Figure 11. 04/14: Inverter

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-impeda	ance or power-off state ⁽²⁾	-0.5	4.6	V
Vo	Output voltage range in the high or low state ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	•		±20	mA
	Continuous current through V _{CC} or GND			±50	mA
		DBV package		165	
		DCK package		259	
^	Dealth and the arread in an adams (3)	DRY package		340	00/14/
θ_{JA}	Package thermal impedance (3)	DSF package		300	°C/W
		YFP package		123	
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{I}	Input voltage		0	3.6	V
Vo	Output voltage		0	V_{CC}	V
	Llimb lovel output ourrent	$V_{CC} = 2.3 \text{ V}$		-3.1	A
IOH	High-level output current	$V_{CC} = 3 V$		-4	mA
	Low lovel output ourrent	V _{CC} = 2.3 V		3.1	mA
loL	Low-level output current	$V_{CC} = 3 V$		4	IIIA
T_A	Operating free-air temperature	· ·	-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A =	25°C	T _A = -40 to 85°0	°C	UNIT	
			MIN	TYP MAX	MIN	MAX		
V_{T+}		2.3 V to 2.7 V	0.6	1.1	0.6	1.1		
Positive-going input threshold voltage		3 V to 3.6 V	0.75	1.16	0.75	1.19	V	
V _{T-}		2.3 V to 2.7 V	0.35	0.6	0.35	0.6		
Negative-going input threshold voltage		3 V to 3.6 V	0.5	0.85	0.5	0.85	V	
ΔV_T		2.3 V to 2.7 V	0.23	0.6	0.1	0.6		
Hysteresis (V _{T+} – V _{T-})		3 V to 3.6 V	0.25	0.56	0.15	0.56	V	
	I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1			
	$I_{OH} = -2.3 \text{ mA}$	2.3 V	2.05		1.97		V	
V _{OH}	$I_{OH} = -3.1 \text{ mA}$	2.3 V	1.9		1.85			
	$I_{OH} = -2.7 \text{ mA}$	3 V	2.72		2.67			
	$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55			
	$I_{OL} = 20 \mu A$	2.3 V to 3.6 V		0.1		0.1		
	$I_{OL} = 2.3 \text{ mA}$	2.3 V		0.31		0.33		
V _{OL}	$I_{OL} = 3.1 \text{ mA}$	2.5 V		0.44		0.45	V	
	$I_{OL} = 2.7 \text{ mA}$	3 V		0.31		0.33		
	$I_{OL} = 4 \text{ mA}$	3 V		0.44		0.45		
I _I All inputs	$V_I = 3.6 \text{ V or GND}$	0 V to 3.6 V		0.1		0.5	μΑ	
I _{off}	V_I or $V_O = 0$ V to 3.6 V	0 V		0.1		0.5	μΑ	
ΔI_{off}	V_I or $V_O = 3.6 \text{ V}$	0 V to 0.2 V		0.2		0.5	μΑ	
I _{CC}	$V_I = 3.6 \text{ V or GND}, I_O = 0$	2.3 V to 3.6 V		0.5		0.9	μΑ	
ΔI _{CC}	One input at 0.3 V or 1.1 V, Other inputs at 0 or V_{CC} , $I_{O} = 0$	2.3 V to 2.7 V				4	μA	
Δ ,(()	One input at 0.45 V or 1.2 V, Other inputs at 0 or V_{CC} , $I_{O} = 0$	3 V to 3.6 V				12	μΛ	
Ci	$V_I = V_{CC}$ or GND	3.3 V		1.5			pF	
Co	$V_O = V_{CC}$ or GND	3.3 V		3			pF	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM	TO (OUTPUT)	CL	Т,	չ = 25°C		T _A =	40°C 5°C	UNIT	
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX		
		5 pF	1.8	2.3	2.9	0.5	6.8			
	t _{pd} A, B, or C		10 pF	2.3	2.8	3.4	1	7.9	no	
^l pd		Ť	Ť	15 pF	2.6	3.1	3.8	1	8.7	ns
			30 pF	3.8	4.4	5.1	1.5	10.8		

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_{I} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T	(= 25°C		T _A = -	40°C 5°C	UNIT
	(INFOT)	(001701)		MIN	TYP	MAX	MIN	MAX	
		5 pF	1.8	2.3	3.1	0.5	6		
	t _{pd} A, B, or C	Y	10 pF	2.2	2.8	3.5	1	7.1	
^l pd			Y	15 pF	2.6	3.2	5.2	1	7.9
			30 pF	3.7	4.4	5.2	1.5	10	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM TO		CL	T,	_{\(\)} = 25°C		T _A = -	40°C 5°C	UNIT								
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX									
		5 pF	2	2.7	3.5	0.5	5.5										
	A B or C		10 pF	2.4	3.1	3.9	1	6.5									
t _{pd}	A, B, or C	Y	Ť	Y	Y	Y	Y	Y	Y	Y	15 pF	2.8	3.5	4.3	1	7.4	ns
		30 pF	4	4.7	5.5	1.5	9.5										

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL	T,	_{\(\)} = 25°C		T _A = -	40°C 5°C	UNIT
	(INFOT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	
		Υ	5 pF	1.6	2	2.5	0.5	8	
			10 pF	2	2.4	2.9	1	8.5	
t _{pd} A, B, or C	Y		15 pF	2.3	2.8	3.3	1	9.1	ns
			30 pF	3.4	3.9	4.4	1.5	9.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM	TO (OUTPUT)	PUT)	T	_ = 25°C		T _A = -		UNIT
	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	
		V	5 pF	1.6	1.9	2.4	0.5	5.3	
			V	10 pF	2	2.3	2.7	1	6.1
t _{pd} A, B, or C	T	15 pF	2.3	2.7	3.1	1	6.8	ns	
			30 pF	3.4	3.8	4.2	1.5	8.5	



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 12)

PARAMETER	FROM	TO CL	T,	_A = 25°C	;	T _A = -	40°C 5°C	UNIT	
	(INPUT)	(OUTPUT)	101)	MIN	TYP	MAX	MIN	MAX	
	A.D. 0		5 pF	1.6	2.1	2.7	0.5	4.7	
		V	10 pF	2	2.4	3	1	5.7	
t _{pd}	A, B, or C	Y	15 pF	2.3	2.7	3.3	1	6.2	ns
			30 pF	3.4	3.8	4.4	1.5	7.8	

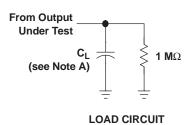
OPERATING CHARACTERISTICS

 $T_A = 25$ °C

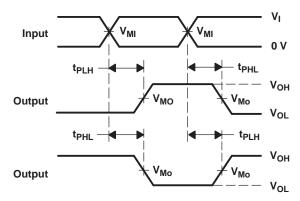
	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	4	5	pF



PARAMETER MEASUREMENT INFORMATION



	V _{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V \pm 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _{MI}	V _I /2	V _I /2
V _{MO}	V _{CC} /2	V _{CC} /2



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, slew rate \geq 1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 12. Load Circuit and Voltage Waveforms

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REVISION HISTORY

Changes from Revision H (May 2010) to Revision I						
•	Updated FUNCTION SELECTION Table.	2				
•	Updated figure caption	5				
•	Updated figure caption	5				

Submit Documentation Feedback

5-Nov-2025

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	. ,	.,			. ,	(4)	(5)		. ,
SN74AUP1T98DBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R
SN74AUP1T98DBVR.B	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R
SN74AUP1T98DBVT	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R
SN74AUP1T98DBVT.B	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R
SN74AUP1T98DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	TKR
SN74AUP1T98DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TKR
SN74AUP1T98DCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR
SN74AUP1T98DCKRG4.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR
SN74AUP1T98DCKT	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR
SN74AUP1T98DCKT.B	Active	Production	SC70 (DCK) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR
SN74AUP1T98DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK
SN74AUP1T98DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK
SN74AUP1T98DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK
SN74AUP1T98DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T98DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T98DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T98DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DCKRG4	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T98DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T98DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T98DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T98DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T98DCKRG4	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T98DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1T98DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T98DSFR	SON	DSF	6	5000	210.0	185.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.









NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.





NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).





NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.





NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).





4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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