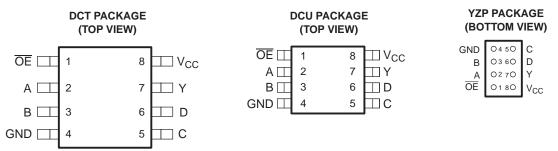
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FEATURES

- Available in the Texas Instruments
 NanoFree[™] Package
- Low Static-Power Consumption (I_{CC} = 0.9 μA Max)
- Low Dynamic-Power Consumption (C_{nd} = 5 pF Typ at 3.3 V)
- Low Input Capacitance (C_I = 1.5 pF)
- Low Noise Overshoot and Undershoot <10% of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs

- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 7.4 ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).

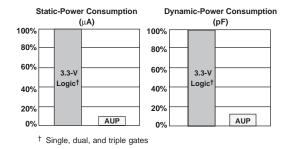


Figure 1. AUP - The Lowest-Power Family

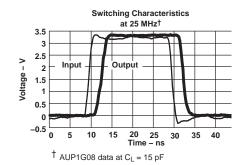


Figure 2. Excellent Signal Integrity

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

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DESCRIPTION/ORDERING INFORMATION

The SN74AUP1G99 features configurable multiple functions with a 3-state output. This device has the input-disable feature, which allows floating input signals. The inputs and output are disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, the output state is determined by 16 patterns of 4-bit input. The user can choose the logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching noise immunity at the input.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar[™] and NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AUP1G99YZPR	HY_
	SSOP - DCT	Tape and reel	SN74AUP1G99DCTR	H99
	VSSOP – DCU	Tape and reel	SN74AUP1G99DCUR	H99_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

 DCU: The actual top-side marking has one additional character that designates the assembly/test site.

 YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

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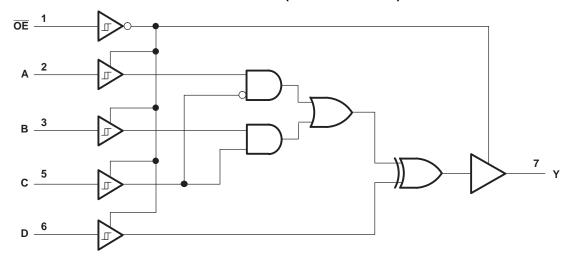


FUNCTION TABLE

		INPUTS			OUTPUT
ŌĒ	D	С	В	Α	Υ
L	L	L	L	L	L
L	L	L	L	Н	Н
L	L	L	Н	L	L
L	L	L	Н	Н	Н
L	L	Н	L	L	L
L	L	Н	L	Н	L
L	L	Н	Н	L	Н
L	L	Н	Н	Н	Н
L	Н	L	L	L	Н
L	Н	L	L	Н	L
L	Н	L	Н	L	Н
L	Н	L	Н	Н	L
L	Н	Н	L	L	Н
L	Н	Н	L	Н	Н
L	Н	Н	Н	L	L
L	Н	Н	Н	Н	L
Н	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	Z

(1) Floating inputs allowed.

LOGIC DIAGRAM (POSITIVE LOGIC)



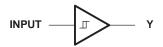
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FUNCTION SELECTION TABLE

PRIMARY FUNCTION	COMPLEMENTARY FUNCTION	PAGE
3-state buffer		4
3-state inverter		4
3-state 2-to-1 data selector MUX		5
3-state 2-to-1 data selector MUX, inverted out		5
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	5
3-state 2-input AND, 1 input inverted	3-state 2-input NOR, 1 input inverted	5
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	5
3-state 2-input NAND	3-state 2-input OR, both inputs inverted	6
3-state 2-input NAND, 1 input inverted	3-state 2-input OR, 1 input inverted	6
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	6
3-state 2-input XOR		6
3-state 2-input XNOR	3-state 2-input XOR, 1 input inverted	7

3-STATE BUFFER FUNCTIONS AVAILABLE



FUNCTION	ŌĒ	Α	В	С	D
	L	Input	X	L	L
		X	Input	Н	L
		L	Н	Input	L
3-state buffer		Н	L	Input	Н
		Н	X	L	Input
		X	L	Н	Input
		L	L	X	Input

3-STATE INVERTER FUNCTIONS AVAILABLE



FUNCTION	ŌĒ	Α	В	С	D
		Input	X	L	Н
		X	Input	Н	Н
	L	L	Н	Input	Н
3-state inverter		Н	L	Input	L
		Н	X	L	Input
		X	Н	Н	Input
		Н	Н	X	Input

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SN74AUP1G99 LOW-POWER ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

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3-STATE MUX FUNCTIONS AVAILABLE



FUNCTION	ŌĒ	Α	В	С	D
3-state 2-to-1, data selector MUX		Input 1	Input 2	Input 1 or Input 2	L
3-state 2-to-1, data selector MUX		Input 2	Input 1	Input 2 or Input 1	L
3-state 2-to-1, data selector MUX, inverted out	L	Input 1	Input 2	Input 1 or Input 2	Н
3-state 2-to-1, data selector MUX, inverted out		Input 2	Input 1	Input 2 or Input 1	Н

3-STATE AND/NOR FUNCTIONS AVAILABLE



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state AND	3-state NOR, both inputs inverted		L	Input 1	Input 2	L
2	3-state AND	3-state NOR, both inputs inverted	L	L	Input 2	Input 1	L



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state AND, with A inverted	3-state NOR, with B inverted		Input 2	L	Input 1	L
2	3-state AND, with A inverted	3-state NOR, with B inverted	L	Н	Input 1	Input 2	Н



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state AND, with B inverted	3-state NOR, with A inverted		Input 1	L	Input 2	L
2	3-state AND, with B inverted	3-state NOR, with A inverted	L	Н	Input 2	Input 1	Н



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	ပ	D
2	3-state AND, both inverted inputs	3-state NOR		Input 1	Н	Input 2	Н
2	3-state AND, both inverted inputs	3-state NOR	L	Input 2	H	Input 1	Н

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3-STATE NAND/OR FUNCTIONS AVAILABLE



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state NAND	3-state OR, with both inputs inverted		L	Input 1	Input 2	Н
2	3-state NAND	3-state OR, with both inputs inverted	L	L	Input 2	Input 1	Н



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state NAND, with A inverted	3-state OR, with B inverted		Input 2	L	Input 1	Ι
2	3-state NAND, with A inverted	3-state OR, with B inverted	L	Н	Input 1	Input 2	L

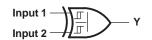


NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state NAND, with B inverted	3-state OR, with A inverted		Input 1	L	Input 2	Н
2	3-state NAND, with B inverted	3-state OR, with A inverted	L	Н	Input 2	Input 1	L



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	ŌĒ	Α	В	С	D
2	3-state NAND, with both inputs inverted	3-state OR		Input 1	Н	Input 2	L
2	3-state NAND, with both inputs inverted	3-state OR	L	Input 2	Н	Input 1	L

3-STATE XOR/XNOR FUNCTIONS AVAILABLE



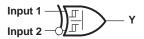
FUNCTION	ŌĒ	Α	В	С	D
		Input 1	X	L	Input 2
		Input 2	X	L	Input 1
3-state XOR		X	Input 1	Н	Input 2
3-state AUR	L	Х	Input 2	Н	Input 1
		L	Н	Input 1	Input 2
		L	Н	Input 2	Input 1

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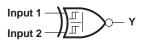
3-STATE XOR/XNOR FUNCTIONS AVAILABLE (continued)



FUNCTION	ŌĒ	Α	В	С	D
3-state XOR, with A inverted	L	Н	L	Input 1	Input 2



FUNCTION	ŌĒ	Α	В	С	D
3-state XOR, with B inverted	L	Н	Ш	Input 1	Input 2



FUNCTION	ŌĒ	Α	В	С	D
3-state XNOR		Н	L	Input 1	Input 2
3-state XNOR	L	Н	L	Input 2	Input 1

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range (2)		-0.5	4.6	V
Vo	Voltage range applied to any output in the high-	impedance or power-off state (2)	-0.5	4.6	V
Vo	Output voltage range in the high or low state ⁽²⁾		-0.5 V	' _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND			±50	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (3)	DCU package		227	°C/W
		YZP package		102	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.



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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	3.6	V
V_{I}	Input voltage		0	3.6	V
Vo	Output voltage	Active state	0	V_{CC}	V
v O	Output voltage	3-state	0	3.6	V
		$V_{CC} = 0.8 \text{ V}$		-20	μΑ
		V _{CC} = 1.1 V		-1.1	
	High-level output current	V _{CC} = 1.4 V		-1.7	
I _{OH}	nigh-level output current	V _{CC} = 1.65 V		-1.9	mA
		$V_{CC} = 2.3 \text{ V}$		-3.1	
		$V_{CC} = 3 V$		-4	
		V _{CC} = 0.8 V		20	μΑ
		V _{CC} = 1.1 V		1.1	
	Low lovel output ourrent	V _{CC} = 1.4 V		1.7	
l _{OL}	Low-level output current	V _{CC} = 1.65 V		1.9	mA
		$V_{CC} = 2.3 \text{ V}$		3.1	
		V _{CC} = 3 V		4	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	T,	_A = 25°C	T _A =	°C MAX 0.6 0.9 1.11 1.29 1.77 2.29 0.6 0.65 0.75 0.84 1.04 1.24 0.5 0.46 0.56 0.66 0.92 1.31 0.1 0.3 × V _{CC} 0.37 0.35 0.33 0.45 0.33 0.45 0.56	UNIT	
			MIN	TYP MAX	MIN	MAX		
		0.8 V	0.3	0.6	0.3	0.6		
V		1.1 V	0.53	0.9	0.53	0.9		
v _{T+} Positive-going		1.4 V	0.74	1.11	0.74	1.11	.,	
input threshold		1.65 V	0.91	1.29	0.91	1.29	V	
voltage		2.3 V	1.37	1.77	1.37	1.77		
		3 V	1.88	2.29	1.88	2.29		
		0.8 V	0.1	0.6	0.1	0.6		
		1.1 V	0.26	0.65	0.26	0.65		
V _T _ Negative-going		1.4 V	0.39	0.75	0.39	0.75	.,	
input threshold		1.65 V	0.47	0.84	0.47	0.84	V	
voltage		2.3 V	0.69	1.04	0.69	1.04	-	
		3 V	0.88	1.24	0.88	1.24	-	
		0.8 V	0.07	0.5	0.07	0.5		
		1.1 V	0.08	0.46	0.08	0.46		
$V_{T-} \\ V_{T-} \\ V_{CA} \\ V$			0.18		0.18	0.56		
	0.27	0.66	V					
(V + - V -)		NS						
		3 V	0.79		0.79	1.31	_	
	I _{OH} = -20 μA							
							Ì	
				1.29	-			
V _{OH}			2.05		1.97		V	
		2.3 V					-	
		3 V						
		0.8 V to 3.6 V		0.1		0.1		
							-	
							-	
V _{T+} Positive-going input threshold voltage 1.1 V 0.53 0.9 0.53 Positive-going input threshold voltage 1.65 V 0.91 1.29 0.91 V _{T-} Negative-going input threshold voltage 0.8 V 0.1 0.6 0.1 V _{T-} Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 Negative-going input threshold voltage 1.65 V 0.47 0.84 0.47 VOL 1.65 V 0.47 0.88 0.07 0.07 0.07 0.07 0.07		V						
		2.3 V				53	-	
							-	
		3 V					-	
		0 V to 3.6 V					μА	
	V_1 or $V_0 = 0 \text{ V}$ to 3.6 V	0 V		0.2		0.6	μA	
Icc	$V_I = GND \text{ or } (V_{CC} \text{ to } 3.6 \text{ V}),$							



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Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARA	PARAMETER TEST CONDITIONS		V _{CC}	T _A = 25°C		T _A = -40°C to 85°C		UNIT	
				MIN	TYP	MAX	MIN	MAX	
	Data inputs	$V_1 = V_{CC} - 0.6 \text{ V},^{(1)} I_O = 0$	3.3 V			40		50	μА
ΔI_{CC}	ŌĒ				110			120	
	All inputs	$V_I = GND \text{ to } 3.6 \text{ V}, \overline{OE} = V_{CC}^{(2)}$	0.8 V to 3.6 V		0				nA
C		V – V or CND	0 V		1.5				nE.
C _I	$V_{l} = V_{CC} \text{ or GND}$		3.6 V		1.5				pF
Co		$V_O = V_{CC}$ or GND	3.6 V		3				pF

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 5 pF$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	Т,	ղ = 25°C		T _A = -40°C to 85°C		UNIT
		(001701)		MIN	TYP	MAX	MIN	MAX	
			0.8 V		32				
			1.2 V ± 0.1 V	0.5	9.9	20.1	0.5	26.6	
t _{pd}	A D C 0" D	Y	1.5 V ± 0.1 V	1.4	6.6	11.9	0.5	16.8	20
	A, B, C, or D	ř	1.8 V ± 0.15 V	1.8	5.3	8.9	1	13	ns
			2.5 V ± 0.2 V	2.1	3.9	5.8	1.3	8.9	
			3.3 V ± 0.3 V	1.9	3.3	4.8	1.2	7.4	ı
	ŌĒ	Y	0.8 V		35				6.4 2.8
			1.2 V ± 0.1 V	0.6	11.1	21.7	0.5	25.2	
			1.5 V ± 0.1 V	2.3	7.4	12.6	1.4	16.4	
t _{en}			1.8 V ± 0.15 V	2	5.7	9.4	1.1	12.8	
			2.5 V ± 0.2 V	2.1	4.1	6.2	1.2	8.5	
			3.3 V ± 0.3 V	1.9	3.4	5	1.1	6.7	
			0.8 V		9.8				
			1.2 V ± 0.1 V	1.4	4.5	7.7	1.5	8.2	
	ŌĒ	Y	1.5 V ± 0.1 V	1.7	3.2	4.8	1.7	6	ns
t _{dis}	OE .	Y	1.8 V ± 0.15 V	1.5	3	4.7	1.3	6.1	
			2.5 V ± 0.2 V	0.9	1.9	3	0.7	4.2	
			3.3 V ± 0.3 V	0.8	2.5	4.4	0.7	4.5	

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 $[\]begin{array}{ll} \hbox{(1)} & \hbox{One input at $V_{CC}-0.6$ V, other input at V_{CC} or GND \\ \hbox{(2)} & \hbox{To show I_{CC} is very low when the input-disable feature is enabled.} \end{array}$



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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	Т,	չ = 25°C		T _A = -40°C to 85°C		UNIT
		(001701)		MIN	TYP	MAX	MIN	MAX	
			0.8 V		36				
			1.2 V ± 0.1 V	0.4	10.7	21.1	0.7	29.8	
	A B C or D	Y	1.5 V ± 0.1 V	2	7.2	12.6	1.1	18.5	
t _{pd}	A, B, C, or D	ř	1.8 V ± 0.15 V	2.3	5.8	9.5	1.5	14.5	ns
			2.5 V ± 0.2 V	2.5	4.4	6.3	1.7	10.5	
			3.3 V ± 0.3 V	2.3	3.7	5.2	1.5	8.4	4
	ŌĒ	Y	0.8 V		0				
			1.2 V ± 0.1 V	1.4	12.1	22.8	0.8	29.3	8.7 4.8
			1.5 V ± 0.1 V	2.8	8	13.3	2	18.7	
t _{en}			1.8 V ± 0.15 V	2.5	6.2	10	1.6	14.8	
			2.5 V ± 0.2 V	2.5	4.5	6.7	1.6	9.9	
			3.3 V ± 0.3 V	2.3	3.8	5.4	1.5	8.2	
			0.8 V		0				
			1.2 V ± 0.1 V	2	5.6	9.3	2	10	
	ŌĒ	V	1.5 V ± 0.1 V	2.5	4.1	5.8	2.4	7.6	20
t _{dis}	OE .	Y	1.8 V ± 0.15 V	2.9	4.2	5.7	2.7	7.9	ns
			2.5 V ± 0.2 V	1.1	2.7	4.4	1.1	5.5	
			3.3 V ± 0.3 V	1.9	3.5	5.2	1.9	5.8	

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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	TO (OUTPUT)	V _{cc}	Т,	λ = 25°C		T _A = -40°C to 85°C		UNIT				
	(INPUT)	(001701)		MIN	TYP	MAX	MIN	MAX	ļ				
		_		0.8 V		38							
				1.2 V ± 0.1 V	0.9	11.4	22	0.5	30.8				
	A B C or D	Y	1.5 V ± 0.1 V	2.5	7.8	13.2	1.6	19.2					
t _{pd}	A, B, C, or D	Ť	1.8 V ± 0.15 V	2.7	6.3	10	1.9	15.1	ns				
			2.5 V ± 0.2 V	2.8	4.7	6.6	2	10.8					
			3.3 V ± 0.3 V	2.6	4	5.5	1.8	8.8					
	ŌĒ		0.8 V		44								
		Y	1.2 V ± 0.1 V	1.8	13	24.2	1.3	30.6	30.6 19.5 15.4 10.3				
			1.5 V ± 0.1 V	3.2	8.6	14.1	2.4	19.5					
t _{en}			1.8 V ± 0.15 V	2.9	6.7	10.6	2	15.4					
			2.5 V ± 0.2 V	2.8	4.9	7	1.9	10.3					
			3.3 V ± 0.3 V	2.6	4.1	5.7	1.8	8.6					
			0.8 V		13								
			1.2 V ± 0.1 V	2.7	6.3	9.9	2.8	10.7					
t _{dis}	or	Y	1.5 ± 0.1 V	3.2	4.6	6.1	3.1	8	20				
	ŌĒ	Y	1.8 V ± 0.15 V	3.2	4.8	6.6	3	8.8	ns				
		ı					2.5 V ± 0.2 V	2.2	3.4	4.7	2	6	
			3.3 V ± 0.3 V	2.4	4.4	6.5	2.3	7.2					

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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	TO (OUTPUT)	V _{cc}	T _A - 25°C			T _A = -40°C to 85°C		UNIT			
	(INPUT)	(001701)		MIN	TYP	MAX	MIN	MAX				
			0.8 V		48							
			1.2 V ± 0.1 V	3.1	14	24.9	2.6	36.1				
	A D C or D	Y	1.5 V ± 0.1 V	4.2	9.6	15.1	3.3	23.1				
t _{pd}	A, B, C, or D	ř	1.8 V ± 0.15 V	4.1	7.9	11.7	3.3	18	ns			
			2.5 V ± 0.2 V	4.1	5.9	7.9	3.1	12.7				
			3.3 V ± 0.3 V	3.7	5.1	6.7	2.8	10.4	+			
	ŌĒ	Y	0.8 V		50							
			1.2 V ± 0.1 V	4.4	16	27.6	3.9	36.8	ns			
			1.5 V ± 0.1 V	5.3	10.7	16.2	4.3	23.6				
t _{en}			1.8 V ± 0.15 V	4.6	8.5	12.4	3.6	18.6				
			2.5 V ± 0.2 V	4.2	6.3	8.5	3.2	12.6				
			3.3 V ± 0.3 V	3.8	5.4	7.1	2.9	10.2				
			0.8 V		19							
			1.2 V ± 0.1 V	6	10.1	14.2	6	14.6				
	0.	V	1.5 V ± 0.1 V	5.1	7.4	10.6	5	10.1				
t _{dis}	ŌĒ	Y	Y	Y	Y	1.8 V ± 0.15 V	5.5	8.6	11.6	5.5	12.1	ns
							2.5 V ± 0.2 V	3.3	5.9	8.3	3.3	8.9
			3.3 V ± 0.3 V	6	8.7	10.9	5.9	11.8				

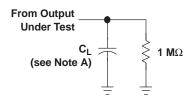
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
				0.8 V	4	
				1.2 ± 0.1 V	4	
		Outputs enabled		1.5 ± 0.1 V	4	
		Outputs enabled		1.8 V ± 0.15 V	4	
			f = 10 MHz	$2.5 \text{ V} \pm 0.2 \text{ V}$	5	pF
	Dower dissination consistence			$3.3 \text{ V} \pm 0.3 \text{ V}$	5	
C _{pd}	Power dissipation capacitance		I = IO WINZ	0.8 V	0	
				1.2 ± 0.1 V	0	
		Outputs disabled		1.5 ± 0.1 V	0	
		Outputs disabled		1.8 V ± 0.15 V	0	
				$2.5 \text{ V} \pm 0.2 \text{ V}$	0	
				3.3 V ± 0.3 V	0	

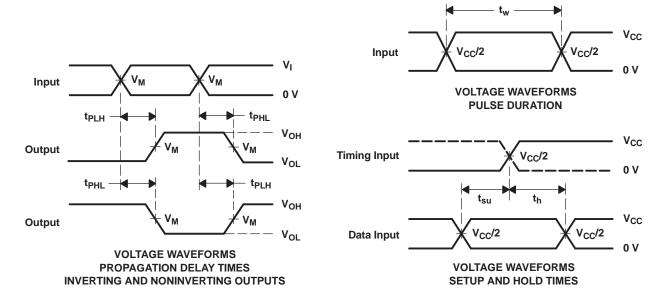


PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}



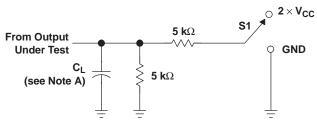
NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, for propagation delays $t_f/t_f = 3$ ns, for setup and hold times and pulse width $t_f/t_f = 1.2$ ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



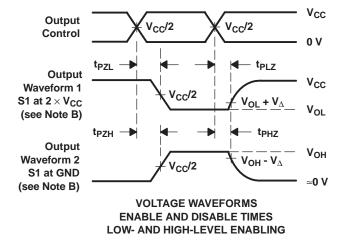
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S 1
t _{PLZ} /t _{PZL}	2×V _{CC}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _∆	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f/t_f = 3~ns$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74AUP1G99DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(2XG5, H99) (R, Z)
SN74AUP1G99DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XG5, H99) (R, Z)
SN74AUP1G99DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(2XG5, H99) (R, Z)
SN74AUP1G99DCTT.B	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2XG5, H99) (R, Z)
SN74AUP1G99DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(H99Q, H99R)
SN74AUP1G99DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H99Q, H99R)
SN74AUP1G99DCUR1G4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 85	
SN74AUP1G99DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(H99Q, H99R)
SN74AUP1G99DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H99Q, H99R)
SN74AUP1G99YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HYN
SN74AUP1G99YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HYN

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS KO P1 BO W Cavity A0

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G99DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUP1G99DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G99YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G99DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUP1G99DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G99DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G99DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74AUP1G99YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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