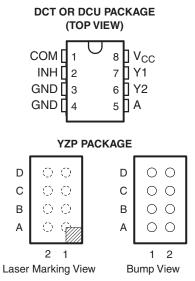
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SCES484C-AUGUST 2003-REVISED JANUARY 2009

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Operates at 0.8 V to 2.7 V
- Sub-1-V Operable
- Low Power Consumption, 10 μA at 2.7 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



YZP TERMINAL ASSIGNMENTS

D	GND	Α
С	GND	Y2
В	INH	Y1
Α	COM	V _{cc}
	1	2

DESCRIPTION/ORDERING INFORMATION

This analog switch is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.



ORDERING INFORMATION

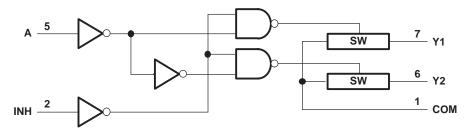
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING (3)
	NanoFree [™] – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G53YZPR	U4_
-40C to 85C	SSOP - DCT	Reel of 3000	SN74AUC2G53DCTR	U53
	VSSOP – DCU	Reel of 3000	SN74AUC2G53DCUR	U53_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

FUNCTION TABLE

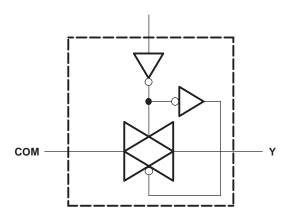
CONT		ON CHANNEL
INH	Α	CHANNEL
L	L	Y1
L	Н	Y2
Н	Χ	None

LOGIC DIAGRAM (POSITIVE LOGIC)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals may be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

SIMPLIFIED SCHEMATIC, EACH SWITCH (SW)



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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range (2)		-0.5	3.6	V
VI	Input voltage range (2)(3)		-0.5	3.6	V
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Control input clamp current	V _I < 0		-50	mA
I _{I/OK}	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		50	mA
I _T	On-state switch current current	$V_{I/O} = 0$ to V_{CC}		50	mA
	Continuous current through V _{CC} or GND			100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (4)	DCU package		227	C/W
		YZP package		102	
T _{stg}	Storage temperature range		-65	150	С

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	0.65 טV _{CC}		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		V _{CC} = 0.8 V		0	
V_{IL}	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		0.35 V _{CC}	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
V _{I/O}	I/O port voltage		0	V_{CC}	V
VI	Control input voltage		0	3.6	V
		V _{CC} = 0.8 V to 1.6 V		20	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 1.65 V to 1.95 V		10	ns/V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		3.5	
T _A	Operating free-air temperature		-40	85	С

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITION	V _{cc}	MIN TYP(1)	MAX	UNIT	
		$V_I = V_{CC}$ or GND,	$I_S = 4 \text{ mA}$	1.1 V		40	
r _{on}	Ton On-State Switch resistance	V _{INH} = V _{IL} I _S = 4 (see Figure 1 and		1.65 V	12.5	20	Ω
		Figure 2)	$I_S = 8 \text{ mA}$	2.3 V	6	15	
		$V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 1 and	I _S = 4 mA	1.1 V	131	180	
r _{on(p)}	Peak on resistance			1.65 V	32	80	Ω
			$I_S = 8 \text{ mA}$	2.3 V	15	20	

(1) $T_A = 25C$

⁽²⁾ All voltages are with respect to ground unless otherwise specified.

³⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIO	NS	V _{CC}	MIN TYP ⁽¹⁾ MAX	UNIT
			$V_I = V_{CC}$ to GND,	$I_S = 4 \text{ mA}$	1.1 V	4	
Δr_{on}	Difference of on-state resistance between switches		$V_C = V_{IH}$ (see Figure 1 and	IS = 4 IIIA	1.65 V	1	Ω
	201110011011101100		Figure 2)		2.3 V	1	
			$V_I = V_{CC}$ and $V_O = GND$, or			1	
I _{S(off)}	Off-state switch leakage current		$V_I = GND$ and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		2.7 V	0.1 (1)	μА
	On-state switch leakage current		$V_I = V_{CC}$ or GND, $V_{INH} = V_I$	L,	2.7 V	1	
I _{S(on)}	On-state switch leakage current		V _O = Open (see Figure 4)		2.7 V	0.1 ⁽¹⁾	μΑ
I _I	Control input current		$V_C = V_{CC}$ or GND		2.7 V	5	μΑ
I _{CC}	Supply current		$V_C = V_{CC}$ or GND		2.7 V	10	μΑ
C _{ic}	Control input capacitance				2.5 V	2	pF
C	Switch input/output capacitance	Υ			2.5 V	3	nE
C _{io(off)}	Cio(off) Switch input/output capacitance				2.3 V	4.5	pF
C _{io(on)}	Switch input/output capacitance				2.5 V	9	pF

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM TO (OUTPUT)		V _{CC} = 0.8 V			V _{CC} = 1.5 V 0.1 V		V _{CC} = 1.8 V 0.15 V		V	V _{CC} = 2.5 V 0.2 V		UNIT
		(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd} ⁽¹⁾	COM or Y	Y or COM	0.3		0.3		0.3			0.2		0.1	ns
t _{en}	INILI	NIII OOM aa V	9.2	0.5	3.5	0.5	2.2	0.5	1	1.9	0.5	1.8	
t _{dis}	INH	COM or Y	8.1	0.5	4.2	0.5	3.2	0.5	1.9	3.4	0.5	2.6	ns
t _{en}	A COM or	COM or Y	9.2	0.5	3.6	0.5	2.3	0.5	1.1	1.9	0.5	1.6	
t _{dis}	А	COIVI OF Y	10	0.5	3.6	0.5	2.3	0.5	1.1	2	0.5	1.6	ns

⁽¹⁾ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO	V _{CC} = 1.8 V 0.15 V			V _{CC} = 2.5 V 0.2 V		UNIT
		(OUTPUT)	MIN	TYP	MAX	MIN	MAX	
t _{pd} ⁽¹⁾	COM or Y	Y or COM			0.4		0.2	ns
t _{en}	INILI	COM or Y	0.5	1.6	3.1	0.5	2.2	no
t _{dis}	INH		0.5	2.2	3.4	0.5	2.2	ns
t _{en}	۸	COM or V	0.5	1.6	3	0.5	2.2	
t _{dis}	A	COM or Y	0.5	1.6	3	0.5	2.3	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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Analog Switch Characteristics

 $T_A = 25C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	TYP	UNIT
				0.8 V	90	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	101	
			f _{in} = sine wave	1.4 V	110	
			(see Figure 6)	1.65 V	122	
Frequency response ⁽¹⁾	COM or Y	Y or COM		2.3 V	198	MHz
(switch ON)	CONTOL			V 8.0	>500	IVIITZ
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	1.1 V	>500	
			f _{in} = sine wave	1.4 V	>500	
			(see Figure 6)	1.65 V	>500	
				2.3 V	>500	
				0.8 V	-59	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	-59	dB
		Y or COM	f _{in} = 1 MHz (sine wave)	1.4 V	-59	
			(see Figure 7)	1.65 V	-59	
Crosstalk ⁽²⁾ between switches)	COM an V			2.3 V	-60	
	COM or Y			0.8 V	-55	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	1.1 V	-55	
			f _{in} = 1 MHz (sine wave)	1.4 V	-55	
			(see Figure 7)	1.65 V	-55	
				2.3 V	-55	
				0.8 V	0.56	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	0.68	
Crosstalk (control input to signal output)	INH	COM or Y	f _{in} = 1 MHz (square wave)	1.4 V	0.81	mV
(control input to signal output)			(see Figure 8)	1.65 V	0.93	
				2.3 V	1.5	
				0.8 V	-60	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	-60	
			f _{in} = 1 MHz (sine wave)	1.4 V	-60	
			(see Figure 9)	1.65 V	-60	
Feed-through attenuation ⁽³⁾	0011	V 0011		2.3 V	-60	. i
(switch OFF)	COM or Y	Y or COM		0.8 V	-59	dB
			$C_L = 5 \text{ pF}, R_L = 600 \Omega,$	1.1 V	-59	
			$G_L = 3 \text{ pF}, R_L = 600 \Omega,$ $f_{in} = 1 \text{ MHz (sine wave)}$ (see Figure 9)	1.4 V	-59	
			(see Figure 9)	1.65 V	-59	
				2.3 V	-59	

 ⁽¹⁾ Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.
 (2) Adjust f_{in} voltage to obtain 0 dBm at input.
 (3) Adjust f_{in} voltage to obtain 0 dBm at input.



Analog Switch Characteristics (continued)

 $T_A = 25C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{cc}	TYP	UNIT
		Y or COM		0.8 V	6.19	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	1.1 V	0.39	
			f _{in} = 1 kHz (sine wave) (see Figure 10)	1.4 V	0.06	%
				1.65 V	0.02	
Sine-wave distortion	COM or Y			2.3 V	0.01	
Sine-wave distortion	COM OF Y	Y OF COIVE		0.8 V	3.55	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	1.1 V	0.38	
			f _{in} = 10 kHz (sine wave)	1.4 V	0.04	
			(see Figure 10)	1.65 V	0.02	
				2.3 V	0.02	

Operating Characteristics

for INH input, $T_A = 25C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	3	3	3	3	3	pF

Operating Characteristics

for A input, $T_A = 25C$

PARAMETER		TEST CONDITIONS	V _{CC} = 0.8 V TYP	V _{CC} = 1.2 V TYP	V _{CC} = 1.5 V TYP	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	UNIT	
_	Power C _{pd} dissipation capacitance	Outputs enabled	f 40 MHz	5.5	5.5	5.5	5.5	5.5	, F
C_{pd}		Outputs disabled	f = 10 MHz	0.5	0.5	0.5	0.5	0.5	pF

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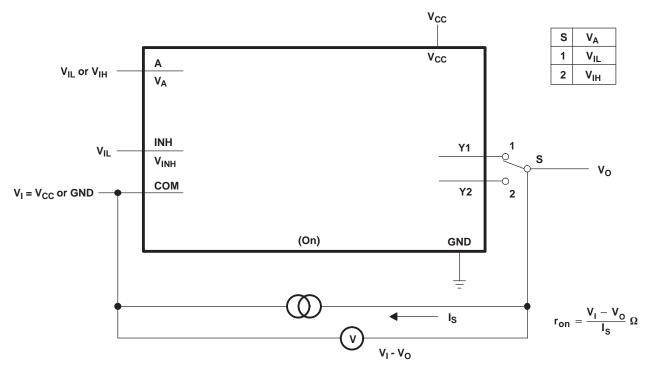


Figure 1. On-State Resistance Test Circuit

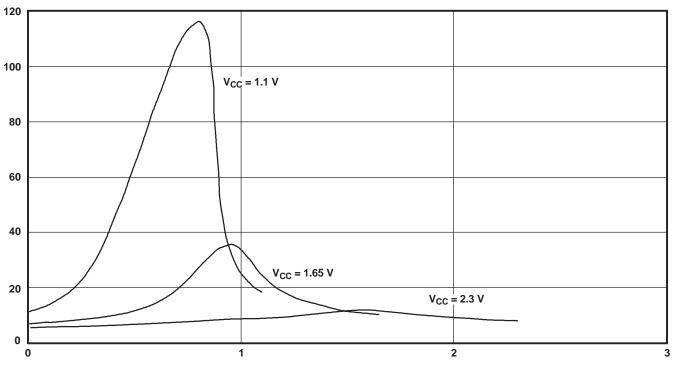


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for $V_{I} = 0$ to V_{CC}



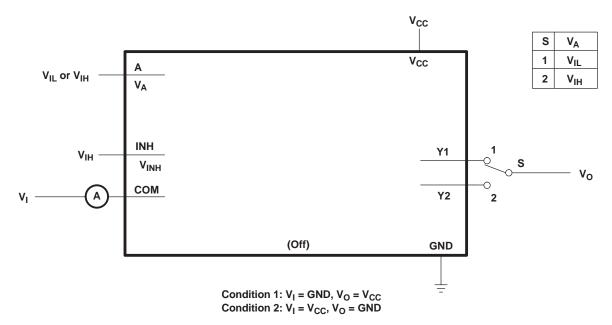


Figure 3. Off-State Switch Leakage-Current Test Circuit

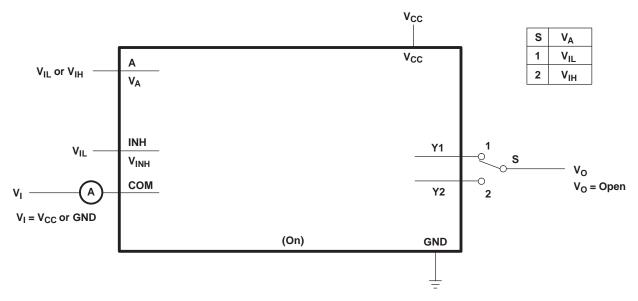
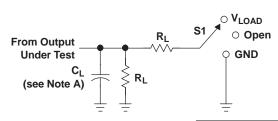


Figure 4. On-State Switch Leakage-Current Test Circuit

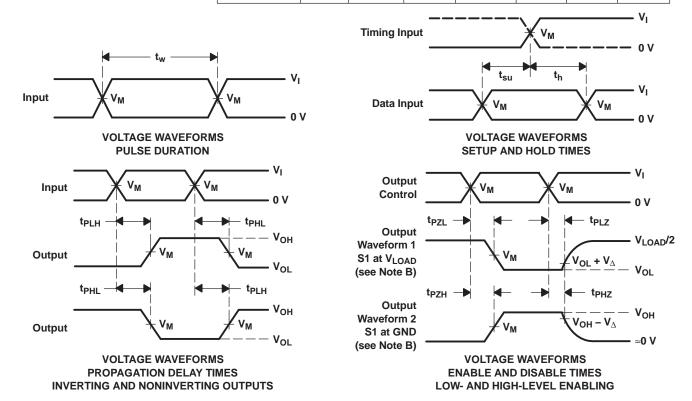




TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

.,	INPUTS		V	V			.,
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_{\Delta}$
0.8 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	15 pF	2 k Ω	0.15 V
1.8 V \pm 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

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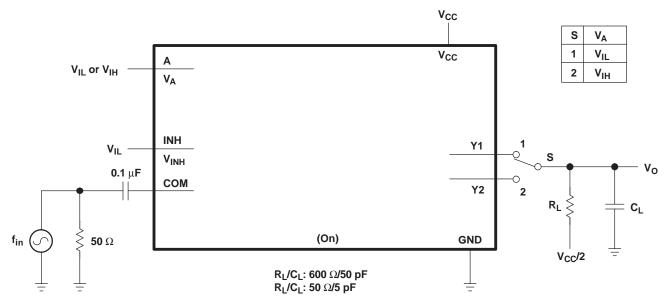


Figure 6. Frequency Response (Switch On)

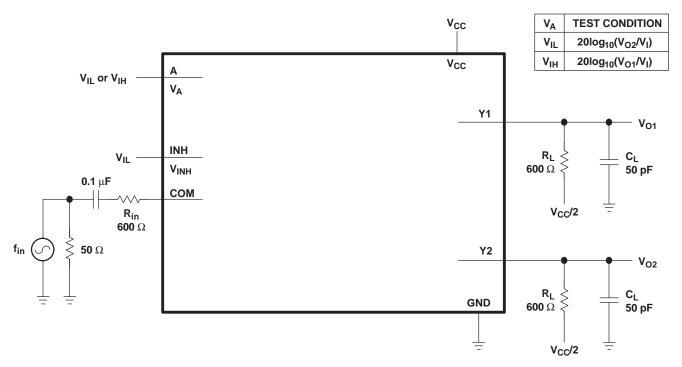


Figure 7. Crosstalk (Between Switches)



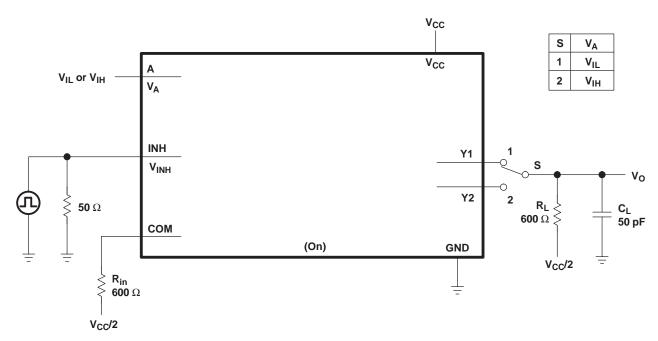


Figure 8. Crosstalk (Control Input, Switch Output)

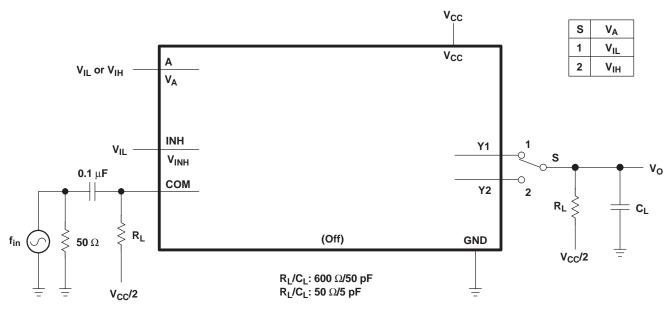
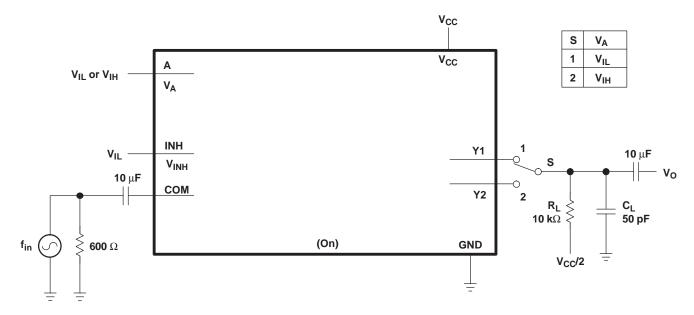


Figure 9. Feedthrough (Switch Off)





$$\begin{split} &V_{CC} = 0.8 \text{ V, V}_I = 0.7 \text{ V}_{P\text{-P}} \\ &V_{CC} = 1.1 \text{ V, V}_I = 1 \text{ V}_{P\text{-P}} \\ &V_{CC} = 1.4 \text{ V, V}_I = 1.2 \text{ V}_{P\text{-P}} \\ &V_{CC} = 1.65 \text{ V, V}_I = 1.4 \text{ V}_{P\text{-P}} \\ &V_{CC} = 2.3 \text{ V, V}_I = 2 \text{ V}_{P\text{-P}} \end{split}$$

Figure 10. Sine-Wave Distortion

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AUC2G53DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53
									Z
SN74AUC2G53DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53
			· , , .						Z
SN74AUC2G53DCTRE4	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53
			` , ,						Z
SN74AUC2G53DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(U53Q, U53R)
SN74AUC2G53DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U53Q, U53R)
SN74AUC2G53DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53R
SN74AUC2G53DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53R
SN74AUC2G53YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U4N
SN74AUC2G53YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U4N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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TAPE AND REEL INFORMATION





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A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G53DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G53DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G53YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G53DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G53DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G53YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

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- 8. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

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DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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