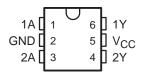
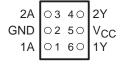
- Available in the Texas Instruments
   NanoStar™ and NanoFree™ Packages
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max t<sub>pd</sub> of 1.7 ns at 1.8 V
- Low Power Consumption, 10 μA at 1.8 V
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### DBV OR DCK PACKAGE (TOP VIEW)



## YEP OR YZP PACKAGE (BOTTOM VIEW)



## description/ordering information

This dual inverter is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC2G04 performs the Boolean function  $Y = \overline{A}$ .

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AUC2G04YEPR	UC
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AUC2G04YZPR	0C_
	SOT (SOT-23) – DBV	Tape and reel	SN74AUC2G04DBVR	U04_
	SOT (SC-70) – DCK	Tape and reel	SN74AUC2G04DCKR	UC_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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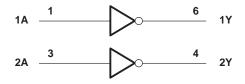
DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

## FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Voltage range applied to any output in the high-impedance or power-off state, Vo	
(see Note 1)	–0.5 V to 3.6 V
Output voltage range, V <sub>O</sub> (see Note 1)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DBV package	165°C/W
DCK package	258°C/W
YEP/YZP package	123°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



## recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		0.8	2.7	V
		V <sub>CC</sub> = 0.8 V	Vcc		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	0.65 × V <sub>CC</sub>		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		V <sub>CC</sub> = 0.8 V		0	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		0.35 × V <sub>CC</sub>	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
VI	Input voltage		0	3.6	V
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 0.8 V		-0.7	
		V <sub>CC</sub> = 1.1 V		-3	
loh	High-level output current	V <sub>CC</sub> = 1.4 V		<b>-</b> 5	mA
		V <sub>CC</sub> = 1.65 V		-8	
		V <sub>CC</sub> = 2.3 V		-9	
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
loL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
		V <sub>CC</sub> = 1.65 V		8	
		V <sub>CC</sub> = 2.3 V		9	
Δt/Δν	Input transition rise or fall rate	•		20	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDITIO	NS	vcc	MIN	TYP†	MAX	UNIT
$I_{OH} = -100  \mu A$		I <sub>OH</sub> = -100 μA		0.8 V to 2.7 V	V <sub>CC</sub> -0.1			
		I <sub>OH</sub> = -0.7 mA		0.8 V		0.55		
V		I <sub>OH</sub> = -3 mA		1.1 V	0.8			V
VOH		I <sub>OH</sub> = -5 mA		1.4 V	1			V
		I <sub>OH</sub> = -8 mA		1.65 V	1.2			
		I <sub>OH</sub> = -9 mA		2.3 V	1.8			
		I <sub>OL</sub> = 100 μA		0.8 V to 2.7 V			0.2	
		I <sub>OL</sub> = 0.7 mA		0.8 V		0.25		
\/-·		I <sub>OL</sub> = 3 mA		1.1 V			0.3	V
VOL		I <sub>OL</sub> = 5 mA		1.4 V			0.4	V
		I <sub>OL</sub> = 8 mA		1.65 V			0.45	
		I <sub>OL</sub> = 9 mA		2.3 V			0.6	
II	A inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		0 to 2.7 V			±5	μΑ
l <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 2.7 V		0			±10	μΑ
Icc		V <sub>I</sub> = V <sub>CC</sub> or GND,	IO = 0	0.8 V to 2.7 V			10	μΑ
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND		2.5 V		2.1		pF

 $<sup>\</sup>overline{\dagger}$  All typical values are at  $T_A = 25^{\circ}C$ .



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# switching characteristics over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = ± 0.		V <sub>CC</sub> =			C = 1.8 0.15 V		V <sub>CC</sub> =		UNIT
	(INT OT)	(0011 01)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
<sup>t</sup> pd	Α	Y	5.4	0.9	3.1	0.7	2	0.6	1	1.7	0.5	1.2	ns

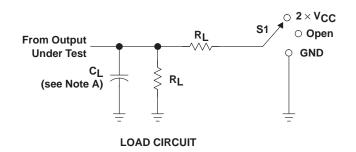
# switching characteristics over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		c = 1.8 0.15 V	V	V <sub>CC</sub> =		UNIT
	(1141 01)	(0011 01)	MIN	TYP	MAX	MIN	MAX	
<sup>t</sup> pd	A	Y	0.8	1.3	2	0.7	1.5	ns

## operating characteristics, T<sub>A</sub> = 25°C

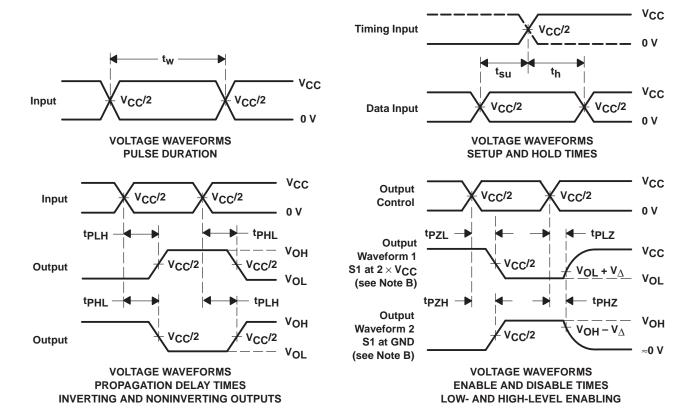
	PARAMETER	TEST	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
	TANAMILTEN	CONDITIONS	TYP	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	12.5	12.5	12.5	12.5	14	pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	$2 \times \mathbf{V_{CC}}$
tPHZ/tPZH	GND

VCC	CL	RL	$v_\Delta$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	<b>2 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	<b>2 k</b> Ω	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74AUC2G04DBVR	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U04R
SN74AUC2G04DBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U04R
SN74AUC2G04DCKR	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(UCF, UCR)
SN74AUC2G04DCKR.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(UCF, UCR)
SN74AUC2G04DCKRG4	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCF
SN74AUC2G04DCKRG4.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCF
SN74AUC2G04YZPR	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UCN
SN74AUC2G04YZPR.B	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UCN

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE OPTION ADDENDUM**

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G04DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC2G04YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G04DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUC2G04YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



#### NOTES:

NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.
- 3. NanoFree<sup>™</sup> package configuration.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

  4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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