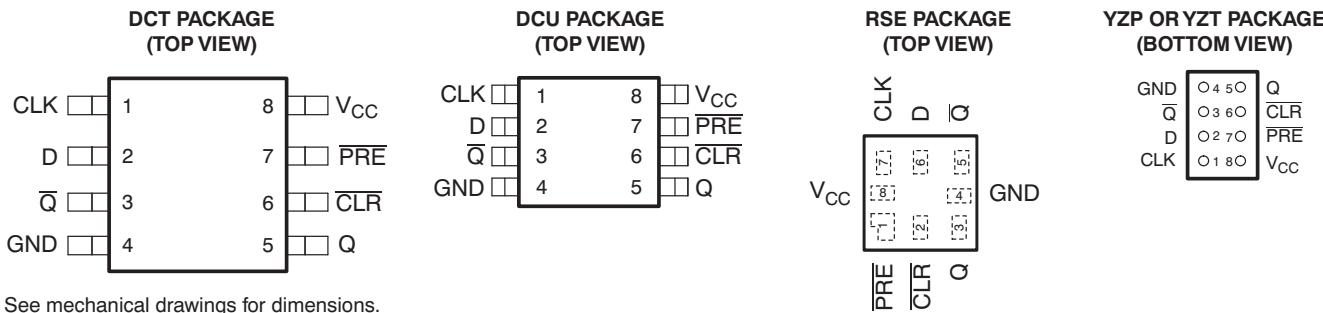


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.5 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{cc}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. To better optimize the flip-flop for higher frequencies, the CLR input overrides the PRE input when they are both low.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000 SN74AUC1G74YZPR	—_UP_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free)	Reel of 3000 SN74AUC1G74YZTR	
	QFN – RSE	Reel of 3000 SN74AUC1G74RSER	UP
	SSOP – DCT	Reel of 3000 SN74AUC1G74DCTR	U74_—_
	VSSOP – DCU	Reel of 3000 SN74AUC1G74DCUR	U74_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

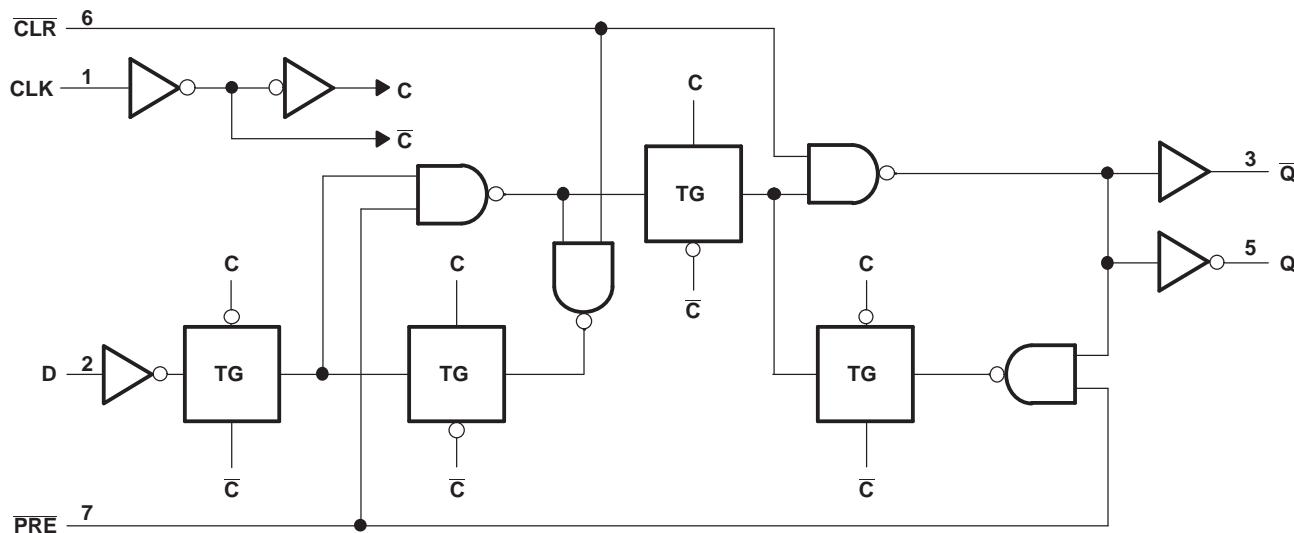
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP/YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

LOGIC DIAGRAM (POSITIVE LOGIC)



A. Pin numbers shown are for the DCT, DCU, YZP, and YZT packages only.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	3.6	V
V_I	Input voltage range ⁽²⁾	-0.5	3.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	3.6	V
V_O	Output voltage range ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current $V_I < 0$	-50		mA
I_{OK}	Output clamp current $V_O < 0$	-50		mA
I_O	Continuous output current		± 20	mA
	Continuous current through V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCT package	220	°C/W
		DCU package	227	
		RSE package	253	
		YZP/YZT package	102	
T_{stg}	Storage temperature range	-65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8$ V	V_{CC}	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8$ V	0	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8$ V	-0.7	mA
		$V_{CC} = 1.1$ V	-3	
		$V_{CC} = 1.4$ V	-5	
		$V_{CC} = 1.65$ V	-8	
		$V_{CC} = 2.3$ V	-9	
I_{OL}	Low-level output current	$V_{CC} = 0.8$ V	0.7	mA
		$V_{CC} = 1.1$ V	3	
		$V_{CC} = 1.4$ V	5	
		$V_{CC} = 1.65$ V	8	
		$V_{CC} = 2.3$ V	9	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8$ V to 1.65 V ⁽²⁾	20	ns/V
		$V_{CC} = 1.65$ V to 2.3 V ⁽³⁾	20	
		$V_{CC} = 2.3$ V to 2.7 V ⁽³⁾	20	
T_A	Operating free-air temperature	-40	85	°C

- All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

- The data was taken at $C_L = 15$ pF, $R_L = 2$ kΩ (see Figure 1).

- The data was taken at $C_L = 30$ pF, $R_L = 500$ Ω (see Figure 1).

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 μ A		0.8 V to 2.7 V	V _{CC} - 0.1			V
	I _{OH} = -0.7 mA		0.8 V		0.55		
	I _{OH} = -3 mA		1.1 V		0.8		
	I _{OH} = -5 mA		1.4 V		1		
	I _{OH} = -8 mA		1.65 V		1.2		
	I _{OH} = -9 mA		2.3 V		1.8		
V _{OL}	I _{OL} = 100 μ A		0.8 V to 2.7 V		0.2		V
	I _{OL} = 0.7 mA		0.8 V		0.25		
	I _{OL} = 3 mA		1.1 V		0.3		
	I _{OL} = 5 mA		1.4 V		0.4		
	I _{OL} = 8 mA		1.65 V		0.45		
	I _{OL} = 9 mA		2.3 V		0.6		
I _I	All inputs	V _I = V _{CC} or GND	0 to 2.7 V		5	μ A	
I _{off}		V _I or V _O = 2.7 V	0		\pm 10	μ A	
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V		10	μ A	
C _I		V _I = V _{CC} or GND	2.5 V		2.5	pF	

(1) All typical values are at T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		V _{CC} = 0.8 V	V _{CC} = 1.2 V \pm 0.1 V		V _{CC} = 1.5 V \pm 0.1 V		V _{CC} = 1.8 V \pm 0.15 V		V _{CC} = 2.5 V \pm 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	50		200		225		250		275	MHz
t _w	Pulse duration	CLK	2	1		1		1		1	ns
		PRE or CLR low	5	1.5		1		1		1	
t _{su}	Setup time before CLK↑	Data	2.2	0.6		0.5		0.5		0.4	ns
		PRE or CLR inactive	2.9	1.6		0.9		0.7		0.4	
t _h	Hold time, data after CLK↑		1.2	0.5		0.4		0.3		0.3	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V \pm 0.1 V		V _{CC} = 1.5 V \pm 0.1 V		V _{CC} = 1.8 V \pm 0.15 V			V _{CC} = 2.5 V \pm 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			50	200		225		250		275			MHz
t _{pd}	CLK	Q	10.3	1.7	3.7	1.2	2.5	1	1.2	1.7	0.8	1.2	ns
		\overline{Q}	9.6	1	3.8	1	3	0.9	1.1	1.5	0.7	1.1	
	PRE or CLR	Q or \overline{Q}	12.9	2	4.5	0.9	3.1	1.1	1.5	2.2	0.9	1.5	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 1](#))

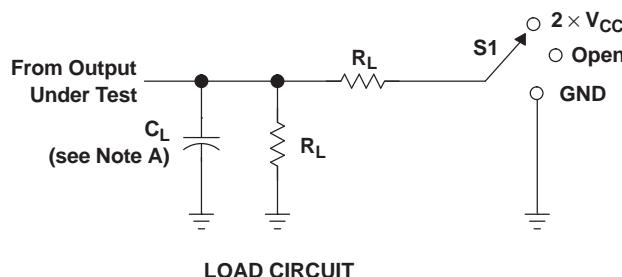
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$			UNIT
			MIN	TYP	MAX	MIN	MAX		
f_{max}			250			275			ns
t_{pd}	CLK	Q	1.5	1.9	2.4	1.4	1.8		ns
		\bar{Q}	1.4	1.9	2.4	1.3	1.8		
	PRE or CLR	Q or \bar{Q}	1.7	2.2	2.8	1.5	2.1		

Operating Characteristics

$T_A = 25^\circ\text{C}$

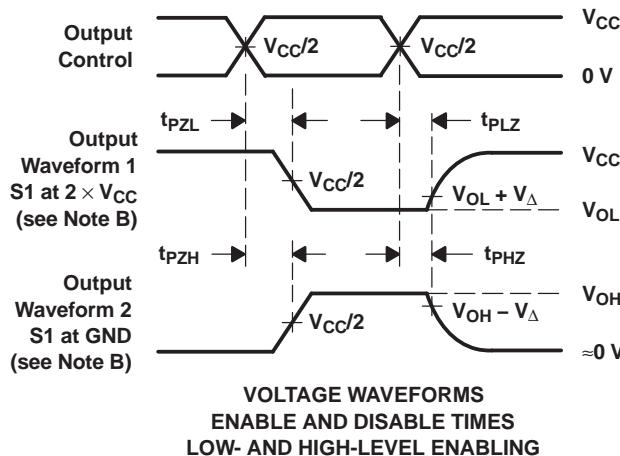
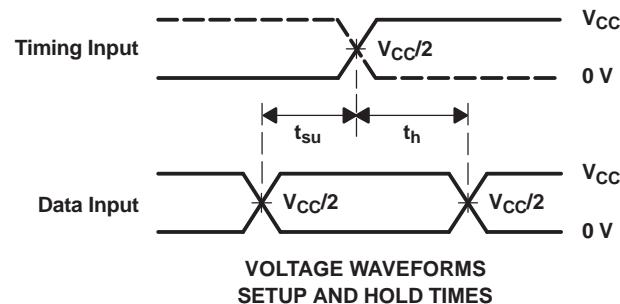
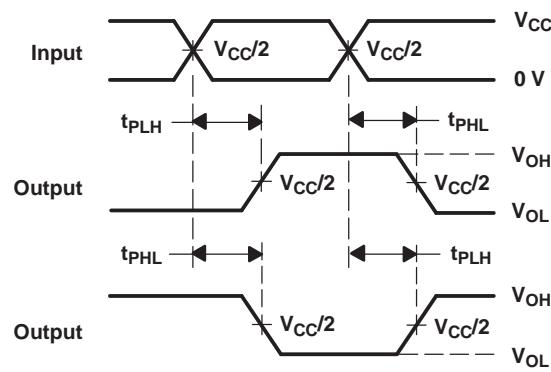
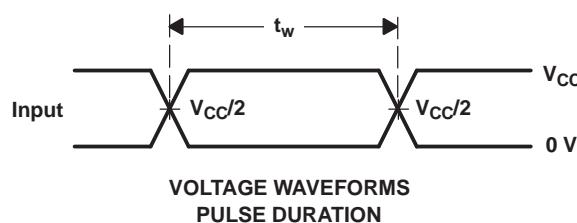
PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8 \text{ V}$		$V_{CC} = 1.2 \text{ V}$		$V_{CC} = 1.5 \text{ V}$		$V_{CC} = 1.8 \text{ V}$		$V_{CC} = 2.5 \text{ V}$		UNIT
		TYP	TYP									
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	36	39	44	59					pF

PARAMETER MEASUREMENT INFORMATION



TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
1.8 V \pm 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	30 pF	500 Ω	0.15 V



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, slew rate ≥ 1 V/ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUC1G74DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74Z
SN74AUC1G74DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74Z
SN74AUC1G74DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(74, U74Q, U74R) UZ
SN74AUC1G74DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(74, U74Q, U74R) UZ
SN74AUC1G74DCURE4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74R
SN74AUC1G74DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74R
SN74AUC1G74DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74R
SN74AUC1G74RSER	Active	Production	UQFN (RSE) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UP
SN74AUC1G74RSER.B	Active	Production	UQFN (RSE) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UP
SN74AUC1G74RSERG4.B	Active	Production	UQFN (RSE) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UP
SN74AUC1G74YZPR	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UPN
SN74AUC1G74YZPR.B	Active	Production	DSBGA (YZP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UPN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

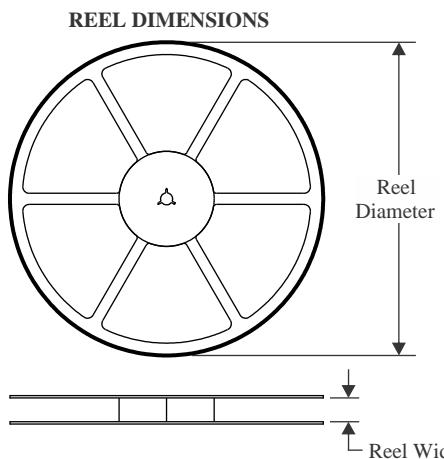
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

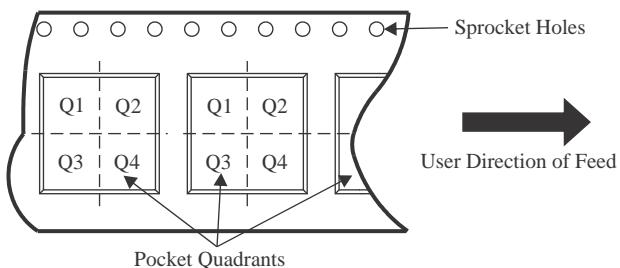
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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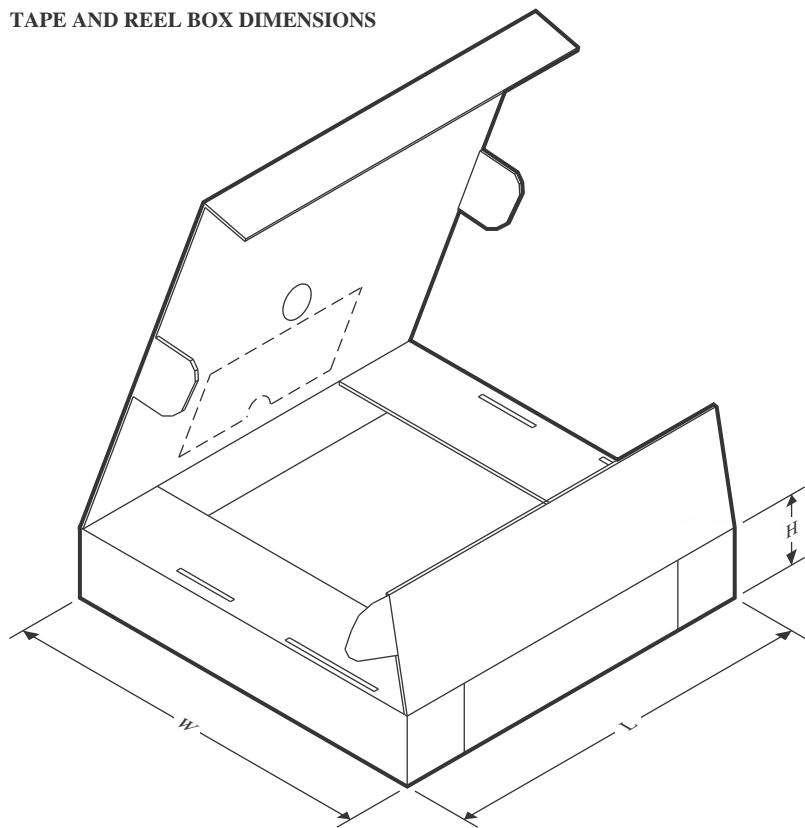
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G74DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC1G74DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74AUC1G74DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC1G74RSER	UQFN	RSE	8	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q2
SN74AUC1G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G74DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUC1G74DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74AUC1G74DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC1G74RSER	UQFN	RSE	8	3000	189.0	185.0	36.0
SN74AUC1G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

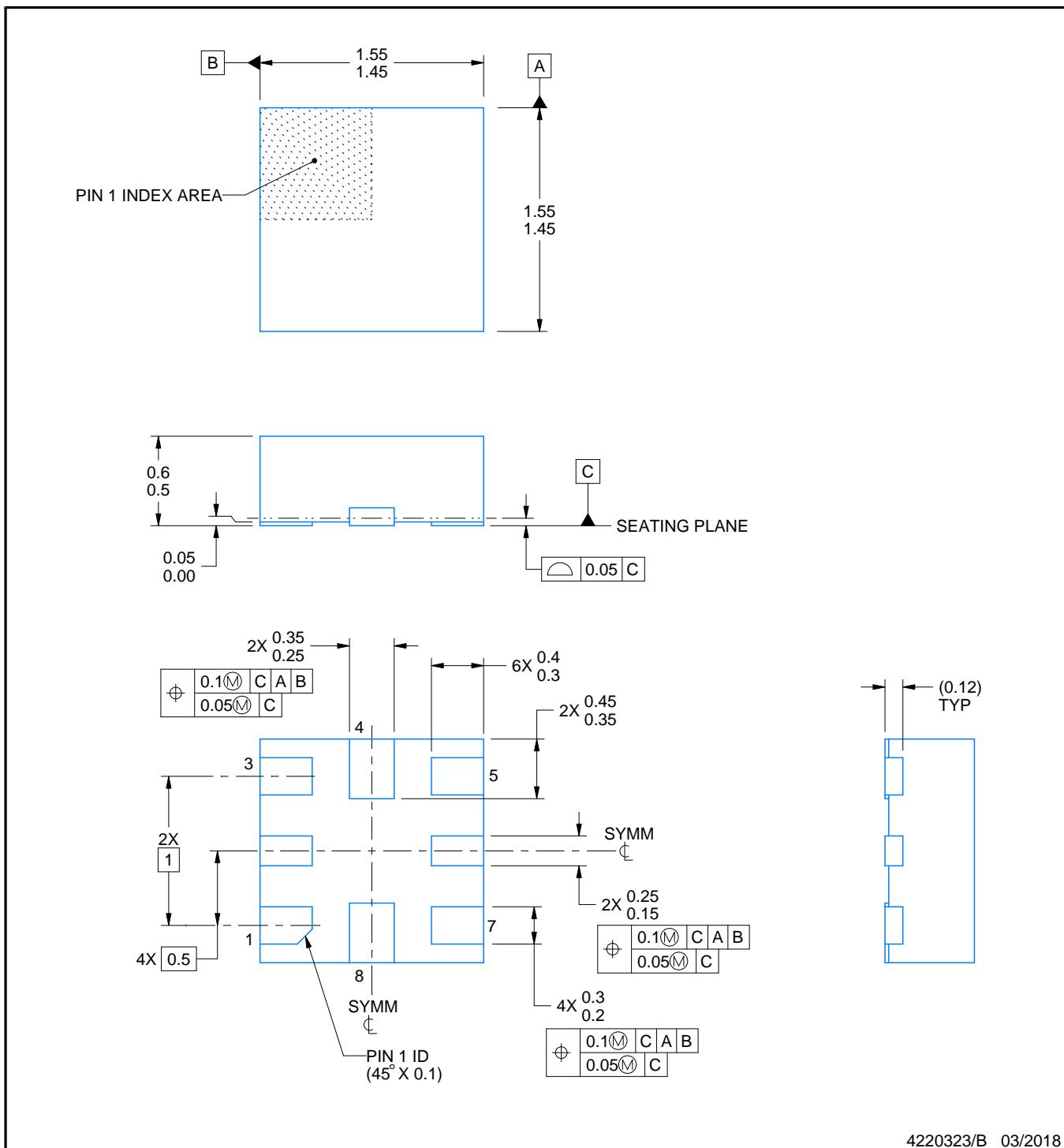
PACKAGE OUTLINE

RSE0008A



UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4220323/B 03/2018

NOTES:

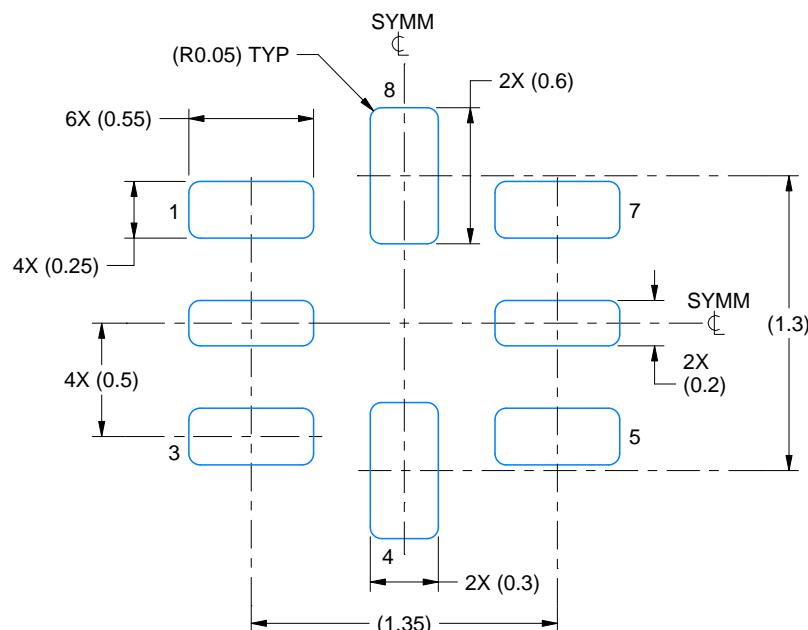
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

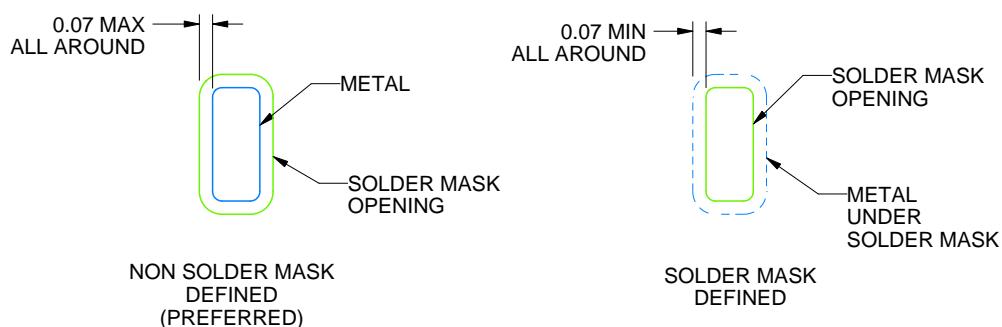
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE



SOLDER MASK DETAILS NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

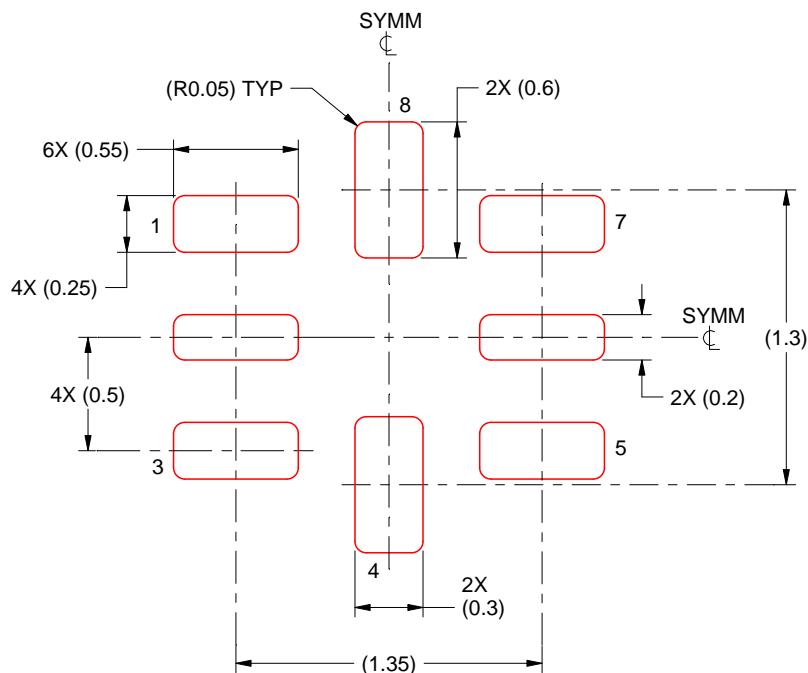
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

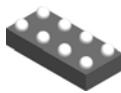


**SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X**

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

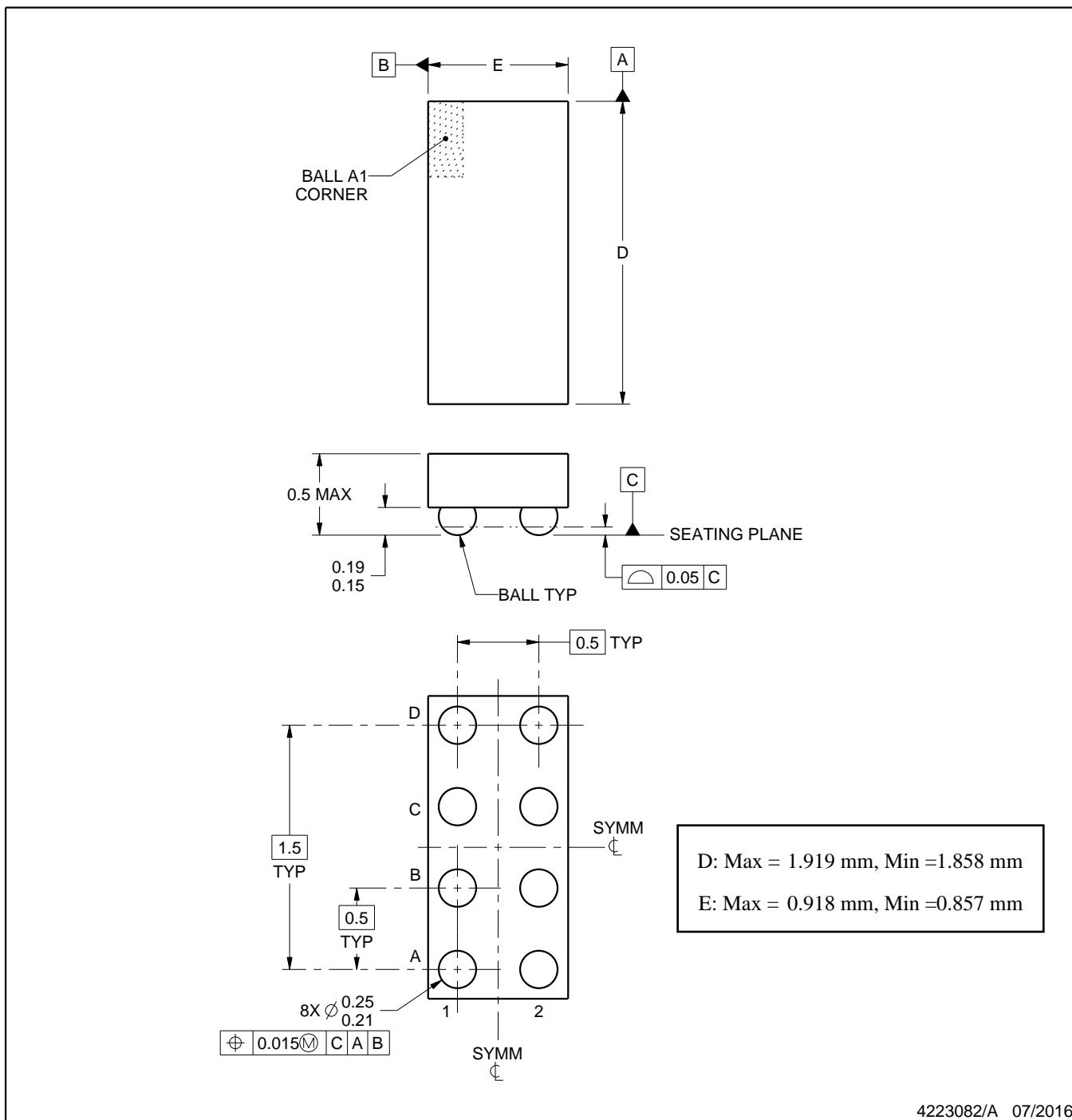


PACKAGE OUTLINE

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

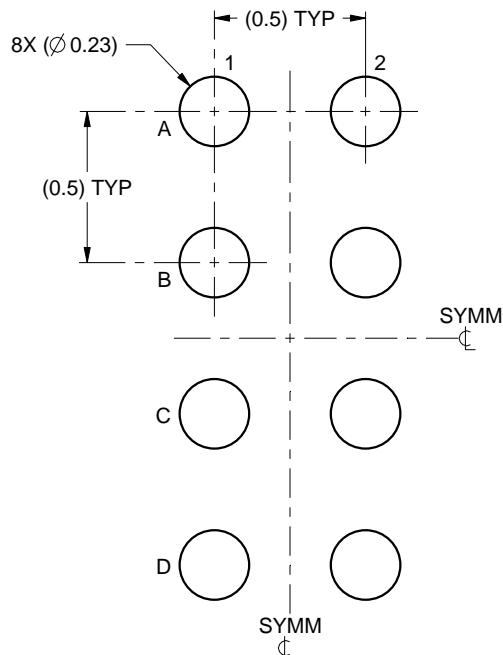
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

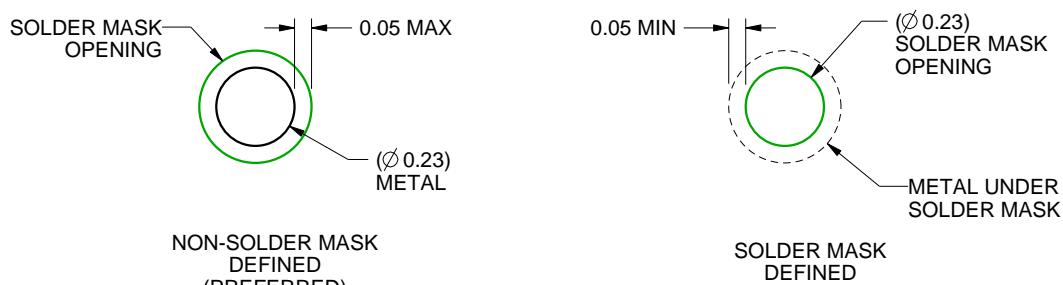
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

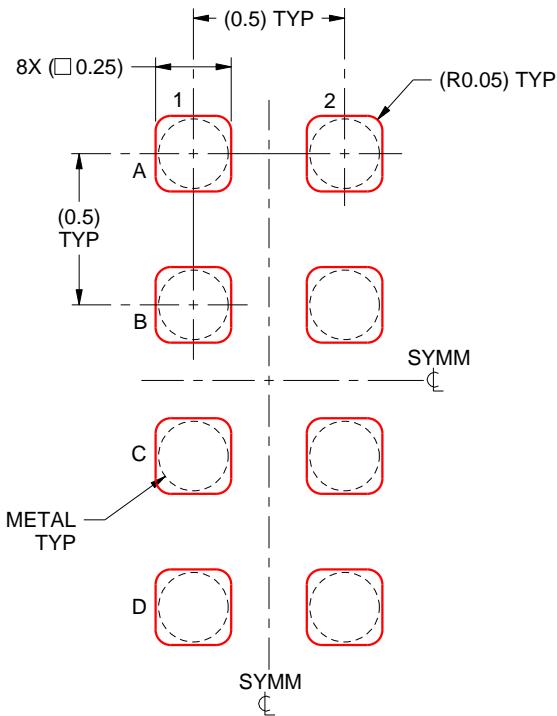
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

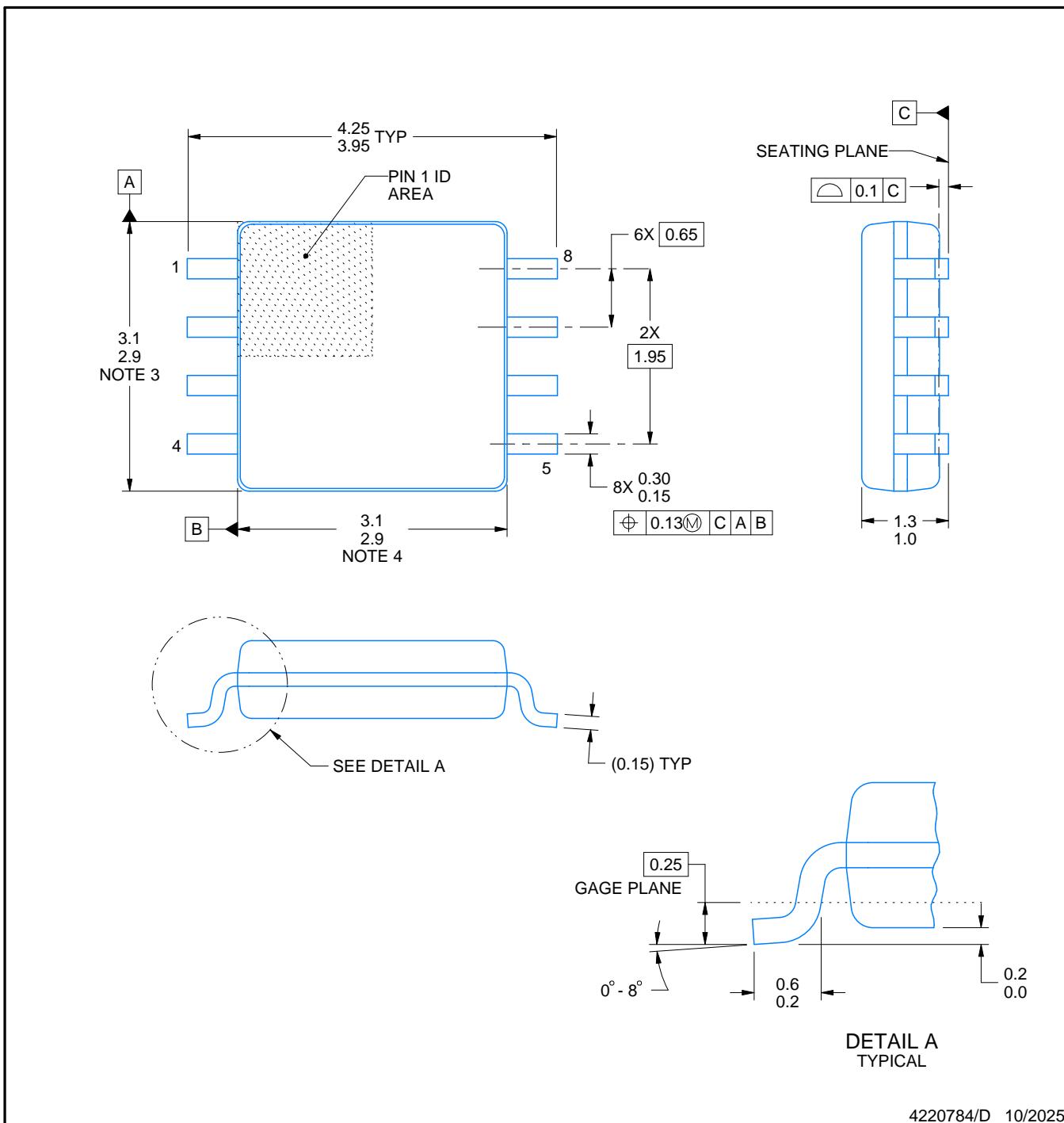
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



PACKAGE OUTLINE

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



NOTES:

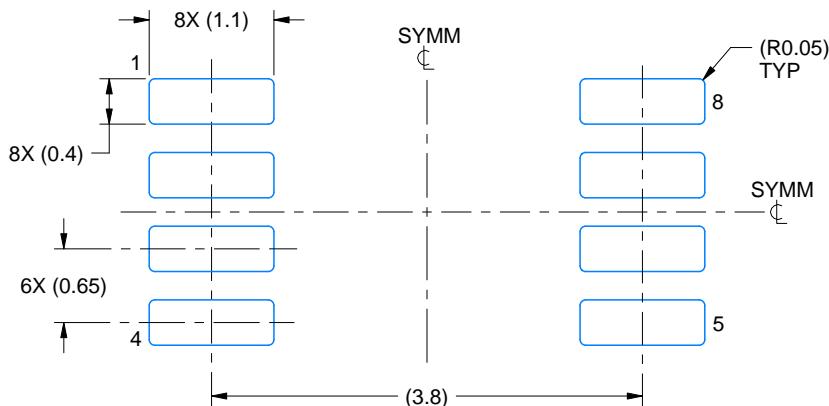
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

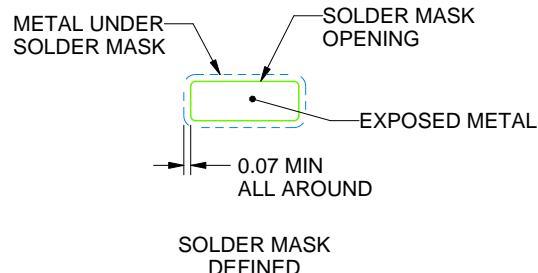
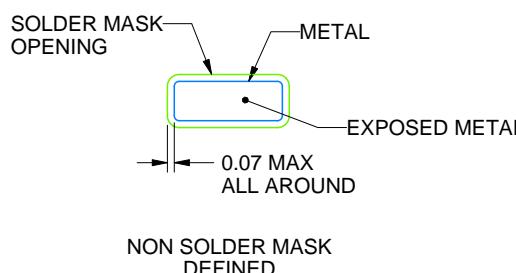
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

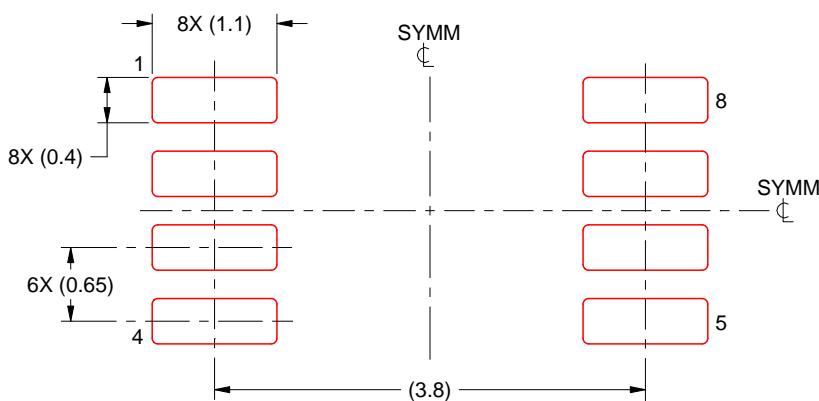
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

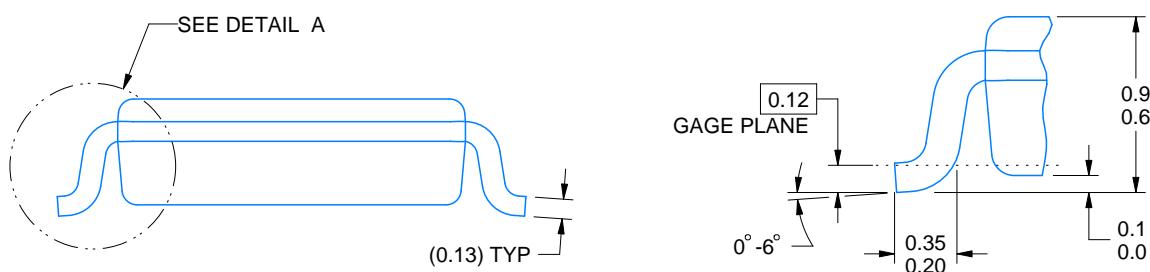
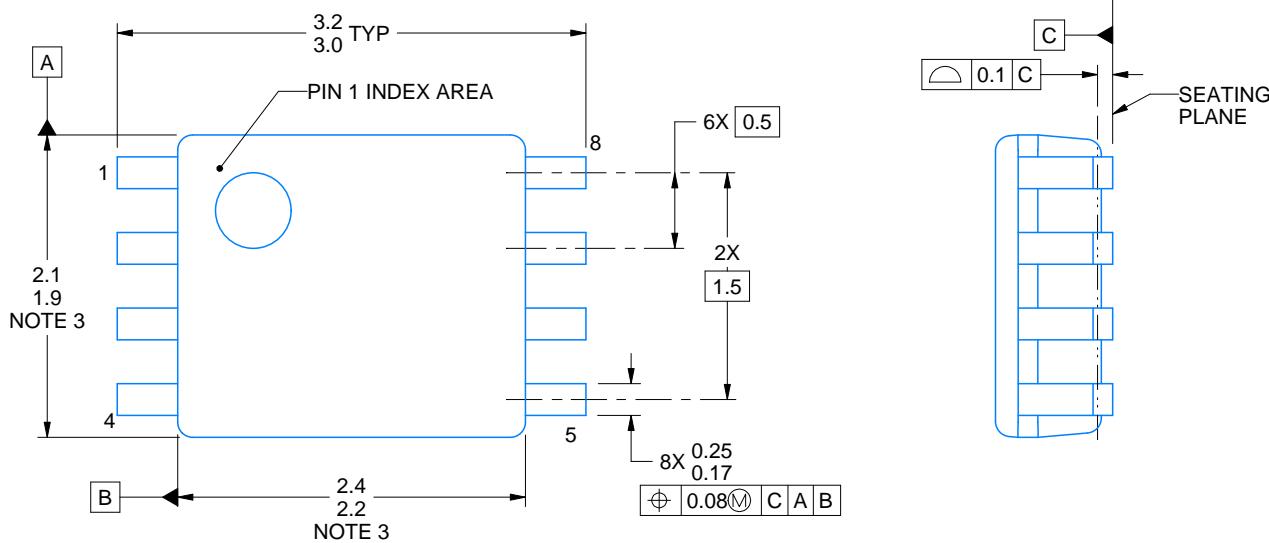
PACKAGE OUTLINE

DCU0008A



VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



DETAIL A TYPICAL

NOTES:

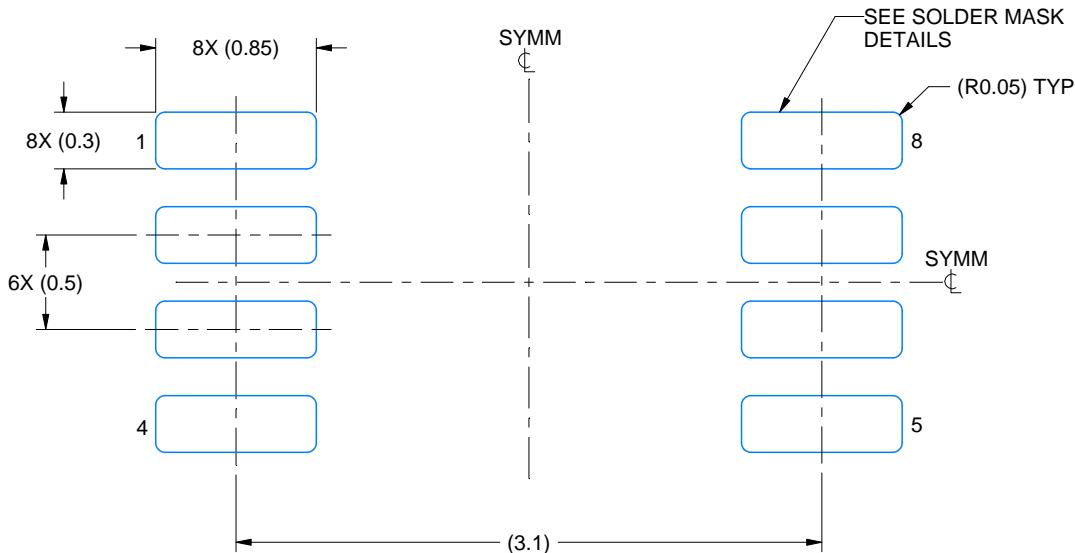
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

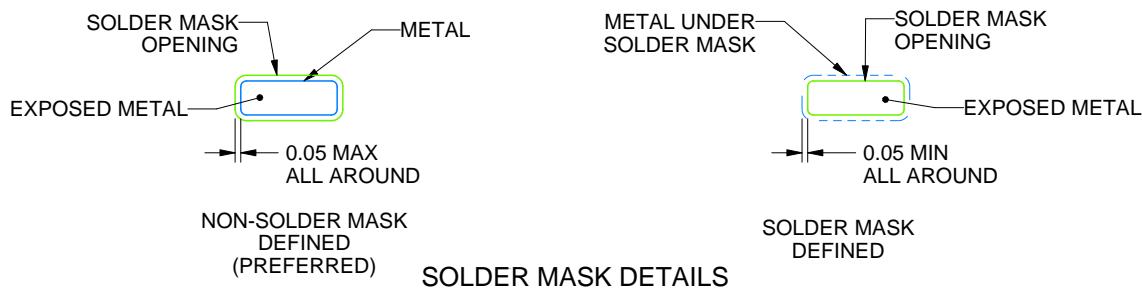
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

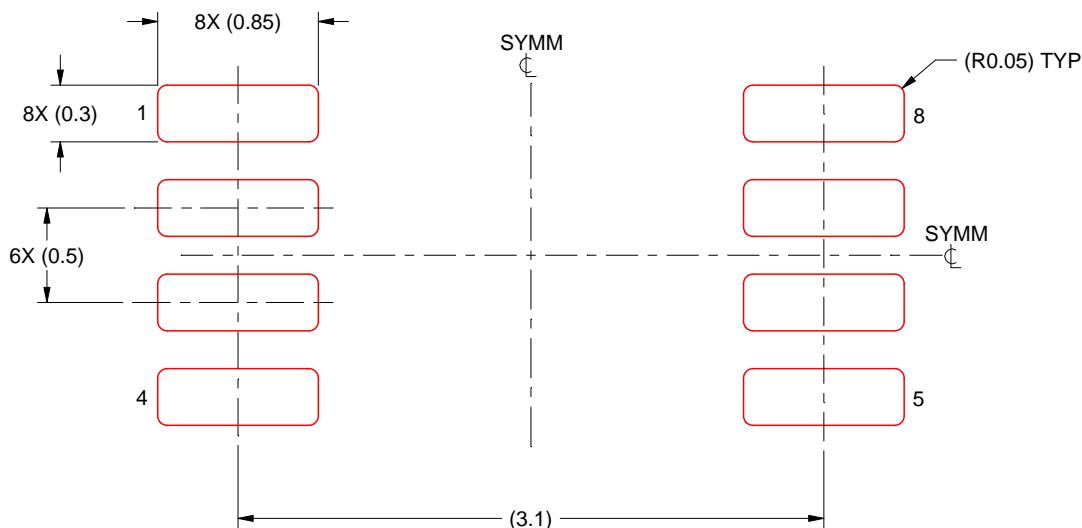
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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