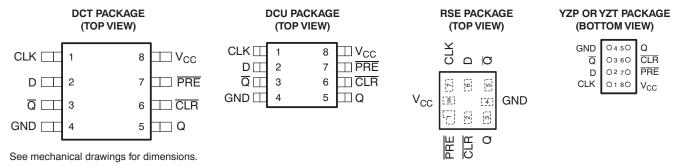
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#### **FEATURES**

- Available in the Texas Instruments
   NanoFree<sup>™</sup> Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t<sub>pd</sub> of 1.5 ns at 1.8 V

- Low Power Consumption, 10-µA Max I<sub>CC</sub>
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



### **DESCRIPTION/ORDERING INFORMATION**

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. To better optimize the flip-flop for higher frequencies, the CLR input overrides the PRE input when they are both low.

NanoFree<sup>™</sup> package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

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#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
	NanoFree <sup>™</sup> – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC1G74YZPR	UP
–40°C to 85°C	NanoFree <sup>™</sup> – WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free)	Reel of 3000	SN74AUC1G74YZTR	0F_
10 0 10 00 0	QFN - RSE	Reel of 3000	SN74AUC1G74RSER	UP
	SSOP - DCT	Reel of 3000	SN74AUC1G74DCTR	U74
	VSSOP – DCU	Reel of 3000	SN74AUC1G74DCUR	U74_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

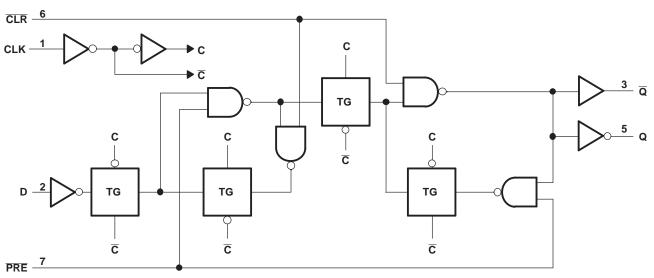
  DCU: The actual top-side marking has one additional character that designates the assembly/test site.

  YZP/YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

#### **FUNCTION TABLE**

	INP	UTS		OUTPUTS			
PRE	CLR	CLK	D	Q	Q		
L	Н	Χ	Χ	Н	L		
X	L	Χ	Χ	L	Н		
Н	Н	$\uparrow$	Н	Н	L		
Н	Н	$\uparrow$	L	L	Н		
Н	Н	L	Χ	$Q_0$	$\overline{Q}_{0}$		

## **LOGIC DIAGRAM (POSITIVE LOGIC)**



A. Pin numbers shown are for the DCT, DCU, YZP, and YZT packages only.

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# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
$V_{CC}$	Supply voltage range		-0.5	3.6	V	
VI	Input voltage range (2)		-0.5	3.6	V	
Vo	Voltage range applied to any output in the	ne high-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V	
Vo	Output voltage range (2)	t clamp current $V_{I} < 0$ ut clamp current $V_{O} < 0$ inuous output current				
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50		
Io	Continuous output current		±20	mA		
	Continuous current through V <sub>CC</sub> or GND			±100	mA	
		DCT package		220		
Δ	Package thermal impedance <sup>(3)</sup>	DCU package		227	°C/W	
$\theta_{JA}$	Fackage thermal impedance (**)	RSE package		253	C/VV	
		YZP/YZT package		102		
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# Recommended Operating Conditions<sup>(1)</sup>

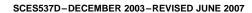
			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		0.8	2.7	V
		$V_{CC} = 0.8 \text{ V}$	$V_{CC}$		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		$V_{CC} = 0.8 \text{ V}$		0	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{\text{CC}}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
$V_{I}$	Input voltage		0	3.6	٧
Vo	Output voltage		0	$V_{CC}$	٧
		V <sub>CC</sub> = 0.8 V		-0.7	
		V <sub>CC</sub> = 1.1 V		-3	
$I_{OH}$	High-level output current	$V_{CC} = 1.4 \text{ V}$		-5	mA
		V <sub>CC</sub> = 1.65 V		-8	
		V <sub>CC</sub> = 2.3 V		-9	
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
$I_{OL}$	Low-level output current	$V_{CC} = 1.4 \text{ V}$		5	mA
		V <sub>CC</sub> = 1.65 V		8	
		V <sub>CC</sub> = 2.3 V		9	
		V <sub>CC</sub> = 0.8 V to 1.65 V <sup>(2)</sup>		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65 \text{ V to } 2.3 \text{ V}^{(3)}$		20	ns/V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}^{(3)}$		20	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>(2)</sup> The data was taken at  $C_L = 15$  pF,  $R_L = 2$  k $\Omega$  (see Figure 1). (3) The data was taken at  $C_L = 30$  pF,  $R_L = 500$   $\Omega$  (see Figure 1).





### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN TYP <sup>(1)</sup> MA	X UNIT
	$I_{OH} = -100 \mu A$	0.8 V to 2.7 V	V <sub>CC</sub> - 0.1	
	$I_{OH} = -0.7 \text{ mA}$	0.8 V	0.55	
V	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8	V
V <sub>OH</sub>	$I_{OH} = -5 \text{ mA}$	1.4 V	1	V
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2	
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8	
	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V	0	2
	I <sub>OL</sub> = 0.7 mA	0.8 V	0.25	
V	I <sub>OL</sub> = 3 mA	1.1 V	0	3 V
V <sub>OL</sub>	I <sub>OL</sub> = 5 mA	1.4 V	0	4
	I <sub>OL</sub> = 8 mA	1.65 V	0.4	5
	I <sub>OL</sub> = 9 mA	2.3 V	0	6
I <sub>I</sub> All inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V		5 μΑ
I <sub>off</sub>	$V_I$ or $V_O = 2.7 \text{ V}$	0	±1	0 μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V	1	0 μΑ
C <sub>I</sub>	$V_I = V_{CC}$ or GND	2.5 V	2.5	pF

<sup>(1)</sup> All typical values are at  $T_A = 25$ °C.

## **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		50		200		225		250		275	MHz
t <sub>w</sub> Pulse duration		CLK	2	1		1		1		1		
	Pulse duration	PRE or CLR low	5	1.5		1		1		1		ns
		Data	2.2	0.6		0.5		0.5		0.4		
t <sub>su</sub>	Setup time before CLK↑	PRE or CLR inactive	2.9	1.6		0.9		0.7		0.4		ns
t <sub>h</sub>	Hold time, data after CLK↑		1.2	0.5		0.4		0.3		0.3		ns

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	-		V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			50	200		225		250			275		MHz
CLK t <sub>pd</sub>	CLIK	Q	10.3	1.7	3.7	1.2	2.5	1	1.2	1.7	0.8	1.2	
	CLK	Q	9.6	1	3.8	1	3	0.9	1.1	1.5	0.7	1.1	ns
	PRE or CLR	Q or $\overline{\mathbb{Q}}$	12.9	2	4.5	0.9	3.1	1.1	1.5	2.2	0.9	1.5	



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## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)		c = 1.8 0.15 \		V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
	(INPUT)	(001F01)	MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			250			275		ns
t <sub>pd</sub>	CLK	Q	1.5	1.9	2.4	1.4	1.8	
	CLK	IQ	1.4	1.9	2.4	1.3	1.8	ns
	PRE or CLR	Q or $\overline{Q}$	1.7	2.2	2.8	1.5	2.1	

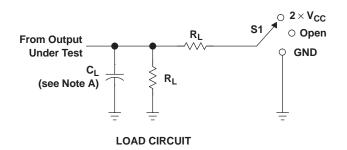
# **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

	PARAMETER			V <sub>CC</sub> = 1.2 V TYP	V <sub>CC</sub> = 1.5 V TYP	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	UNIT
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	35	36	39	44	59	pF

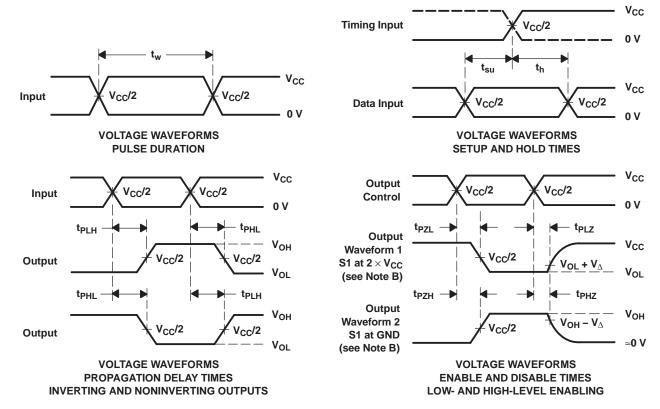


#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	$2 \times V_{CC}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>CC</sub>	CL	R <sub>L</sub>	$oldsymbol{V}_\Delta$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	<b>2 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	<b>2 k</b> Ω	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(.,	(=)			(8)	(4)	(5)		(0)
SN74AUC1G74DCTR	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74 Z
SN74AUC1G74DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74 Z
SN74AUC1G74DCUR	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(74, U74Q, U74R) UZ
SN74AUC1G74DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(74, U74Q, U74R) UZ
SN74AUC1G74DCURE4	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74R
SN74AUC1G74DCURG4	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74R
SN74AUC1G74DCURG4.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U74R
SN74AUC1G74RSER	Active	Production	UQFN (RSE)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UP
SN74AUC1G74RSER.B	Active	Production	UQFN (RSE)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UP
SN74AUC1G74RSERG4.B	Active	Production	UQFN (RSE)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UP
SN74AUC1G74YZPR	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UPN
SN74AUC1G74YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UPN

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G74DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC1G74DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74AUC1G74DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC1G74RSER	UQFN	RSE	8	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q2
SN74AUC1G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



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#### \*All dimensions are nominal

7 th difference die Herrinia.										
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
SN74AUC1G74DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0			
SN74AUC1G74DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0			
SN74AUC1G74DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0			
SN74AUC1G74RSER	UQFN	RSE	8	3000	189.0	185.0	36.0			
SN74AUC1G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0			





### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-187 variation CA.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





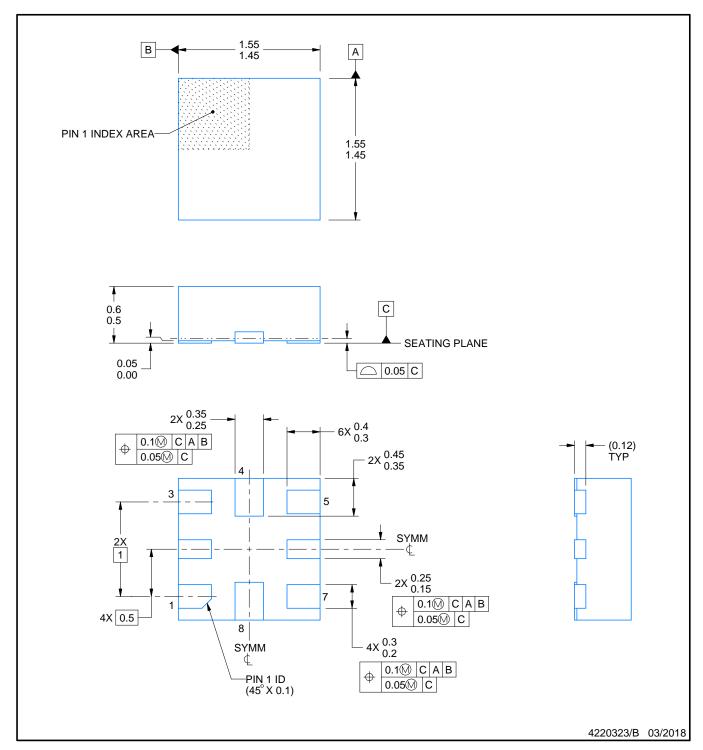
NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





PLASTIC QUAD FLATPACK - NO LEAD

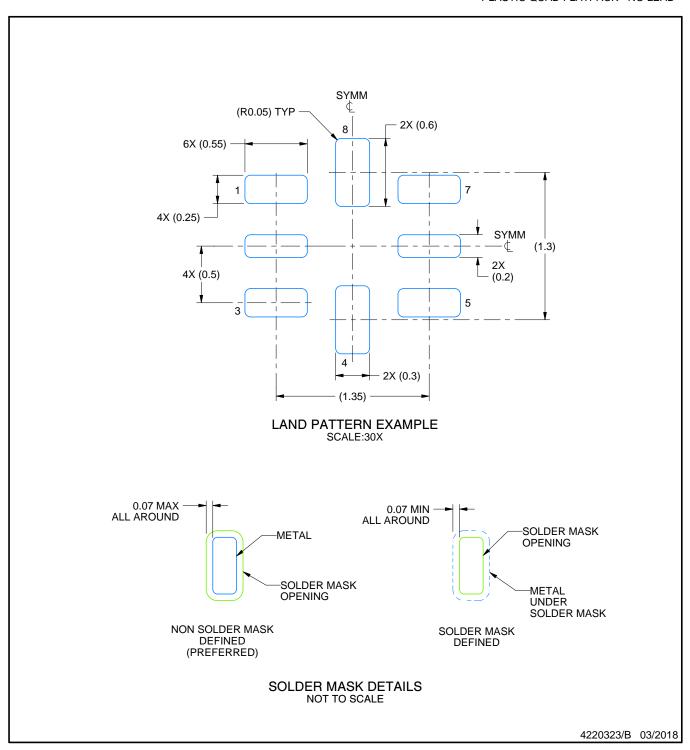


### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC QUAD FLATPACK - NO LEAD

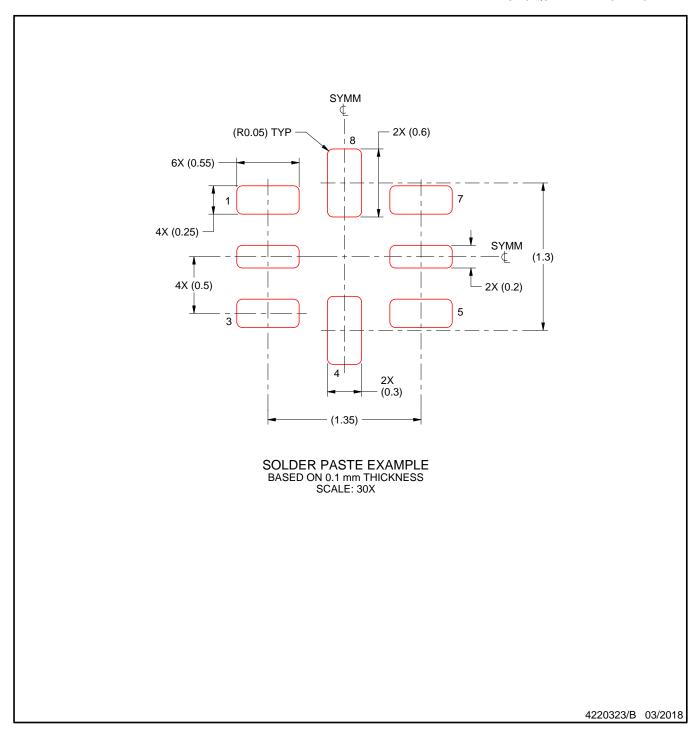


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



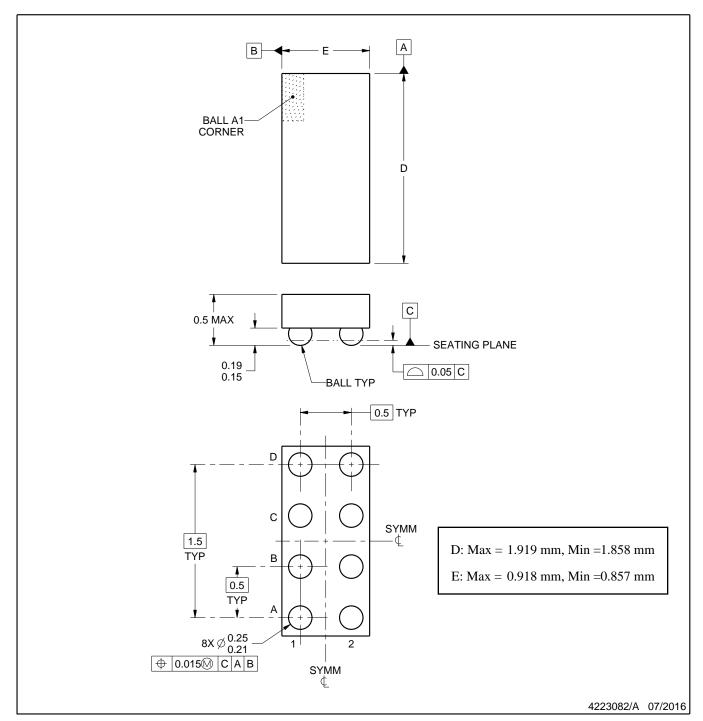
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





DIE SIZE BALL GRID ARRAY



### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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Last updated 10/2025