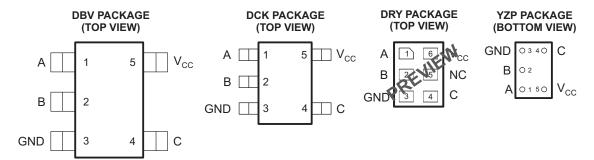
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SINGLE BILATERAL ANALOG SWITCH

FEATURES

- Available in the Texas Instruments NanoFree[™] Package
- Wide V_{CC} Range of 0.8 V to 2.7 V
- Sub-1-V Operable
- Low Power Consumption, 10-μA Max I_{CC}
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed Max 0.2 ns (V_{CC} = 1.8 V, C_L = 15 pF)

- Low On-State Impedance Typically 9 Ω (V_{CC} = 2.3 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions. NC– No internal connection

DESCRIPTION/ORDERING INFORMATION

This single analog switch is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G66 can handle both analog and digital signals. The combined AC and DC signal has to be between V_{CC} and GND for it to be transmitted in either direction.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

M

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.



ORDERING INFORMATION

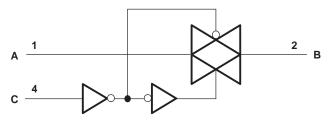
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
	NanoFree™ WCSP (DSBGA) – YZP (Pb-free)	Reel of 3000	SN74AUC1G66YZPR	U6_
-40°C to 85°C	SON - DRY	Reel of 5000	SN74AUC1G66DRYR	PREVIEW
	SOT (SOT-23) - DBV	Reel of 3000	SN74AUC1G66DBVR	U66_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUC1G66DCKR	U6_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRY: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
Н	ON

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	3.6	V
VI	Input voltage range ⁽²⁾		-0.5	3.6	V
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾	Switch I/O voltage range ⁽²⁾⁽³⁾		V _{CC} + 0.5	V
I _{IK}	Control input clamp current	V _I < 0		-50	mA
I _{IOK}	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		±50	mA
I _T	On-state switch current	$V_{I/O} = 0$ to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
		DBV package		206	
0	Package thermal impedance (4)	DCK package		252	°C/W
θ_{JA}	Package thermal impedance	DRY package		234	*C/VV
		YZP package		123	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- 3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	0.65 × V _{CC}		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		V _{CC} = 0.8 V		0	
V_{IL}	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
V _{I/O}	I/O port voltage		0	V_{CC}	V
VI	Control input voltage		0	3.6	V
Δt/Δν	Input transition rise or fall rate		20	ns/V	
T _A	Operating free-air temperature	-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	DITIONS	V _{cc}	MIN TYP(1)	MAX	UNIT
		$V_I = V_{CC}$ or GND,	I _S = 4 mA	1.65 V	10	20	_
r _{on}	On-state switch resistance	V _C = V _{IH} (see Figure 1)	$I_S = 8 \text{ mA}$	2.3 V	9	15	Ω
		$V_I = V_{CC}$ to GND,	I _S = 4 mA	1.65 V	32	80	
r _{on(p)}	Peak on resistance	V _C = V _{IH} (see Figure 1)	$I_S = 8 \text{ mA}$	2.3 V	15	20	Ω
I _{S(off)}	Off-state switch leakage current	$V_I = V_{CC}$ and $V_O = GN$ $V_I = GND$ and $V_O = V_C$ $V_C = V_{IL}$ (see Figure 2)	CC,	2.7 V		±1 ±0.1 ⁽¹⁾	μΑ
I _{S(on)}	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = (\text{see Figure 3})$	= V _{IH} , V _O = Open	2.7 V		±1 ±0.1 ⁽¹⁾	μΑ
I	Control input current	$V_I = V_{CC}$ or GND		0 to 2.7 V		±5	μΑ
I _{CC}	Supply current	$V_I = V_{CC}$ or GND,	I _O = 0	0.8 V to 2.7 V		10	μΑ
C _{ic}	Control input capacitance			2.5 V	2		pF
C _{io(off)}	Switch input/output capacitance			2.5 V	3.5		pF
C _{io(on)}	Switch input/output capacitance			2.5 V	7		pF

⁽¹⁾ All typical values are at $T_A = 25$ °C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = ± 0.		V _{CC} = ± 0.			_C = 1.8 : 0.15 \		V _{CC} = ± 0.		UNIT
	(INFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd} ⁽¹⁾	A or B	B or A	0.9		0.3		0.2			0.2		0.1	ns
t _{en}	С	A or B	4.1	0.5	2.6	0.5	1.7	0.5	8.0	1.1	0.5	1	ns
t _{dis}	С	A or B	5	0.7	3.6	0.5	2.6	0.5	1.7	2.9	0.5	2.2	ns

⁽¹⁾ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		
	(INPUT)	(001701)	MIN	TYP	MAX	MIN	MAX		
t _{pd} ⁽¹⁾	A or B	B or A			0.3		0.3	ns	
t _{en}	С	A or B	0.5	1.4	2.3	0.8	1.4	ns	
t _{dis}	С	A or B	0.5	1.7	2.9	0.5	1.5	ns	

⁽¹⁾ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



Analog Switch Characteristics

 $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	TYP	UNIT
				0.8 V	60	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	60	
			f _{in} = sine wave	1.4 V	80	
			(see Figure 5)	1.65 V	120	
Frequency response ⁽¹⁾	A or B	B or A		2.3 V	170	MHz
(switch ON)	AOIB	BULK		0.8 V	>500	IVII IZ
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	1.1 V	>500	
			f _{in} = sine wave	1.4 V	>500	
			(see Figure 5)	1.65 V	>500	
				2.3 V	>500	
				0.8 V	9	
O			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	14	
Crosstalk (control input to signal output)	С	A or B	f _{in} = 1 MHz (square wave)	1.4 V	15	mV
			(see Figure 6)	1.65 V	16	
				2.3 V	20	
				0.8 V	-60	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.1 V	-60	
		B or A	f _{in} = 1 MHz (sine wave) (see Figure 7)	1.4 V	-60	dB
			(See Figure 7)	1.65 V	-60	
Feedthrough attenuation (2)	A or B			2.3 V	-60	
(switch OFF)	7(0) 5			0.8 V	– 55	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	1.1 V	– 55	
			f _{in} = 1 MHz (sine wave)	1.4 V	– 55	
			(see Figure 7)	1.65 V	– 55	
				2.3 V	- 55	
				0.8 V	7.5	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	1.1 V	0.16	
	A or B	B or A	f _{in} = 1 kHz (sine wave)	1.4 V	0.04	
			(see Figure 8)	1.65 V	0.03	
Sine-wave distortion				2.3 V	0.02	%
C Maro diotoritori				0.8 V	4.2	70
	$C_1 = 50 pF$		$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	1.1 V	0.2	
	A or B	B or A	f _{in} = 10 kHz (sine wave)	1.4 V	0.03	
			(see Figure 8)	1.65 V	0.02	
				2.3 V	0.02	

⁽¹⁾ Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB. (2) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

 $T_A = 25$ °C

PARAMETER		TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V				UNIT	
		CONDITIONS	TYP	TYP	TYP	TYP	TYP	ļ	
C _{pd}	Power dissipation capacitance	f = 10 MHz	3	3	3	3	3	pF	



PARAMETER MEASUREMENT INFORMATION

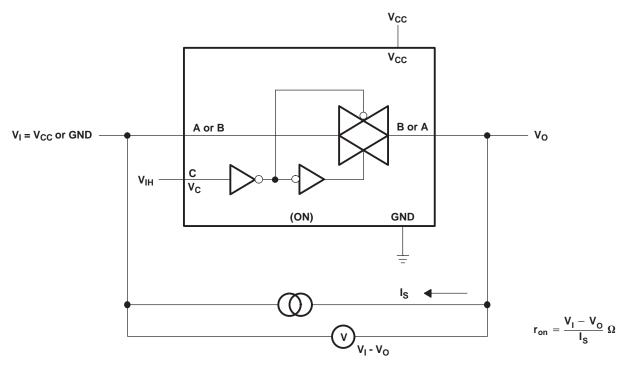


Figure 1. On-State Resistance Test Circuit

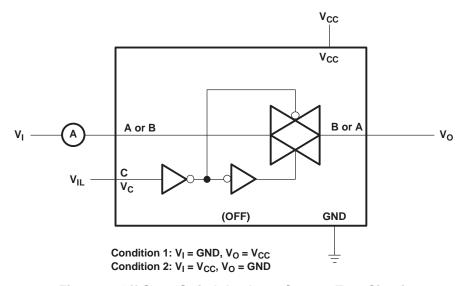


Figure 2. Off-State Switch Leakage-Current Test Circuit



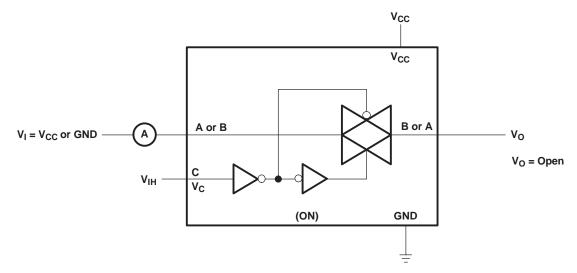
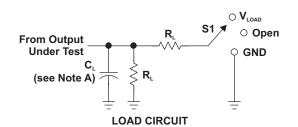


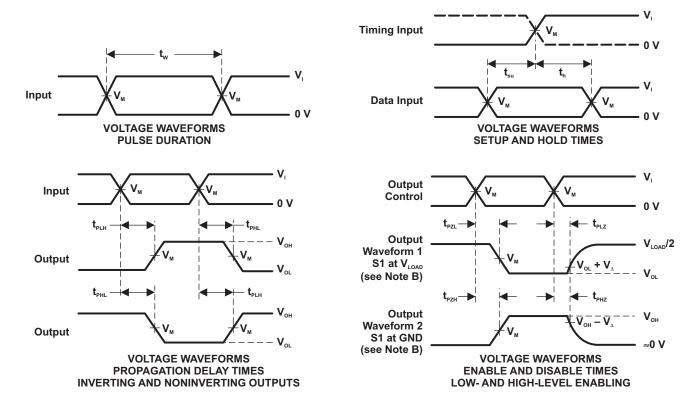
Figure 3. On-State Leakage-Current Test Circuit





TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	$V_{\scriptscriptstyle LOAD}$
t _{PHZ} /t _{PZH}	GND

V	INPUTS		V	V	•	Б	V
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _∟	R _∟	V _A
0.8 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	2 kΩ	0.15 V
$2.5~V\pm0.2~V$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
$2.5~\textrm{V} \pm 0.2~\textrm{V}$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V



NOTES: A. C. includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{\circ} = 50 Ω , Slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $t_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{\mbox{\tiny PLH}}$ and $t_{\mbox{\tiny PHL}}$ are the same as $t_{\mbox{\tiny pd}}$

Figure 4. Load Circuit and Voltage Waveforms

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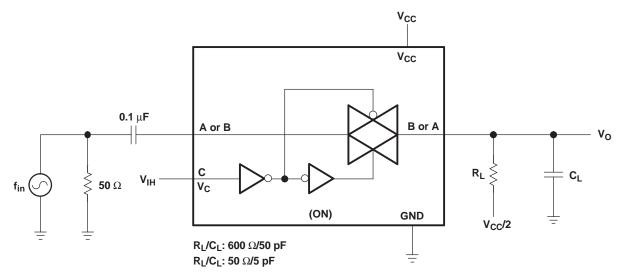


Figure 5. Frequency Response (Switch ON)

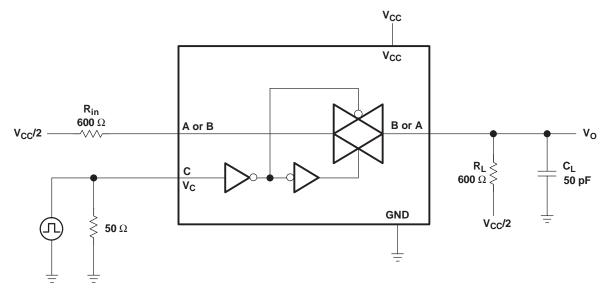


Figure 6. Crosstalk (Control Input – Switch Output)



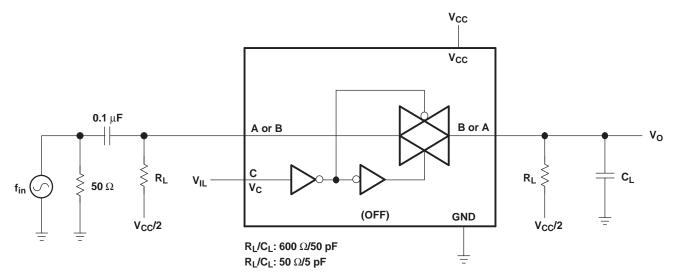


Figure 7. Feedthrough (Switch OFF)

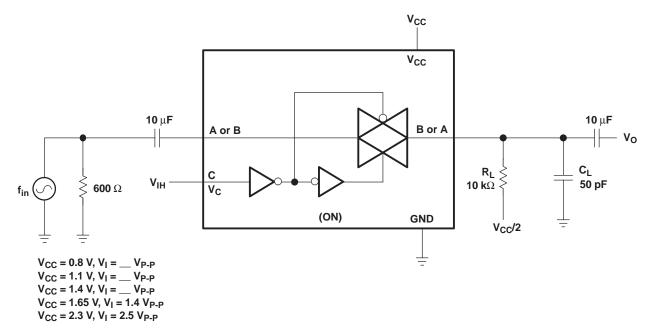


Figure 8. Sine-Wave Distortion

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AUC1G66DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(U66F, U66R)
SN74AUC1G66DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U66F, U66R)
SN74AUC1G66DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U66F
SN74AUC1G66DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U65, U6F, U6R)
SN74AUC1G66DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U65, U6F, U6R)
SN74AUC1G66YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U6N
SN74AUC1G66YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U6N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G66DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC1G66DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUC1G66DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUC1G66DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUC1G66DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUC1G66YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G66DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUC1G66DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AUC1G66DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUC1G66DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUC1G66DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUC1G66YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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