SCES092F-JANUARY 1997-REVISED OCTOBER 2004

#### **FEATURES**

- Member of the Texas Instruments Widebus™
   Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

### **DESCRIPTION/ORDERING INFORMATION**

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH162374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

The output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

#### DGG OR DL PACKAGE (TOP VIEW)

10E	] <sub>1</sub>	48	] 1CLK
1Q1	2	47	] 1D1
1Q2	3	46	] 1D2
GND [	4	45	GND
1Q3 [	5	44	] 1D3
1Q4 [	6	43	] 1D4
v <sub>cc</sub> [	7	42	] v <sub>cc</sub>
1Q5	8	41	] 1D5
1Q6	9	40	] 1D6
GND [	10	39	GND
1Q7	11	38	] 1D7
1Q8 [	12	37	] 1D8
2Q1	13	36	2D1
2Q2	14	35	] 2D2
GND [		34	GND
2Q3	16	33	2D3
2Q4 [	17	32	2D4
V <sub>CC</sub> [	18	31	] v <sub>cc</sub>
2Q5 [	19	30	2D5
2Q6	20	29	2D6
GND [	21	28	GND
2Q7	22	27	2D7
2Q8 [	23	26	2D8
2 <del>0E</del> [	24	25	] 2CLK
			l

The outputs, which are designed to sink up to 12 mA, include equivalent 26- $\Omega$  resistors to reduce overshoot and undershoot.

#### ORDERING INFORMATION

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	SSOP - DL	Tube	SN74ALVCH162374DL	ALVCH162374		
-40°C to 85°C			SN74ALVCH162374DLR	ALVCH102374		
	TSSOP - DGG	Tape and reel	SN74ALVCH162374GR	ALVCH162374		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

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# **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

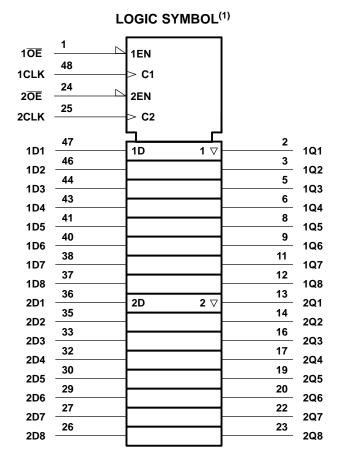
To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

# FUNCTION TABLE (each flip-flop)

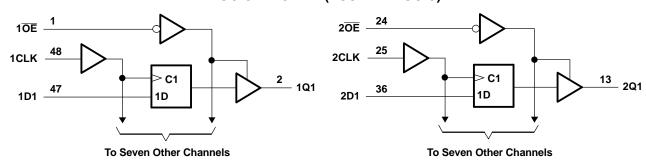
	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	$\uparrow$	L	L
L	H or L	Χ	$Q_0$
Н	Χ	Χ	Z

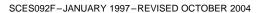
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(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### **LOGIC DIAGRAM (POSITIVE LOGIC)**







### ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
VI	Input voltage range (2)				
Vo	Output voltage range <sup>(2)(3)</sup>		-0.5	$V_{CC} + 0.5$	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current		-50	mA	
Io	Continuous output current			±50	mA
	Continuous current through each V <sub>CC</sub> or GNE	)		±100	mA
0	Dackage thermal impedence (4)	DGG package		89	°C/W
$\theta_{JA}$	Package thermal impedance (4)	DL package		94	C/VV
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# **RECOMMENDED OPERATING CONDITIONS**(1)

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage		1.65	3.6	V	
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>			
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2			
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V	
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V	
Vo	Output voltage		0	V <sub>CC</sub>	V	
		V <sub>CC</sub> = 1.65 V		-2		
	I Park Town Louds of Summer	V <sub>CC</sub> = 2.3 V		-6	mA	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		-8		
		V <sub>CC</sub> = 3 V		-12		
		V <sub>CC</sub> = 1.65 V		2		
	Laurianal antent annest	V <sub>CC</sub> = 2.3 V		6		
l <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V	8		mA	
		V <sub>CC</sub> = 3 V				
Δt/Δν	Input transition rise or fall rate	,		10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> This value is limited to 4.6 V maximum.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51.



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### **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2				
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
$V_{OH}$	$V_{OH}$	L 6 mA	2.3 V	1.7			V	
		I <sub>OH</sub> = -6 mA	3 V	2.4				
		I <sub>OH</sub> = -8 mA	2.7 V	2				
	V <sub>OL</sub>	I <sub>OH</sub> = -12 mA	3 V	2				
		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2		
		I <sub>OL</sub> = 2 mA	1.65 V			0.45		
		I <sub>OL</sub> = 4 mA	2.3 V			0.4		
$V_{OL}$			2.3 V			0.55	V	
		I <sub>OL</sub> = 6 mA	3 V			0.55		
V <sub>OL</sub> I <sub>I</sub>	I <sub>OL</sub> = 8 mA	2.7 V			0.6			
	I <sub>OL</sub> = 12 mA	3 V			0.8			
I <sub>I</sub>		$V_I = V_{CC}$ or GND	3.6 V			±5	μΑ	
		V <sub>I</sub> = 0.58 V	1.65 V	25				
		V <sub>I</sub> = 1.07 V	1.65 V	-25				
		V <sub>I</sub> = 0.7 V	2.3 V	45				
I <sub>I(hold)</sub>		V <sub>I</sub> = 1.7 V	2.3 V	-45			μΑ	
, ,		V <sub>I</sub> = 0.8 V	3 V	75				
		V <sub>I</sub> = 2 V	3 V	-75				
		V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V			±500		
l <sub>OZ</sub>		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ	
I <sub>CC</sub>		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
$\Delta I_{CC}$		One input at $V_{CC}$ - 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	V V CND	221/		3			
C <sub>i</sub>	Data inputs	$V_I = V_{CC}$ or GND	3.3 V		6		pF	
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7		pF	

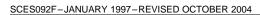
### **TIMING REQUIREMENTS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 1.8 V		$V_{CC}$ = 2.5 V $\pm$ 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency		(1)		150		150		150	MHz	
t <sub>w</sub>	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns	
t <sub>su</sub>	Setup time, data before CLK↑	(1)		2.1		2.2		1.9		ns	
t <sub>h</sub>	Hold time, data after CLK↑	(1)		0.6		0.5		0.5		ns	

<sup>(1)</sup> This information was not available at the time of publication.

All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ . This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.





### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1	V <sub>CC</sub> = 1.8 V		$V_{CC}$ = 2.5 V $\pm$ 0.2 V		V <sub>CC</sub> = 2.7 V		$V_{CC}$ = 3.3 V $\pm$ 0.3 V	
	(INFOI)	(OUTPUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			(1)		150		150		150		MHz
t <sub>pd</sub>	CLK	Q		(1)	1	5.4		5.4	1	4.6	ns
t <sub>en</sub>	ŌĒ	Q		(1)	1	6.5		6.4	1	5.2	ns
t <sub>dis</sub>	ŌĒ	Q		(1)	1	5.6		5	1.2	4.5	ns

<sup>(1)</sup> This information was not available at the time of publication.

### **OPERATING CHARACTERISTICS**

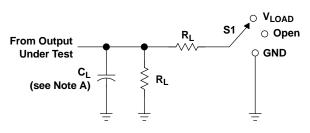
 $T_A = 25^{\circ}C$ 

PARAMETER	PARAMETER			V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	UNIT	
C Power dissination constitutes	Outputs enabled	C 0 f 10 MHz	(1)	28	31	۰	
C <sub>pd</sub> Power dissipation capacitance	Outputs disabled	$C_L = 0$ , $f = 10 \text{ MHz}$	(1)	10	11	pF	

<sup>(1)</sup> This information was not available at the time of publication.



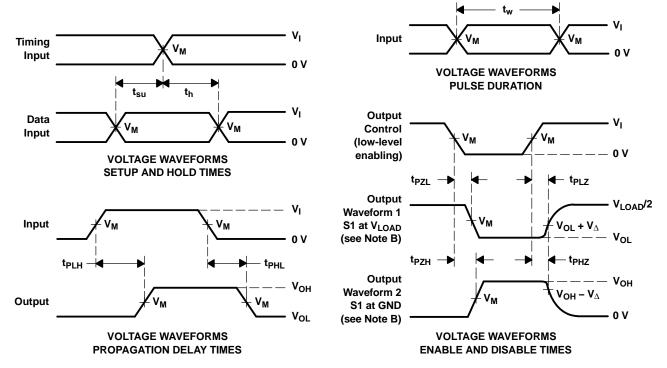
### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>pd</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

LOAD CIRCUIT

V	INPUT		V	v	•	ь	V
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	R <sub>L</sub>	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	V <sub>CC</sub>	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\Omega} = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74ALVCH162374DL	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162374
SN74ALVCH162374DL.B	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162374
SN74ALVCH162374DLR	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162374
SN74ALVCH162374DLR.B	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162374
SN74ALVCH162374GR	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162374
SN74ALVCH162374GR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162374

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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# **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVCH162374GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162374DLR	SSOP	DL	48	1000	356.0	356.0	53.0
SN74ALVCH162374GR	TSSOP	DGG	48	2000	356.0	356.0	45.0

# **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALVCH162374DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ALVCH162374DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

# DL (R-PDSO-G48)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.





SMALL OUTLINE PACKAGE



### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



### DGG (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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