SDAS027B - APRIL 1984 - REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

### description

This 8-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus.

The eight latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs.

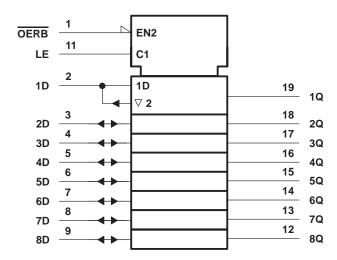
(TOP VIEW) **OERB** 20 🛮 V<sub>CC</sub> 1D 2 19 1Q 2D 3 18 2Q 17 3Q 3D 4D 5 16 4Q 15 5Q 5D 14 6Q 6D 13**∏** 7Ω 7D 8 8D 9 12 8Q 10 11 🛮 LE GND

**DW OR N PACKAGE** 

Read back is provided through the output-enable (OERB) input. When OERB is taken low, the data present at the output of the data latches is allowed to pass back onto the input data bus. When OERB is taken high, the output of the data latches is isolated from the D inputs. OERB does not affect the internal operation of the latches; however, precautions should be taken not to create a bus conflict.

The SN74ALS990 is characterized for operation from 0°C to 70°C.

## logic symbol†

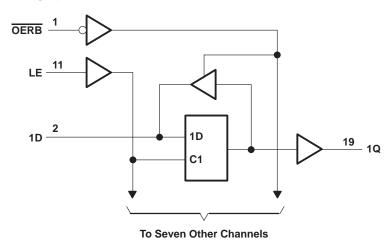


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

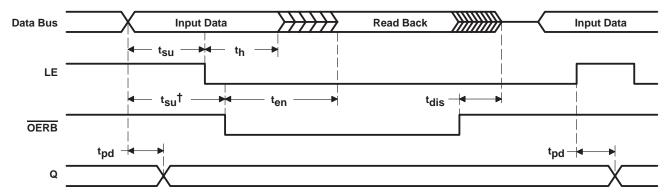


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## logic diagram (positive logic)



#### timing diagram



<sup>†</sup> This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub> (OERB and LE)	7 V
Voltage applied to D inputs	5.5 V
Operating free-air temperature range, T <sub>A</sub>	$\dots$ $$ 0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



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## recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V	
VIH						V
V <sub>IL</sub>	V <sub>IL</sub> Low-level input voltage				0.8	V
I i i i i i i i i i i i i i i i i i i i		Q			-2.6	mA
IOH	High-level output current	D			-0.4	mA
la.	Low level output ourrant	Q			24	mA
OL	Low-level output current	D			8	IIIA
t <sub>W</sub>	Pulse duration, LE high		10			ns
	Catua tima	Data before LE↓	10			
t <sub>SU</sub> Setup time		Data before OERB↓	10			ns
th	Hold time, data after LE↓		5			ns
T <sub>A</sub>	Operating free-air temperature		0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CON	DITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{I} = -18 \text{ mA}$			-1.2	V
.,	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2			.,
VOH	Q	V <sub>CC</sub> = 4.5 V,	$I_{OH} = -2.6 \text{ mA}$	2.4	3.2		V
		V 45V	I <sub>OL</sub> = 4 mA		0.25	0.4	
\ <sub>\\\\\\</sub>	D	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 8 mA		0.35	0.5	V
VOL		V 45V	I <sub>OL</sub> = 12 mA		0.25	0.4	V
	Q	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 24 mA		0.35	0.5	
	OERB, LE	V	V <sub>I</sub> = 5.5 V			0.1	mA
Ч	D inputs	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V			0.1	IIIA
	OERB, LE	V00 - 5 5 V	V <sub>I</sub> = 2.7 V			20	
ΊΗ	D inputs‡	V <sub>CC</sub> = 5.5 V,	V  = 2.7 V			20	μΑ
	OERB, LE	V00 - 5 5 V	\\\ 0.4 \\			-0.1	mA
IIL	D inputs‡	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.1	IIIA
IO§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	mA
		<u>VCC</u> = 5.5 V,	Outputs high		27	50	mA
Icc		OERB high	Outputs low		40	70	IIIA

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> For I/O ports (Q<sub>A</sub> thru Q<sub>H</sub>), the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>§</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

## **SN74ALS990** 8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

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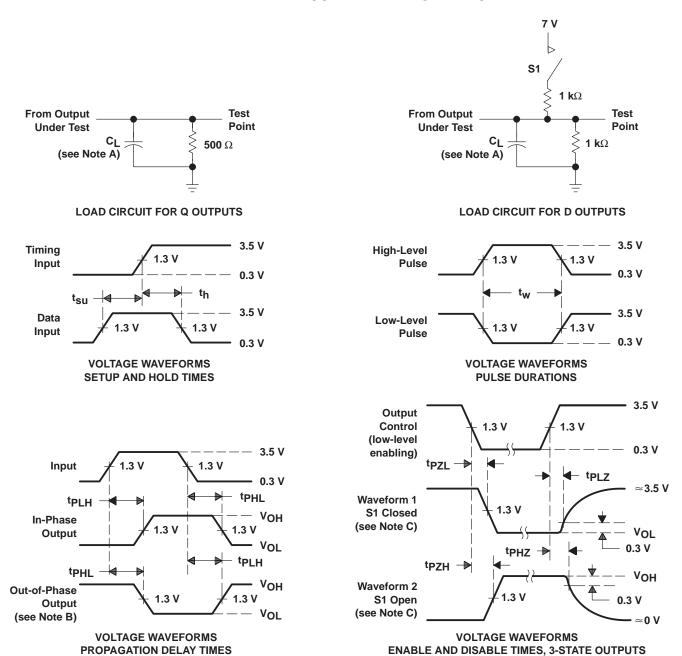
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 C <sub>L</sub> = 50 pF T <sub>A</sub> = MIN to	UNIT	
			MIN	MAX	
tPLH	D		4	17	20
<sup>t</sup> PHL	ט	Q	5	24	ns
<sup>t</sup> PLH	LE		6	26	ne
<sup>t</sup> PHL	LL	Q	8	26	ns
t <sub>en</sub> ‡	OERB	D	4	21	ns
t <sub>dis</sub> §	OERB	D	4	19	ns

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

t<sub>en</sub> = t<sub>PZH</sub> or t<sub>PZL</sub> t<sub>dis</sub> = t<sub>PHZ</sub> or t<sub>PLZ</sub>

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_{\Gamma}$  =  $t_{f}$  = 2 ns, duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74ALS990DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	ALS990
SN74ALS990DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS990
SN74ALS990DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS990
SN74ALS990N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS990N
SN74ALS990N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS990N

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS990DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

# **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
I	SN74ALS990DWR	SOIC	DW	20	2000	356.0	356.0	45.0	

# **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS990N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS990N.A	N	PDIP	20	20	506	13.97	11230	4.32

# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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