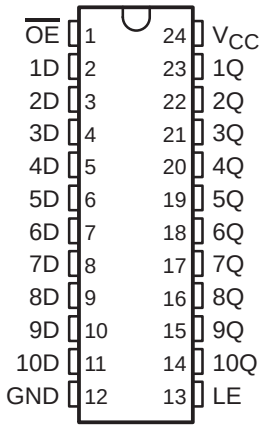
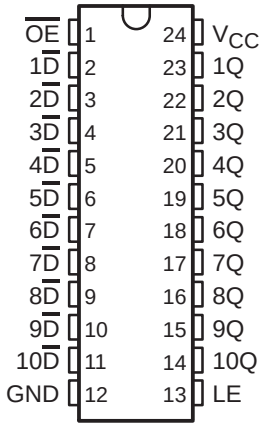
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Buffered Control Inputs to Reduce dc Loading Effects**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

SN74ALS841, SN74AS841A . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS842 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The SN74ALS841 and SN74AS841A have noninverting data (D) inputs. The SN74ALS842 has inverting $\overline{D}$ inputs.

A buffered output-enable ($\overline{OE}$) input places the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS841, SN74AS841A, and SN74ALS842 are characterized for operation from 0°C to 70°C.

Function Tables

SN74ALS841, SN74AS841A

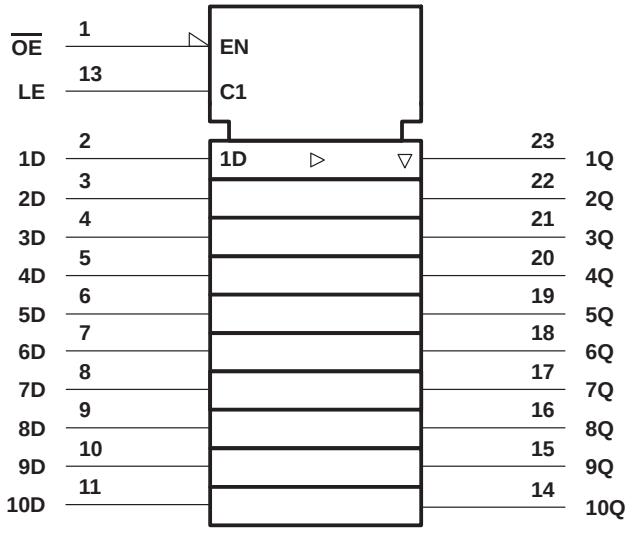
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN74ALS842

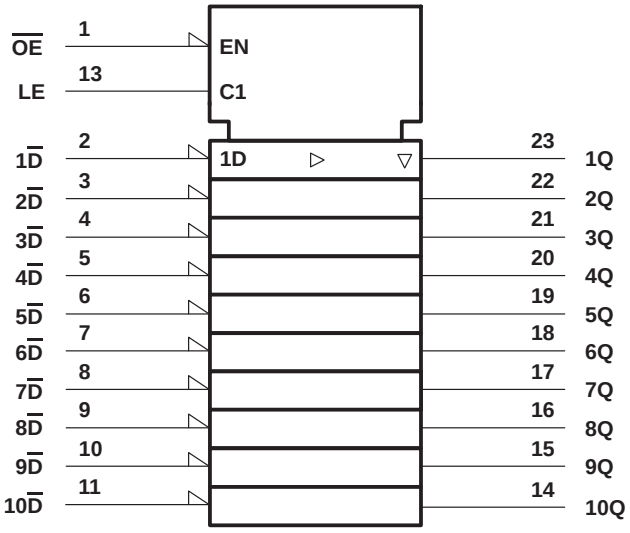
INPUTS			OUTPUT
$\overline{OE}$	LE	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbols†

SN74ALS841, SN74AS841A



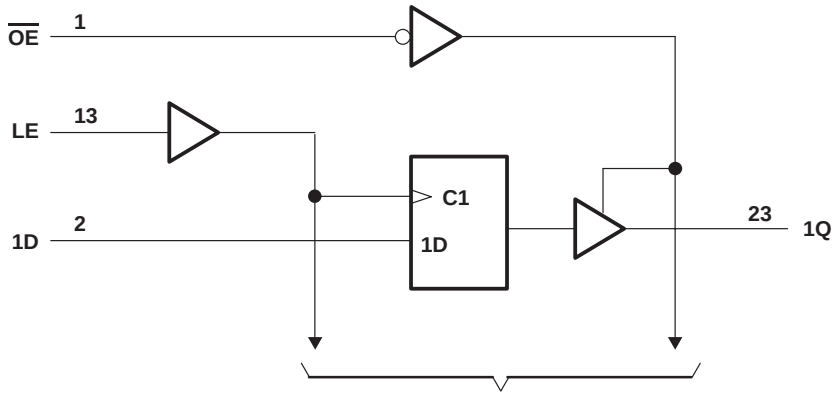
SN74ALS842



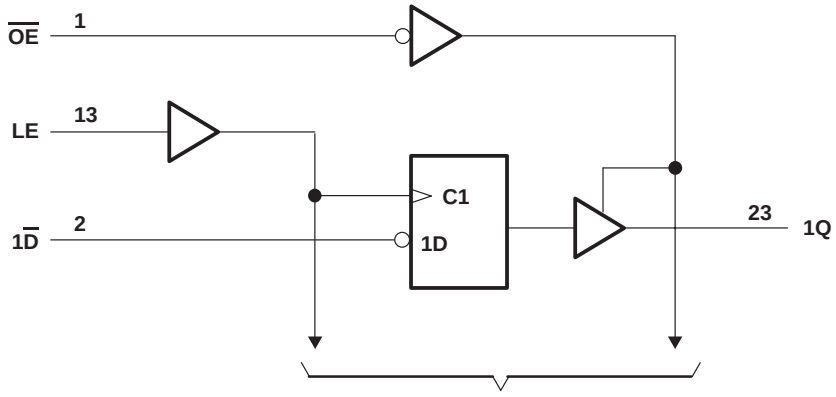
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74ALS841, SN74AS841A



SN74ALS842



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74ALS841, SN74ALS842 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS841 SN74ALS842			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, LE high	20			ns
t_{su}	Setup time, data before LE↓	10			ns
t_h	Hold time, data after LE↓	5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS841 SN74ALS842			UNIT
				MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V
		V_{CC} = 4.5 V,	I_{OH} = –2.6 mA	2.4	3.2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–20	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	SN74ALS841	V_{CC} = 5.5 V	Outputs high		19	30	mA
			Outputs low		38	62	
			Outputs disabled		23	40	
	SN74ALS842	V_{CC} = 5.5 V	Outputs high		20	35	
			Outputs low		48	74	
			Outputs disabled		27	44	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74ALS841		
			MIN	MAX	
t_{PLH}	D	Q	2	13	ns
t_{PHL}			2	13	
t_{PLH}	LE	Q	7	21	ns
t_{PHL}			8	26	
t_{PZH}	$\overline{OE}$	Q	2	12	ns
t_{PZL}			2	12	
t_{PHZ}	$\overline{OE}$	Q	2	10	ns
t_{PLZ}			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74ALS842		
			MIN	MAX	
t_{PLH}	$\overline{D}$	Q	4	18	ns
t_{PHL}			3	13	
t_{PLH}	LE	Q	8	27	ns
t_{PHL}			6	20	
t_{PZH}	$\overline{OE}$	Q	2	12	ns
t_{PZL}			2	12	
t_{PHZ}	$\overline{OE}$	Q	1	10	ns
t_{PLZ}			2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74AS841A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS841A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, LE high	4			ns
t_{su}	Setup time, data before LE↓	2.5			ns
t_h	Hold time, data after LE↓	2.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS841A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V
	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4	3.2		
		I_{OH} = –24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		36	60	mA
		Outputs low		58	94	
		Outputs disabled		56	93	

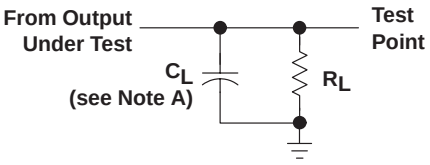
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

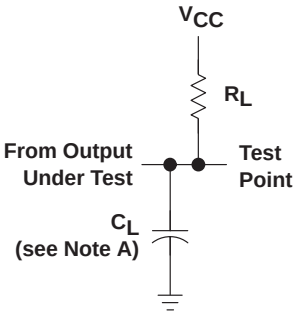
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74AS841A		
			MIN	MAX	
t_{PLH}	D	Q	1	6.5	ns
t_{PHL}			1	10.5	
t_{PLH}	LE	Q	2	12	ns
t_{PHL}			2	12	
t_{PZH}	$\overline{OE}$	Q	2	14	ns
t_{PZL}			2	16	
t_{PHZ}	$\overline{OE}$	Q	1	8	ns
t_{PLZ}			1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

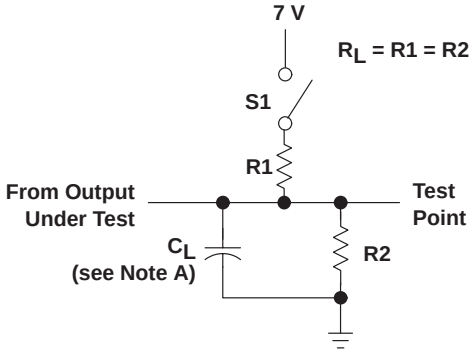
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



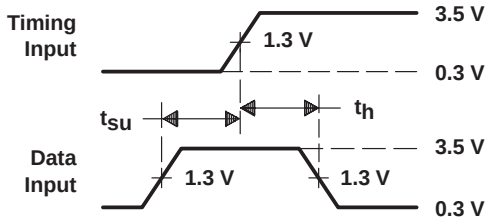
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



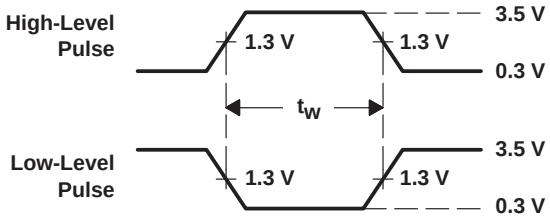
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



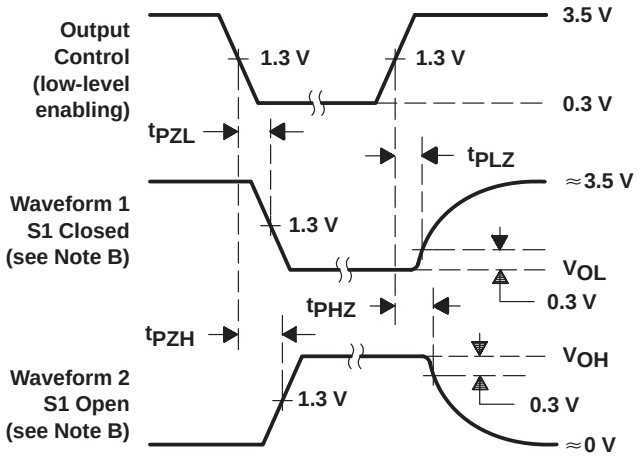
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



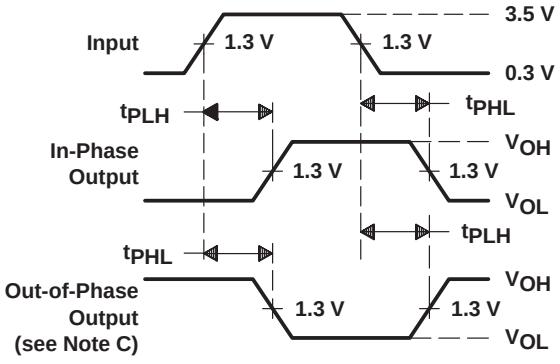
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS841DW	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS841
SN74ALS841DW.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS841

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

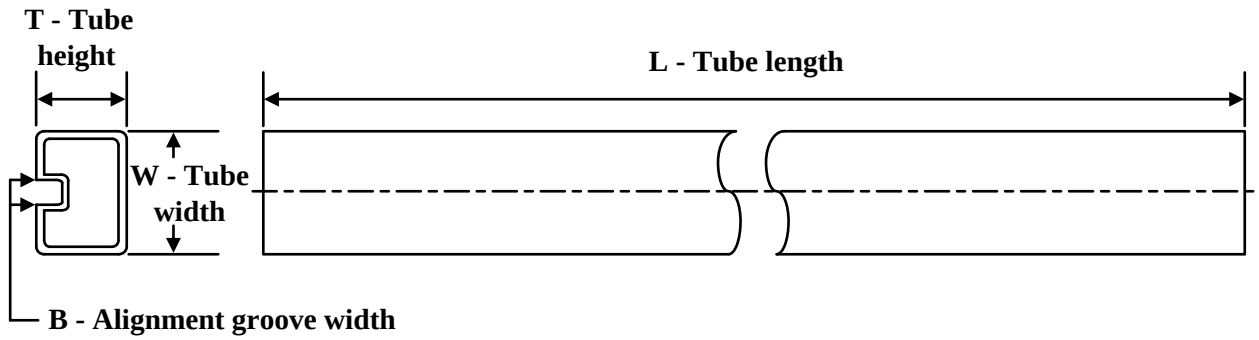
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

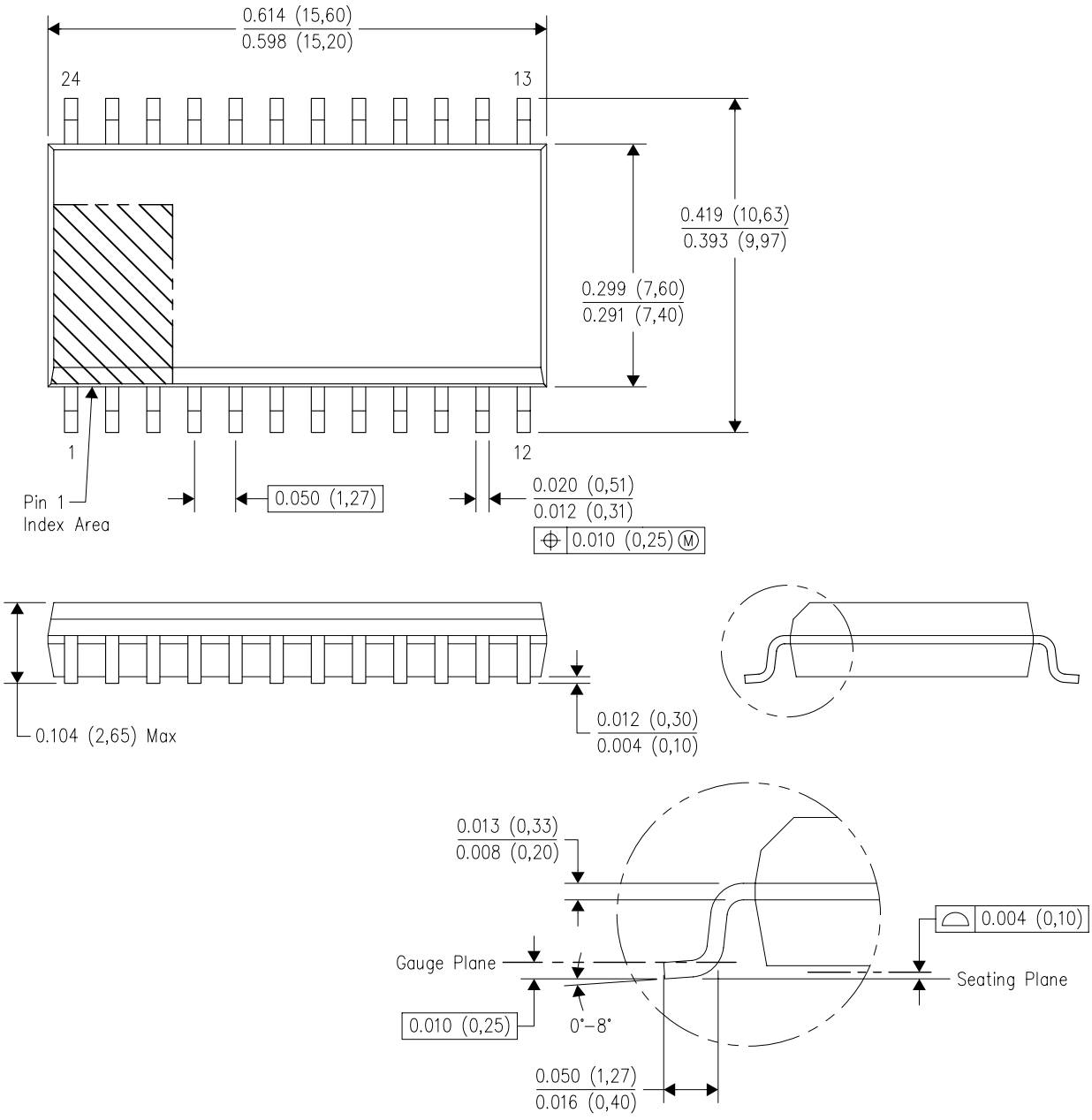
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS841DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS841DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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Last updated 10/2025