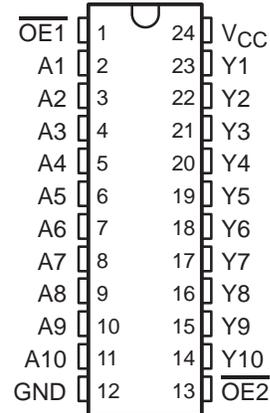


SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

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- Functionally Equivalent to AMD's AM29827 and AM29828
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

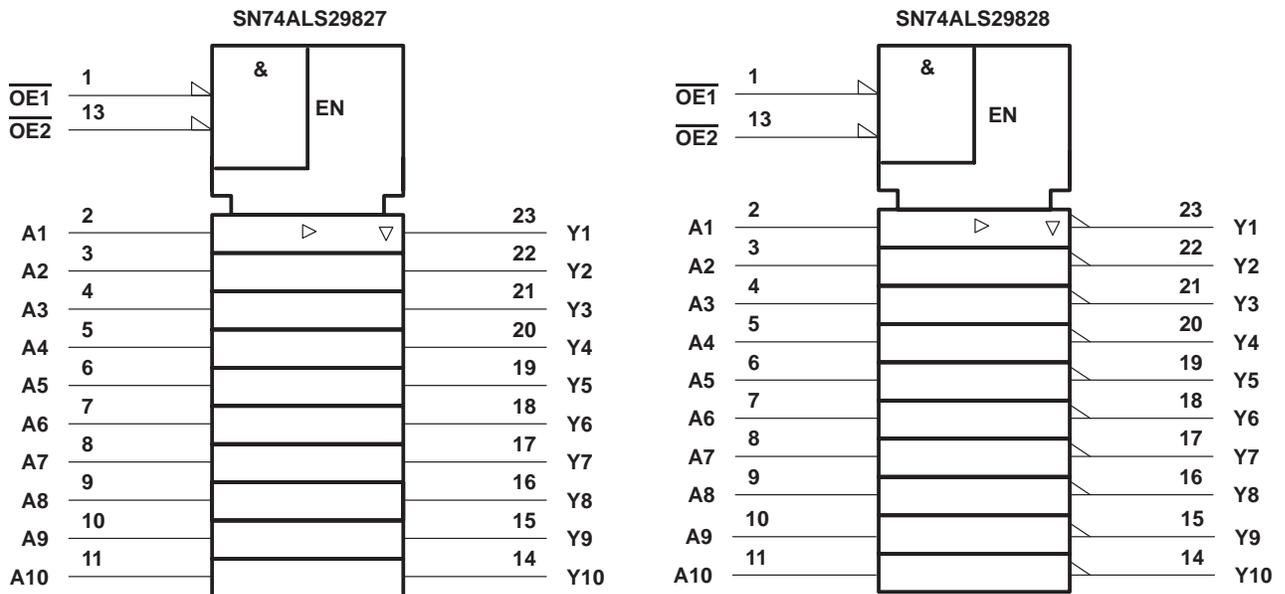
These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all ten outputs are in the high-impedance state.

The SN74ALS29827 provides true data and the SN74ALS29828 provides inverted data at their respective outputs.

The SN74ALS29827 and SN74ALS29828 are characterized for operation from 0°C to 70°C.

logic symbols†

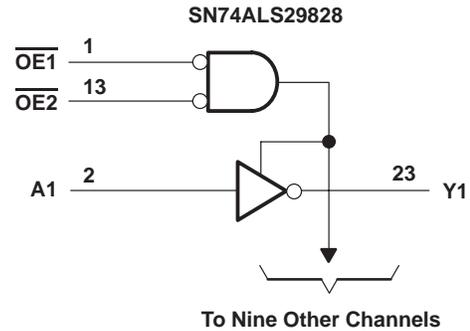
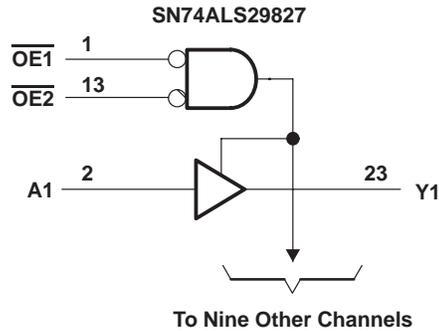


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

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logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS29827 SN74ALS29828			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

SN74ALS29827, SN74ALS29828
10-BIT BUFFERS AND BUS DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS29827 SN74ALS29828			UNIT
			MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.75\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.75\text{ V}$	$I_{OH} = -15\text{ mA}$	2.4			V
		$I_{OH} = -24\text{ mA}$	2			
V_{OL}	$V_{CC} = 4.75\text{ V}$,	$I_{OL} = 48\text{ mA}$	0.35	0.5		V
I_{OZH}	$V_{CC} = 5.25\text{ V}$,	$V_O = 2.4\text{ V}$			20	μA
I_{OZL}	$V_{CC} = 5.25\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
I_I	$V_{CC} = 5.25\text{ V}$,	$V_I = 5.5\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.25\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.25\text{ V}$,	$V_I = 0.4\text{ V}$			-0.1	mA
I_{OS}^\ddagger	$V_{CC} = 5.25\text{ V}$,	$V_O = 0$	-75		-250	mA
I_{CC}	$V_{CC} = 5.25\text{ V}$		25	40		mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

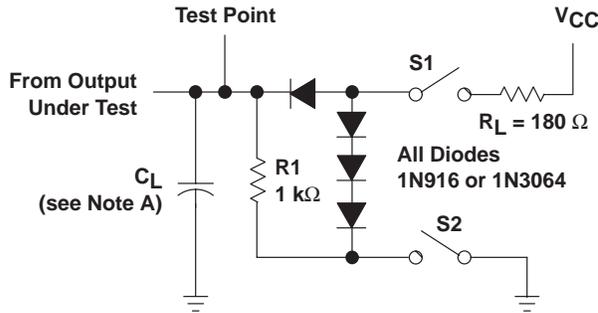
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 4.75\text{ V to }5.25\text{ V}$				UNIT
				SN74ALS29827		SN74ALS29828		
				MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 300\text{ pF}$	15		14		ns
t_{PHL}				15		14		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	8		7		ns
t_{PHL}				8		7.5		
t_{PZH}	\overline{OE}	Y	$C_L = 300\text{ pF}$	20		20		ns
t_{PZL}				23		23		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	15		15		ns
t_{PZL}				15		15		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	17		17		ns
t_{PLZ}				12		12		
t_{PHZ}	\overline{OE}	Y	$C_L = 5\text{ pF}$	9		9		ns
t_{PLZ}				9		9		

SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

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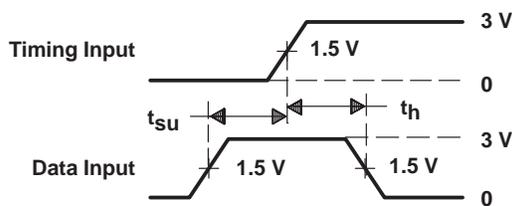
PARAMETER MEASUREMENT INFORMATION



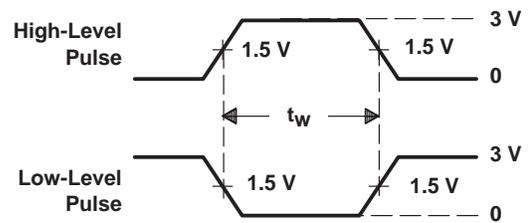
LOAD CIRCUIT

SWITCH POSITION TABLE

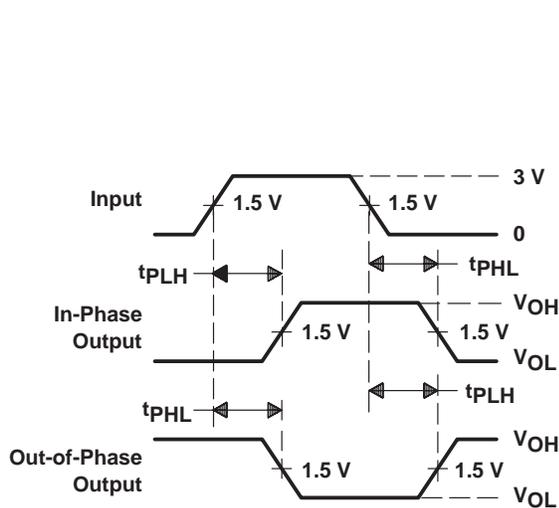
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



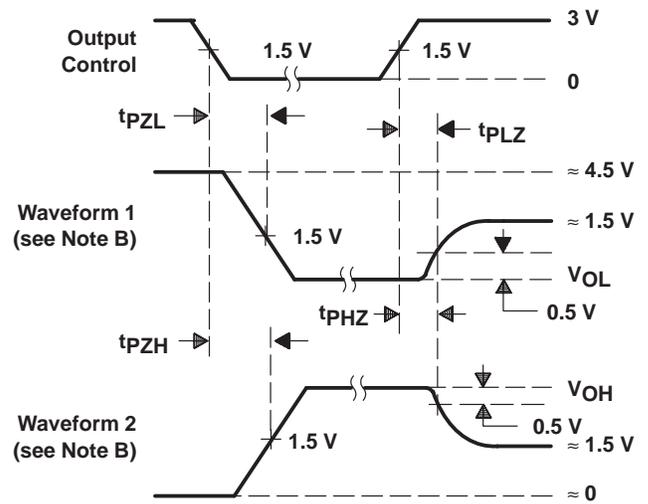
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS29827DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS29827
SN74ALS29827DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS29827

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

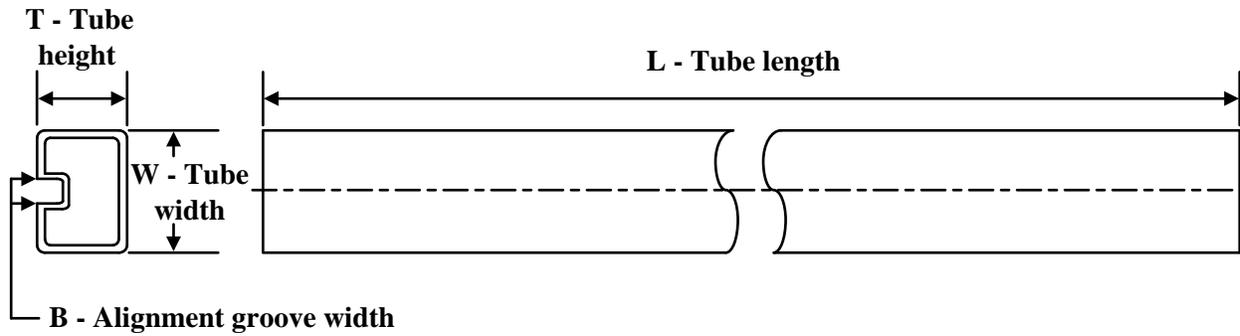
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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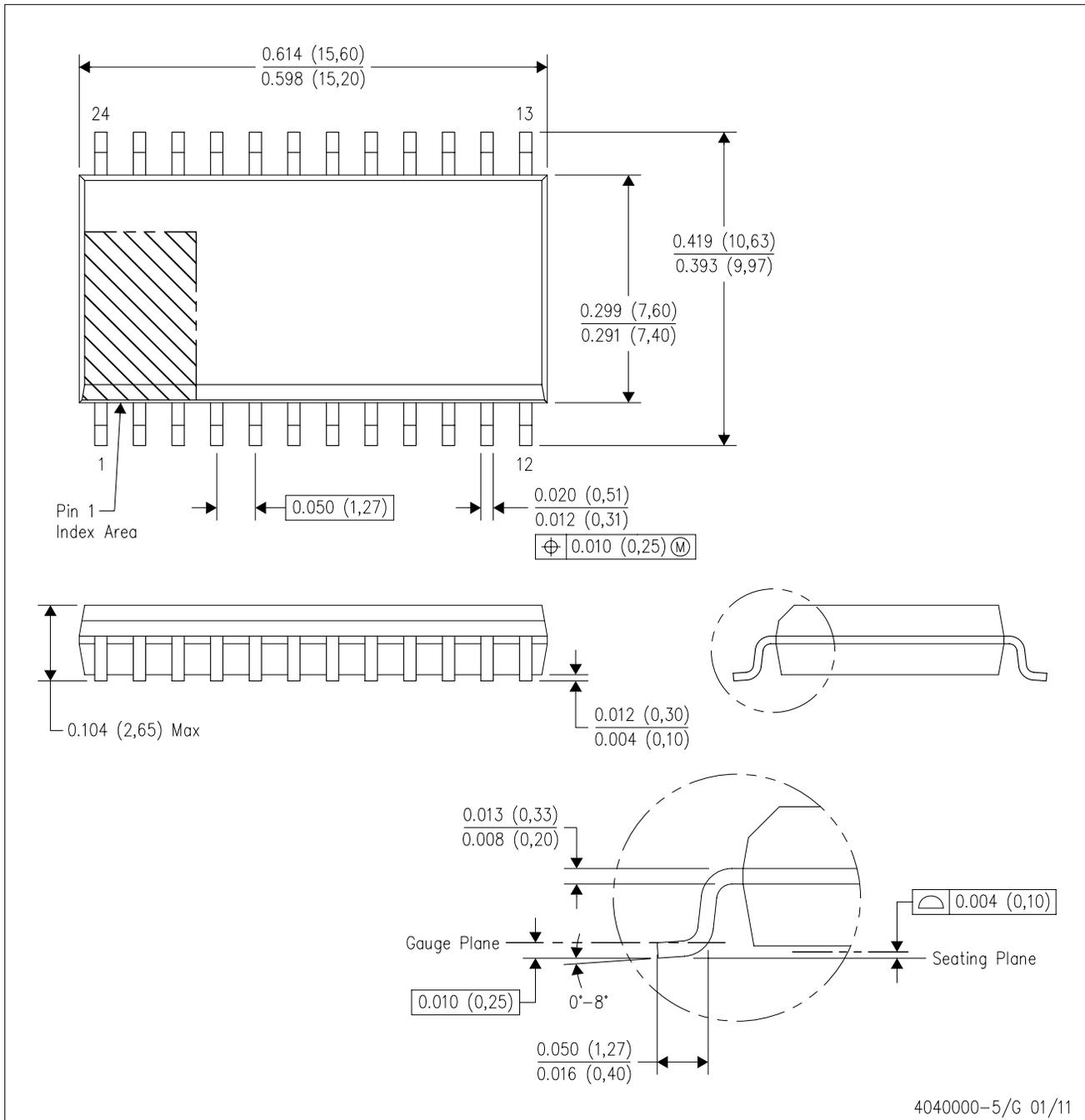
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS29827DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS29827DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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