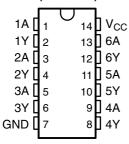
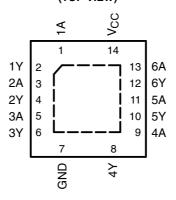
- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Unbuffered Outputs
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

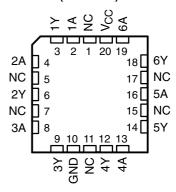
SN54AHCU04 . . . J OR W PACKAGE SN74AHCU04 . . . D, DB, DGV, N, NS, OR PW PACKAGE (TOP VIEW)



SN74AHCU04...RGY PACKAGE (TOP VIEW)



SN54AHCU04 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

## description/ordering information

The 'AHCU04 devices contain six independent inverters. These devices perform the Boolean function  $Y = \overline{A}$ . Internal circuitry consists of single-stage inverters that can be used in analog applications such as crystal oscillators.

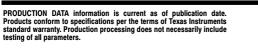
#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKA	.GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Tape and reel	SN74AHCU04RGYR	HD04
	PDIP – N	Tube	SN74AHCU04N	SN74AHCU04N
–40°C to 85°C	COIC D	Tube	SN74AHCU04D	ALICUO4
	SOIC – D	Tape and reel	SN74AHCU04DR	AHCU04
	SOP – NS	Tape and reel	SN74AHCU04NSR	AHCU04
	SSOP – DB	Tape and reel	SN74AHCU04DBR	HD04
	TOOOD DW	Tube	SN74AHCU04PW	LIDO4
	TSSOP – PW	Tape and reel	SN74AHCU04PWR	HD04
	TVSOP – DGV	Tape and reel	SN74AHCU04DGVR	HD04
	CDIP – J	Tube	SNJ54AHCU04J	SNJ54AHCU04J
–55°C to 125°C	CFP – W	Tube	SNJ54AHCU04W	SNJ54AHCU04W
	LCCC - FK	Tube	SNJ54AHCU04FK	SNJ54AHCU04FK

<sup>&</sup>lt;sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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# FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, V <sub>O</sub> (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-5.



# recommended operating conditions (see Note 4)

			SN54AH	ICU04	SN74AH	ICU04	
			MIN	MAX	MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	2	5.5	V
		V <sub>CC</sub> = 2 V	1.7		1.7		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.4		2.4		V
		V <sub>CC</sub> = 5.5 V	4.4		4.4		
		V <sub>CC</sub> = 2 V		0.3		0.3	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.6		0.6	V
		V <sub>CC</sub> = 5.5 V		1.1		1.1	
VI	Input voltage		0	5.5	0	5.5	V
Vo	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
		V <sub>CC</sub> = 2 V		-50		-50	μΑ
I <sub>OH</sub>	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8		-8	
		V <sub>CC</sub> = 2 V		50		50	μΑ
l <sub>OL</sub>	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4		4	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		8		8	mA
T <sub>A</sub>	Operating free-air temperature	•	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEGT COMPLETIONS	.,	T,	գ = 25°C	;	SN54AH	ICU04	SN74AH	ICU04	
PARAMETER	TEST CONDITIONS	v <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.8	2		1.8		1.8		
	$I_{OH} = -50 \mu A$	3 V	2.7	3		2.7		2.7		
V <sub>ОН</sub>		4.5 V	4	4.5		4		4		٧
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
		2 V			0.2		0.2		0.2	
	$I_{OL} = 50 \mu A$	3 V			0.3		0.3		0.3	
V <sub>OL</sub>		4.5 V			0.5		0.5		0.5	٧
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

 $<sup>^{\</sup>star}$  On products compliant to MIL-PRF-38535, this parameter is not production tested at  $V_{CC}$  = 0 V.

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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCU04		SN74AH	LINUT	
PARAMETER	(INPUT)			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	•	V	0 45 -5		5*	7.1*	1*	8.5*	1	8.5	
t <sub>PHL</sub>	A	Y	$C_L = 15 pF$		5*	7.1*	1*	8.5*	1	8.5	ns
t <sub>PLH</sub>	Α	V	C <sub>I</sub> = 50 pF		7.5	10.6	1	12	1	12	ns
t <sub>PHL</sub>		A T	OL = 30 pr		7.5	10.6	1	12	1	12	115

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCU04		SN74AHCU04		LINUT
PARAMETER	(INPUT)	(OUTPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t <sub>PLH</sub>	•	V	0 455		3.5*	5.5*	1*	6*	1	6.5	
t <sub>PHL</sub>	A	Y	$C_L = 15 pF$		3.5*	5.5*	1*	6*	1	6.5	ns
t <sub>PLH</sub>	Δ.	V	C - 50 pE		5	7	1	8	1	8	no
t <sub>PHL</sub>	А	ī	C <sub>L</sub> = 50 pF		5	7	1	8	1	8	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

# noise characteristics, $V_{CC} = 5 \text{ V}$ , $C_L = 50 \text{ pF}$ , $T_A = 25^{\circ}\text{C}$ (see Note 5)

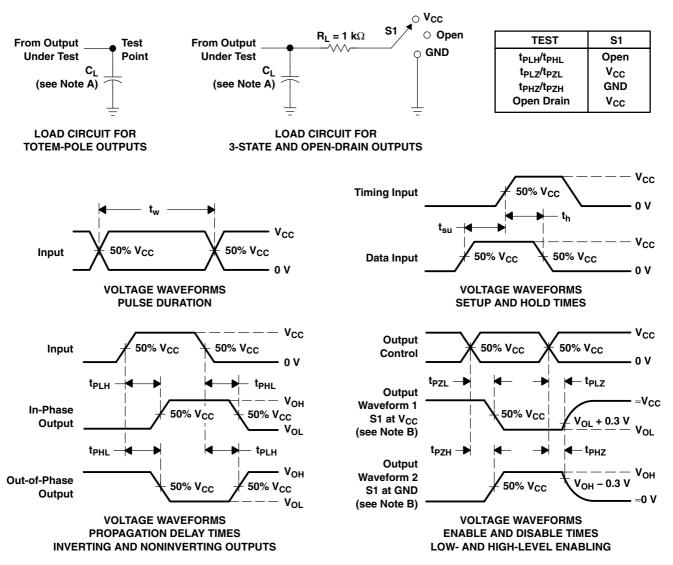
	DADAMETED	SN7	LINUT		
	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.5		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.5		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		4.3		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	4			V
$V_{IL(D)}$	Low-level dynamic input voltage			1	V

NOTE 5: Characteristics are for surface-mount packages only.

# operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load, f = 1 MHz	7.3	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9680301QDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680301QD A SNJ54AHCU04W
SN74AHCU04D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	AHCU04
SN74AHCU04DBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04
SN74AHCU04DBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04
SN74AHCU04DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04
SN74AHCU04DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04
SN74AHCU04N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCU04N
SN74AHCU04N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCU04N
SN74AHCU04NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04
SN74AHCU04NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04
SN74AHCU04PW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HD04
SN74AHCU04PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04
SN74AHCU04PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04
SN74AHCU04PWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04
SNJ54AHCU04W	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680301QD A SNJ54AHCU04W

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54AHCU04, SN74AHCU04:

Catalog: SN74AHCU04

Automotive: SN74AHCU04-Q1, SN74AHCU04-Q1

Enhanced Product: SN74AHCU04-EP, SN74AHCU04-EP

Military: SN54AHCU04

#### NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

**PACKAGE MATERIALS INFORMATION** 

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## TAPE AND REEL INFORMATION



## 

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCU04DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCU04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCU04NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHCU04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)				
SN74AHCU04DBR	SSOP	DB	14	2000	353.0	353.0	32.0				
SN74AHCU04DR	SOIC	D	14	2500	353.0	353.0	32.0				
SN74AHCU04NSR	SOP	NS	14	2000	353.0	353.0	32.0				
SN74AHCU04PWR	TSSOP	PW	14	2000	353.0	353.0	32.0				

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9680301QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHCU04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCU04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCU04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCU04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCU04W	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# W (R-GDFP-F14)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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