

SNx4AHCT541 Octal Buffers/Drivers With 3-State Outputs

1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD
- ESD protection exceeds JESD 22
 - 2000V human-body model (A114-A)
 - 1000V charged-device model (C101)
- On products compliant to MIL-PRF-38535. all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

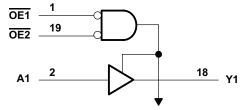
2 Description

The 'AHCT541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE(3)	
	N (PDIP, 20)	24.33mm x 9.4mm	25.40 mm x 6.35mm	
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm x 5.30mm	
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm x 4.40mm	
SNx4AHCT541	DGV (TVSOP, 20)	5.00mm x 6.4mm	5.00mm x 4.40mm	
	DW (SOIC, 20)	12.80 mm × 10.3 mm	12.80 mm x 7.50 mm	
	J (CDIP, 20)	24.2mm x 7.62mm	24.2mm x 6.92mm	
	W (CFP, 20)	13.09mm x 8.13mm	13.09mm x 6.92mm	

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



To Seven Other Channels

Logic Diagram, Each Flip-Flop (Positive Logic)



Table of Contents

1 Features	1	6.3 Device Functional Modes	7
2 Description	1	7 Application and Implementation	8
3 Pin Configuration and Functions	3	7.1 Power Supply Recommendations	8
4 Specifications	4	7.2 Layout	8
4.1 Absolute Maximum Ratings		8 Device and Documentation Support	
4.2 ESD Ratings	4	8.1 Device and Documentation Support	9
4.3 Recommended Operating Conditions		8.2 Receiving Notification of Documentation Updates	
4.4 Thermal Information	4	8.3 Support Resources	9
4.5 Electrical Characteristics	<mark>5</mark>	8.4 Trademarks	
4.6 Switching Characteristics	<mark>5</mark>	8.5 Electrostatic Discharge Caution	9
4.7 Operating Characteristics	5	8.6 Glossary	
5 Parameter Measurement Information		9 Revision History	9
6 Detailed Description	<mark>7</mark>	10 Mechanical, Packaging, and Orderable	
6.1 Overview		Information	. 10
6.2 Functional Block Diagram	<mark>7</mark>		



3 Pin Configuration and Functions

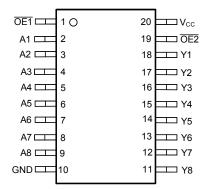


Figure 3-1. SN54AHCT541 J or W Package; SN74AHCT541 DB, DW, N, NS, or PW Package; 20-Pin SSOP, SOIC, PDIP, SOP, or TSSOP (Top View)

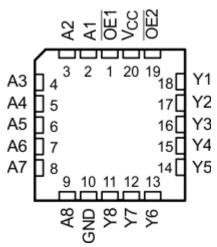


Figure 3-2. SN54AHCT541 FK Package, 20-Pin LCCC (Top View)

Table 3-1. Pin Functions

	PIN	1/0	DESCRIPTION
NO.	NAME	I/O	DESCRIPTION
1	ŌE1	ı	Output Enable 1
2	A1	ı	A1 Input
3	A2	1	A2 Input
4	A3	1	A3 Input
5	A4	1	A4 Input
6	A5	1	A5 Input
7	A6	ı	A6 Input
8	A7	ı	A7 Input
9	A8	1	A8 Input
10	GND	_	Ground
11	Y8	0	Y8 Output
12	Y7	0	Y7 Output
13	Y6	0	Y6 Output
14	Y5	0	Y5 Output
15	Y4	0	Y4 Output
16	Y3	0	Y3 Output
17	Y2	0	Y2 Output
18	Y1	0	Y1 Output
19	ŌE2	I	Output Enable 2
20	V _{CC}	_	Power Pin



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	Supply voltage range			
VI	Input voltage range ⁽²⁾	-0.5	7	V	
Vo	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-20	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V _{CC} or GND			±75	mA

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	v

⁽¹⁾ JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHCT541		SN74AHCT541		UNIT
		MIN	MAX	MIN	MIN MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level Input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δν	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.4 Thermal Information

		SN74AHCT541						
THERMAL METRIC ⁽¹⁾		DB (SSOP)	DGV (TVSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.2	92	81.1	69	60	116.8	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

						T _A = -55		T _A = -40		T _A = -40° 125°		
PARAMETER	TEST CONDITIONS	V _{cc}	Т	_A = 25°C	;	125°C		05 0		Recommended		UNIT
						SN54AHCT541		SN74AHCT541		SN74AHCT541		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50μA	4.5V	4.4	4.5		4.4		4.4		4.4		V
	I _{OH} = -8mA	4.50	3.94			3.8		3.8		3.8		\ \ \ \ \
V _{OL}	I _{OL} = 50μA	4.5V			0.1		0.1		0.1		0.1	V
	I _{OH} = 8mA	4.50			0.36		0.44		0.44		0.44	, '
I _I	V _I = 5.5V or GND	0V to 5.5V			±0.1		±1 ⁽¹⁾		±1		±1	μΑ
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	μΑ
I _{CC}	$V_1 = V_{CC}$ or $I_0 = 0$	5.5V			4		40		20		40	μΑ
ΔI _{CC} ⁽²⁾	One input at 3.4V, Other inputs at V _{CC} or GND	5.5V			1.35		1.5		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5V		2	10				10			pF
Co	V _O = V _{CC} or GND	5V		4								pF

On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0V$.

4.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Figure 5-1)

						T _A = -55		T _A = -40		T _A = -40 125°		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 2$	T _A = 25°C		125°C		85°C		ended	UNIT
	(INPUT)	(OUTPUT)	CAPACITANCE					SN54AH	CT541			
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	А	Y	C _L = 15pF	4.1 ⁽¹⁾	6.0 <mark>(1)</mark>	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	6.5	ns
t _{PHL}	A	T	CL - 13pr	4.1 ⁽¹⁾	6.0 <mark>(1)</mark>	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	6.5	1115
t _{PZH}	ŌĒ	Y	C ₁ = 15pF	5.0 ⁽¹⁾	7.0 <mark>(1)</mark>	1 ⁽¹⁾	8.0(1)	1	8.0	1	8.0	ns
t _{PZL}		OE OE	Ť	C _L = 15pF	5.0 ⁽¹⁾	7.0 ⁽¹⁾	1 ⁽¹⁾	8.0(1)	1	8.0	1	8.0
t _{PHZ}	ŌĒ	Ē Y	Y C ₁ = 15pF	4.5 ⁽¹⁾	7.0 <mark>(1)</mark>	1 ⁽¹⁾	8.0(1)	1	8.0	1	8.0	ns
t _{PLZ}	OE .		С[– 13рі	4.5 ⁽¹⁾	7.0 <mark>(1)</mark>	1 ⁽¹⁾	8.0 ⁽¹⁾	1	8.0	1	8.0	115
t _{PLH}	Α	Υ	0 - 50-5	6.2	8.5	1	9.5	1	9.5	1	9.5	no
t _{PHL}		T	C _L = 50pF	6.2	8.5	1	9.5	1	9.5	1	9.5	ns
t _{PZH}	ŌĒ	Υ	C = 50pE	7.5	10.0	1	12	1	12	1	12	no
t _{PZL}	OE .	T	C _L = 50pF	7.5	10.0	1	12	1	12	1	12	ns
t _{PHZ}	ŌĒ		C = 50pE	7.0	10.0	1	12	1	12	1	12	
t _{PLZ}	OE	Y	Y $C_L = 50pF$	7.0	10.0	1	12	1	12	1	12	ns
t _{sk(o)}			C _L = 50pF		1(2)				1	1		ns

 ⁽¹⁾ On products compliant to MIL-PRF-38535, this parameter is not production tested.
 (2) On products compliant to MIL-PRF-38535, this parameter does not apply.

4.7 Operating Characteristics

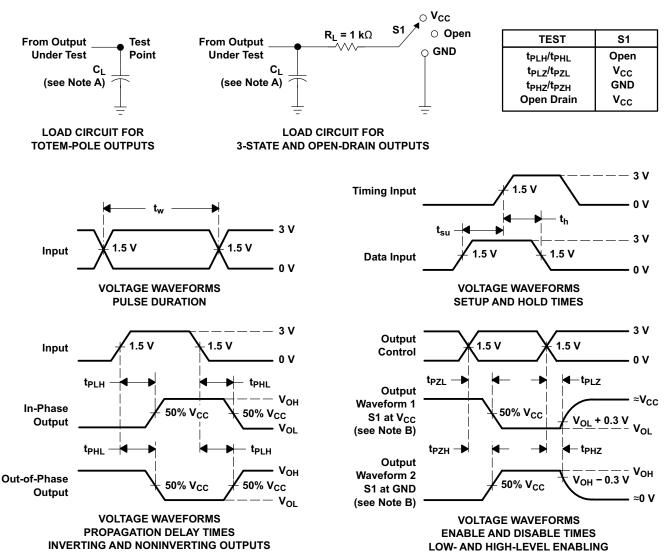
 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST	CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0V or V_{CC}.



5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms



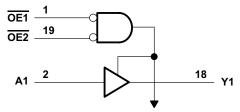
6 Detailed Description

6.1 Overview

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{\text{OE1}}$ or $\overline{\text{OE2}}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram



To Seven Other Channels

6.3 Device Functional Modes

Table 6-1 lists the functional modes for the SNx4AHCT541 devices.

Table 6-1. Function Table (Each Buffer/Driver)

	INPUTS	OUTPUT			
OE1	OE2	Α	Υ		
L	L	L	L		
L	L	Н	Н		
Н	Х	Х	Z		
Х	Н	Х	Z		

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Section 4.3 table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} terminals then 0.01 μ F or 0.022 μ F is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the Figure 7-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

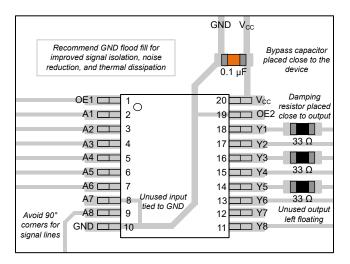


Figure 7-1. Example Layout for the SN74AHCT541



8 Device and Documentation Support

8.1 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT541	Click here	Click here	Click here	Click here	Click here
SN74AHCT541	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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	pdated RθJA values: PW = 83 to 116.8, DB = 70 to 87.2, DW = 58 to 81.1; Updated PW, DB, and D ackages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	
	and from Businian O (Into 2000) to Businian B (Into 2004)	
Chan	nges from Revision O (July 2003) to Revision P (June 2013)	Page
	nges from Revision O (July 2003) to Revision P (June 2013) xtended operating temperature range to 125°C	

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Submit Document Feedback

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9685801Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9685801Q2A SNJ54AHCT 541FK
5962-9685801QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J
5962-9685801QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685801QS A SNJ54AHCT541W
SN74AHCT541DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AHCT541, HB541)
SN74AHCT541DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AHCT541, HB541)
SN74AHCT541DGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541DGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	AHCT541
SN74AHCT541DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541
SN74AHCT541DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541
SN74AHCT541N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT541N
SN74AHCT541N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT541N
SN74AHCT541NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541
SN74AHCT541NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541
SN74AHCT541PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541PWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541PWRG3	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541PWRG3.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541PWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541
SN74AHCT541RKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54AHCT541FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9685801Q2A SNJ54AHCT 541FK
SNJ54AHCT541FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9685801Q2A SNJ54AHCT 541FK
SNJ54AHCT541J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J
SNJ54AHCT541J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J
SNJ54AHCT541W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685801QS A SNJ54AHCT541W
SNJ54AHCT541W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685801QS A SNJ54AHCT541W

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AHCT541, SN74AHCT541:

Catalog: SN74AHCT541

Automotive: SN74AHCT541-Q1, SN74AHCT541-Q1

Enhanced Product: SN74AHCT541-EP, SN74AHCT541-EP

Military: SN54AHCT541

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications



www.ti.com 7-Sep-2025

TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT541DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHCT541DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT541DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHCT541NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT541PWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT541PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT541PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT541RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1



www.ti.com 7-Sep-2025



*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT541DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHCT541DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHCT541DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT541DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT541NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHCT541PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT541PWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHCT541PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT541PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT541RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

PACKAGE MATERIALS INFORMATION

www.ti.com 7-Sep-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9685801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9685801QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT541N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHCT541N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT541FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT541FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT541W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHCT541W.A	W	CFP	20	25	506.98	26.16	6220	NA





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
- 5. Features may differ or may not be present.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025