









SN54AHCT157, SN74AHCT157

SCLS347L - MAY 1996 - REVISED APRIL 2024

SNx4AHCT157 Automotive Quadruple 2-Line to 1-Line Data Selectors Multiplexers

1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD

2 Description

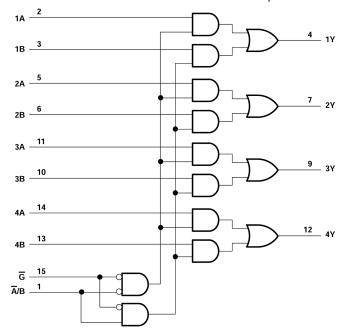
These quadruple 2-line to 1-line data selectors/ multiplexers are designed for 4.5V to 5.5V V_{CC} operation.

The SNx4AHCT157 devices feature a common strobe (\overline{G}) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
SNx4AHCT157	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
3NX4A1101137	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm

- For more information, see Section 10 (1)
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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3 Pin Configuration and Functions

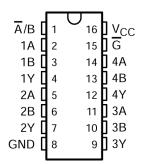
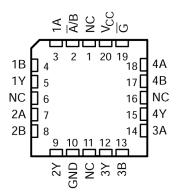


Figure 3-1. SN54AHCT157 J or W Package; SN74AHCT157 D, DB, DGV, N, NS, or PW Package (Top View)



NC - No internal connection

Figure 3-2. SN54AHCT157 FK Package (Top View)

Table 3-1. Pin Functions

	PIN	TYPE(1)	DESCRIPTION	
NAME	NO.	ITPE("/	DESCRIPTION	
Ā/B	1	I	Address select	
1A	2	I	Channel 1, data input A	
1B	3	I	Channel 1, data input B	
1Y	4	0	Channel 1, data output	
2A	5	I	Channel 2, data input A	
2B	6	I	Channel 2, data input B	
2Y	7	0	Channel 2, data output	
GND	8	G	Ground	
3Y	9	0	Channel 3, data output	
3B	10	I	Channel 3, data input B	
3A	11	I	Channel 3, data input A	
4Y	12	0	Channel 4, data output	
4B	13	I	Channel 4, data input B	
4A	14	I	Channel 4, data input A	
G	15	I	Output strobe, active low	
V _{CC}	16	Р	Positive supply	

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I ⁽²⁾	Input voltage range		-0.5	7	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)		-20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±25	mA
	Continuous current through V _{CC} or GI		±50	mA	
T _{stg}	Storage temperature range	-65	150	°C	

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AH0	CT157	SN74AHC	UNIT	
		MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage			4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δν	Input transition rise or fall time		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC(1)		D	DB	DGV	N	NS	PW	UNIT
				16 F	PINS			
R _{0JA} (2)	Junction-to-ambient thermal resistance	73	82	120	67	64	135.9	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	Т	A = 25°C		SN54AH	ICT157	SN74AH	CT157	UNIT
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V	I _{OH} = -50μA	4.5V	4.4	4.5		4.4		4.4		\/
V_{OH}	I _{OH} = -8mA	4.50	3.94			3.8		3.8		V

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT157		SN74AHCT157	UNIT
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN I	MAX	MIN MAX	UNII
V	I _{OL} = 50μA	4.5V			0.1		0.1	0.1	V
V _{OL}	I _{OL} = 8mA	4.5V			0.36		0.44	0.44	
II	V _I = 5.5V or GND	0V to 5.5V			±0.1	:	±1 ⁽¹⁾	±1	μА
I _{CC}	$V_I = V_{CC}$ or $I_O = 0$	5.5V			2		20	20	μА
ΔI _{CC} (2)	One input at 3.4V, Other inputs at V _{CC} or GND	5.5V			1.35		1.5	1.5	mA
C _i	V _I = V _{CC} or GND	5V		2	10			10	pF

- On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0V. This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0V or V_{CC} .

4.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V \pm 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

DADAMETED	FROM	то	LOAD	Т	A = 25 °C		SN54AHC	T157	SN74AHC	T157	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
t _{PLH}	A or B	Y	C _L = 15pF		4.1 ⁽¹⁾	6.4 ⁽¹⁾	1 ⁽¹⁾	7.5 ⁽¹⁾	1	7.5		
t _{PHL}	AOIB	Ĭ Ť	CL = 15PF		4.1 ⁽¹⁾	6.4 ⁽¹⁾	1 ⁽¹⁾	7.5 ⁽¹⁾	1	7.5	ns	
t _{PLH}	Ā/B	Y	C _L = 15pF		5.3 ⁽¹⁾	8.1 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	20	
t _{PHL}	AVB	T T	CL = 15pF		5.3 ⁽¹⁾	8.1 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	ns	
t _{PLH}	G	Y	C _L = 15pF		5.6 ⁽¹⁾	8.6 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns	
t _{PHL}	3	Ţ	CL = 15pr		5.6 ⁽¹⁾	8.6 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	115	
t _{PLH}	A or B	Y	C _L = 50pF		5.6	8.7	1	10.8	1	9.8	20	
t _{PHL}	AOIB	Ĭ Ť	CL = 50PF		5.6	8.7	1	10.8	1	9.8	ns	
t _{PLH}	Ā/B	Y	C = 50mF		6.8	10.4	1	13.2	1	12		
t _{PLH}	AVB	Ĭ Ť	C _L = 50pF		6.8	10.4	1	13.2	1	12	ns	
t _{PLH}	G	Y	C = 50pE		7.1	11	1	13.5	1	12	200	
t _{PHL}		ļ [†]	Y $C_L = 50pF$		7.1	11	1	13.5	1	12	ns	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.6 Noise Characteristics

 $V_{CC} = 5V, C_L = 50pF, T_A = 25^{\circ}C^{(1)}$

	PARAMETER	SN	UNIT		
	PARAWETER	MIN	TYP	MAX	UNII
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.4	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.4	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		1.8		V
V _{IH(D)}	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

4.7 Operating Characteristics

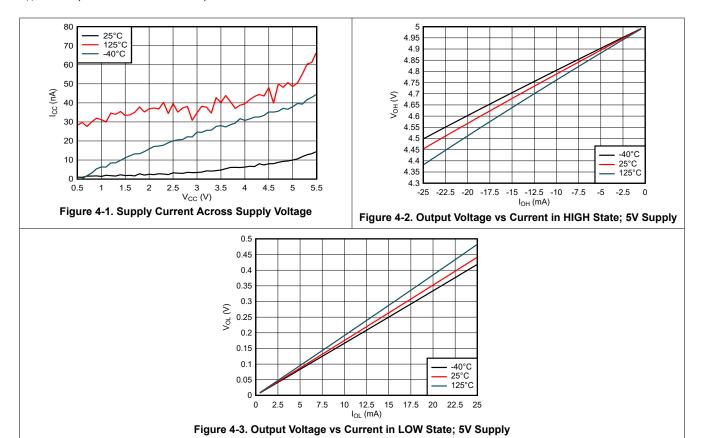
 $V_{CC} = 5V, T_{\Delta} = 25^{\circ}C$

- 60	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load, f = 1MHz	11	pF



4.8 Typical Characteristics

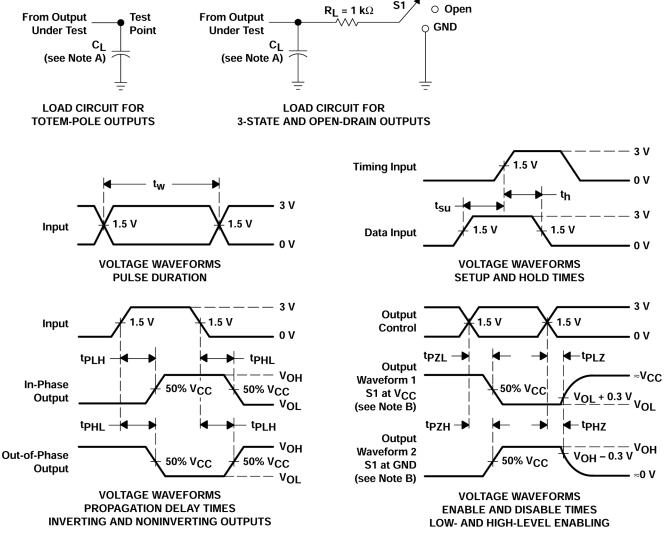
T_A = 25°C (unless otherwise noted)



o vcc



5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{CC}
t _{PHZ} /t _{PZH}	GND
Open Drain	V _{CC}



6 Detailed Description

6.1 Functional Block Diagram

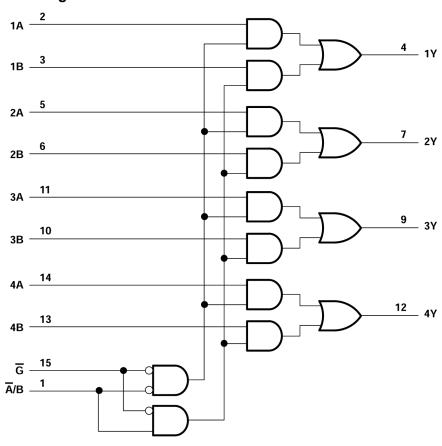


Figure 6-1. Logic Diagram (Positive Logic)

Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

6.2 Device Functional Modes

Table 6-1. Function Table

	INPUTS	OUTPUT Y				
G	A/B	Α	В	OUIFUL		
Н	Х	Х	Х	L		
L	L	L	Х	L		
L	L	Н	Х	Н		
L	Н	Х	L	L		
L	Н	Х	Н	Н		



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 4.2 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ f is recommended; if there are multiple V_{CC} pins, then 0.01 μ f or 0.022 μ f is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ f and a 1 μ f are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{\rm CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.1.1 Layout Example

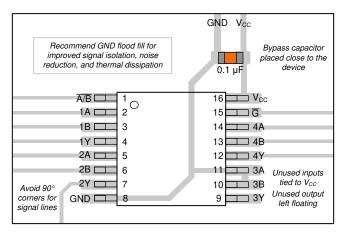


Figure 7-1. Example Layout for the SNx4AHCT157



8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN54AHCT157	Click here	Click here	Click here	Click here	Click here	
SN74AHCT157	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (July 2003) to Revision L (April 2024)

Page

- Added Device Information table, Pin Functions table, Thermal Information table, Device Functional
 Modes, Application and Implementation section, Device and Documentation Support section, and Mechanical,
 Packaging, and Orderable Information section



10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/			Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AHCT157D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	AHCT157
SN74AHCT157DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157
SN74AHCT157DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157
SN74AHCT157DGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157
SN74AHCT157DGVR.A	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157
SN74AHCT157DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT157
SN74AHCT157DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT157
SN74AHCT157N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT157N
SN74AHCT157N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT157N
SN74AHCT157PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	HB157
SN74AHCT157PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HB157
SN74AHCT157PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB157

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT157:

Automotive: SN74AHCT157-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT157DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT157DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74AHCT157DBR	SSOP	DB	16	2000	353.0	353.0	32.0
	SN74AHCT157DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
	SN74AHCT157DR	SOIC	D	16	2500	340.5	336.1	32.0
ı	SN74AHCT157PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHCT157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT157N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT157N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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