

# SNx4AHCT157 Automotive Quadruple 2-Line to 1-Line Data Selectors Multiplexers

## 1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17

## 2 Description

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5V to 5.5V  $V_{CC}$  operation.

The SNx4AHCT157 devices feature a common strobe ( $\overline{G}$ ) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

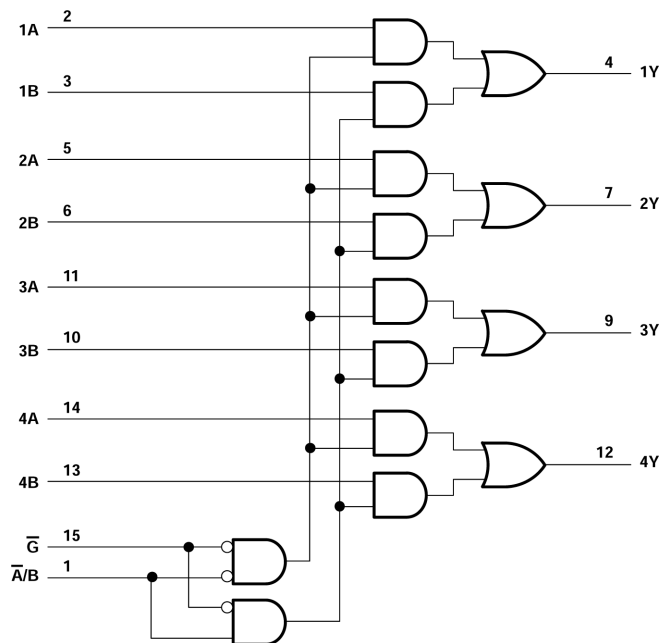
### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|-------------|------------------------|-----------------------------|--------------------------|
| SNx4AHCT157 | BQB (WQFN, 16)         | 3.5mm × 2.5mm               | 3.5mm × 2.5mm            |
|             | PW (TSSOP, 16)         | 5mm × 6.4mm                 | 5mm × 4.4mm              |

(1) For more information, see [Section 10](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



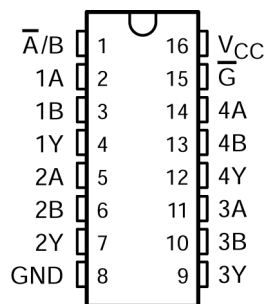
Logic Diagram (Positive Logic)



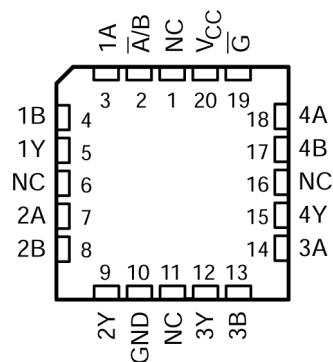
## Table of Contents

|                                                  |          |                                                                      |           |
|--------------------------------------------------|----------|----------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                          | <b>1</b> | 6.2 Device Functional Modes.....                                     | <b>8</b>  |
| <b>2 Description</b> .....                       | <b>1</b> | <b>7 Application and Implementation</b> .....                        | <b>9</b>  |
| <b>3 Pin Configuration and Functions</b> .....   | <b>3</b> | 7.1 Power Supply Recommendations.....                                | <b>9</b>  |
| <b>4 Specifications</b> .....                    | <b>4</b> | 7.2 Layout.....                                                      | <b>9</b>  |
| 4.1 Absolute Maximum Ratings.....                | <b>4</b> | <b>8 Device and Documentation Support</b> .....                      | <b>10</b> |
| 4.2 Recommended Operating Conditions.....        | <b>4</b> | 8.1 Documentation Support.....                                       | <b>10</b> |
| 4.3 Thermal Information.....                     | <b>4</b> | 8.2 Receiving Notification of Documentation Updates....              | <b>10</b> |
| 4.4 Electrical Characteristics.....              | <b>4</b> | 8.3 Support Resources.....                                           | <b>10</b> |
| 4.5 Switching Characteristics.....               | <b>5</b> | 8.4 Trademarks.....                                                  | <b>10</b> |
| 4.6 Noise Characteristics.....                   | <b>5</b> | 8.5 Electrostatic Discharge Caution.....                             | <b>10</b> |
| 4.7 Operating Characteristics.....               | <b>5</b> | 8.6 Glossary.....                                                    | <b>10</b> |
| 4.8 Typical Characteristics.....                 | <b>6</b> | <b>9 Revision History</b> .....                                      | <b>10</b> |
| <b>5 Parameter Measurement Information</b> ..... | <b>7</b> | <b>10 Mechanical, Packaging, and Orderable<br/>Information</b> ..... | <b>11</b> |
| <b>6 Detailed Description</b> .....              | <b>8</b> |                                                                      |           |
| 6.1 Functional Block Diagram.....                | <b>8</b> |                                                                      |           |

### 3 Pin Configuration and Functions



**Figure 3-1. SN54AHCT157 J or W Package;  
SN74AHCT157 D, DB, DGV, N, NS, or PW Package  
(Top View)**



NC – No internal connection  
**Figure 3-2. SN54AHCT157 FK Package (Top View)**

**Table 3-1. Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION               |
|-----------------|-----|---------------------|---------------------------|
| NAME            | NO. |                     |                           |
| A/B             | 1   | I                   | Address select            |
| 1A              | 2   | I                   | Channel 1, data input A   |
| 1B              | 3   | I                   | Channel 1, data input B   |
| 1Y              | 4   | O                   | Channel 1, data output    |
| 2A              | 5   | I                   | Channel 2, data input A   |
| 2B              | 6   | I                   | Channel 2, data input B   |
| 2Y              | 7   | O                   | Channel 2, data output    |
| GND             | 8   | G                   | Ground                    |
| 3Y              | 9   | O                   | Channel 3, data output    |
| 3B              | 10  | I                   | Channel 3, data input B   |
| 3A              | 11  | I                   | Channel 3, data input A   |
| 4Y              | 12  | O                   | Channel 4, data output    |
| 4B              | 13  | I                   | Channel 4, data input B   |
| 4A              | 14  | I                   | Channel 4, data input A   |
| G               | 15  | I                   | Output strobe, active low |
| V <sub>CC</sub> | 16  | P                   | Positive supply           |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                               |                                                   | MIN                                                       | MAX                   | UNIT   |
|-------------------------------|---------------------------------------------------|-----------------------------------------------------------|-----------------------|--------|
| V <sub>CC</sub>               | Supply voltage range                              | –0.5                                                      | 7                     | V      |
| V <sub>I</sub> <sup>(2)</sup> | Input voltage range                               | –0.5                                                      | 7                     | V      |
| V <sub>O</sub> <sup>(2)</sup> | Output voltage range                              | –0.5                                                      | V <sub>CC</sub> + 0.5 | V      |
| I <sub>IK</sub>               | Input clamp current                               | (V <sub>I</sub> < 0)                                      |                       | –20 mA |
| I <sub>OK</sub>               | Output clamp current                              | (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) |                       | ±20 mA |
| I <sub>O</sub>                | Continuous output current                         | (V <sub>O</sub> = 0 to V <sub>CC</sub> )                  |                       | ±25 mA |
|                               | Continuous current through V <sub>CC</sub> or GND |                                                           |                       | ±50 mA |
| T <sub>stg</sub>              | Storage temperature range                         | –65                                                       | 150                   | °C     |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | SN54AHCT157 |                 | SN74AHCT157 |                 | UNIT |
|-----------------|------------------------------------|-------------|-----------------|-------------|-----------------|------|
|                 |                                    | MIN         | MAX             | MIN         | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     |             |                 | 4.5         | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2           |                 | 2           |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |             | 0.8             |             | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      | 0           | 5.5             | 0           | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | 0           | V <sub>CC</sub> | 0           | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          |             | –8              |             | –8              | mA   |
| I <sub>OL</sub> | Low-level output current           |             | 8               |             | 8               | mA   |
| Δt/Δv           | Input transition rise or fall time |             | 20              |             | 20              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | –55         | 125             | –40         | 85              | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup>   |                                        | SN74AHCT157 |    |     |    |    |       | UNIT |
|---------------------------------|----------------------------------------|-------------|----|-----|----|----|-------|------|
|                                 |                                        | D           | DB | DGV | N  | NS | PW    |      |
|                                 |                                        | 16 PINS     |    |     |    |    |       |      |
| R <sub>θJA</sub> <sup>(2)</sup> | Junction-to-ambient thermal resistance | 73          | 82 | 120 | 67 | 64 | 135.9 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

### 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS         | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54AHCT157 |     | SN74AHCT157 |     | UNIT |
|-----------------|-------------------------|-----------------|-----------------------|-----|-----|-------------|-----|-------------|-----|------|
|                 |                         |                 | MIN                   | TYP | MAX | MIN         | MAX | MIN         | MAX |      |
| V <sub>OH</sub> | I <sub>OH</sub> = –50μA | 4.5V            | 4.4                   | 4.5 |     | 4.4         |     | 4.4         |     | V    |
|                 | I <sub>OH</sub> = –8mA  |                 | 3.94                  |     |     | 3.8         |     | 3.8         |     |      |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |      | SN54AHCT157 |                   | SN74AHCT157 |      | UNIT |
|---------------------------------|-------------------------------------------------------------|-----------------|-----------------------|-----|------|-------------|-------------------|-------------|------|------|
|                                 |                                                             |                 | MIN                   | TYP | MAX  | MIN         | MAX               | MIN         | MAX  |      |
| V <sub>OL</sub>                 | I <sub>OL</sub> = 50μA                                      | 4.5V            |                       |     | 0.1  |             | 0.1               |             | 0.1  | V    |
|                                 | I <sub>OL</sub> = 8mA                                       |                 |                       |     | 0.36 |             | 0.44              |             | 0.44 |      |
| I <sub>I</sub>                  | V <sub>I</sub> = 5.5V or GND                                | 0V to 5.5V      |                       |     | ±0.1 |             | ±1 <sup>(1)</sup> |             | ±1   | μA   |
| I <sub>CC</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5V            |                       |     | 2    |             | 20                |             | 20   | μA   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | One input at 3.4V, Other inputs at V <sub>CC</sub> or GND   | 5.5V            |                       |     | 1.35 |             | 1.5               |             | 1.5  | mA   |
| C <sub>i</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5V              |                       | 2   | 10   |             |                   |             | 10   | pF   |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

## 4.5 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5V ± 0.5V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER        | FROM (INPUT)     | TO (OUTPUT) | LOAD CAPACITANCE      | T <sub>A</sub> = 25 °C |                    |                    | SN54AHCT157      |                    | SN74AHCT157 |     | UNIT |
|------------------|------------------|-------------|-----------------------|------------------------|--------------------|--------------------|------------------|--------------------|-------------|-----|------|
|                  |                  |             |                       | MIN                    | TYP                | MAX                | MIN              | MAX                | MIN         | MAX |      |
| t <sub>PLH</sub> | A or B           | Y           | C <sub>L</sub> = 15pF |                        | 4.1 <sup>(1)</sup> | 6.4 <sup>(1)</sup> | 1 <sup>(1)</sup> | 7.5 <sup>(1)</sup> | 1           | 7.5 | ns   |
| t <sub>PHL</sub> |                  |             |                       |                        | 4.1 <sup>(1)</sup> | 6.4 <sup>(1)</sup> | 1 <sup>(1)</sup> | 7.5 <sup>(1)</sup> | 1           | 7.5 |      |
| t <sub>PLH</sub> | $\overline{A}/B$ | Y           | C <sub>L</sub> = 15pF |                        | 5.3 <sup>(1)</sup> | 8.1 <sup>(1)</sup> | 1 <sup>(1)</sup> | 9.5 <sup>(1)</sup> | 1           | 9.5 | ns   |
| t <sub>PHL</sub> |                  |             |                       |                        | 5.3 <sup>(1)</sup> | 8.1 <sup>(1)</sup> | 1 <sup>(1)</sup> | 9.5 <sup>(1)</sup> | 1           | 9.5 |      |
| t <sub>PLH</sub> | $\overline{G}$   | Y           | C <sub>L</sub> = 15pF |                        | 5.6 <sup>(1)</sup> | 8.6 <sup>(1)</sup> | 1 <sup>(1)</sup> | 10 <sup>(1)</sup>  | 1           | 10  | ns   |
| t <sub>PHL</sub> |                  |             |                       |                        | 5.6 <sup>(1)</sup> | 8.6 <sup>(1)</sup> | 1 <sup>(1)</sup> | 10 <sup>(1)</sup>  | 1           | 10  |      |
| t <sub>PLH</sub> | A or B           | Y           | C <sub>L</sub> = 50pF |                        | 5.6                | 8.7                | 1                | 10.8               | 1           | 9.8 | ns   |
| t <sub>PHL</sub> |                  |             |                       |                        | 5.6                | 8.7                | 1                | 10.8               | 1           | 9.8 |      |
| t <sub>PLH</sub> | $\overline{A}/B$ | Y           | C <sub>L</sub> = 50pF |                        | 6.8                | 10.4               | 1                | 13.2               | 1           | 12  | ns   |
| t <sub>PHL</sub> |                  |             |                       |                        | 6.8                | 10.4               | 1                | 13.2               | 1           | 12  |      |
| t <sub>PLH</sub> | $\overline{G}$   | Y           | C <sub>L</sub> = 50pF |                        | 7.1                | 11                 | 1                | 13.5               | 1           | 12  | ns   |
| t <sub>PHL</sub> |                  |             |                       |                        | 7.1                | 11                 | 1                | 13.5               | 1           | 12  |      |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 4.6 Noise Characteristics

V<sub>CC</sub> = 5V, C<sub>L</sub> = 50pF, T<sub>A</sub> = 25°C<sup>(1)</sup>

| PARAMETER          |                                               | SN74AHCT157 |      |      | UNIT |
|--------------------|-----------------------------------------------|-------------|------|------|------|
|                    |                                               | MIN         | TYP  | MAX  |      |
| V <sub>OL(P)</sub> | Quiet output, maximum dynamic V <sub>OL</sub> |             | 0.4  | 0.8  | V    |
| V <sub>OL(V)</sub> | Quiet output, minimum dynamic V <sub>OL</sub> |             | –0.4 | –0.8 | V    |
| V <sub>OH(V)</sub> | Quiet output, minimum dynamic V <sub>OH</sub> |             | 1.8  |      | V    |
| V <sub>IH(D)</sub> | High-level dynamic input voltage              | 2           |      |      | V    |
| V <sub>IL(D)</sub> | Low-level dynamic input voltage               |             |      | 0.8  | V    |

(1) Characteristics are for surface-mount packages only.

## 4.7 Operating Characteristics

V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

| PARAMETER       |                               | TEST CONDITIONS |          | TYP | UNIT |
|-----------------|-------------------------------|-----------------|----------|-----|------|
| C <sub>pd</sub> | Power dissipation capacitance | No load,        | f = 1MHz | 11  | pF   |

## 4.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

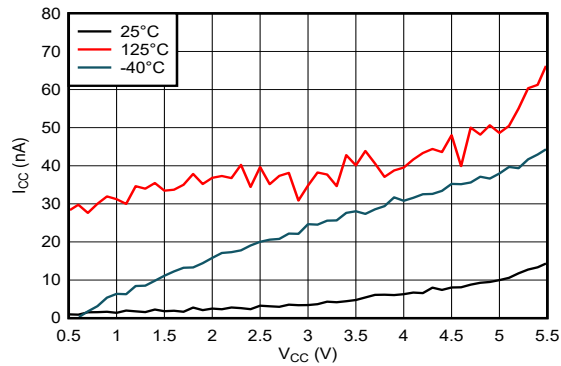


Figure 4-1. Supply Current Across Supply Voltage

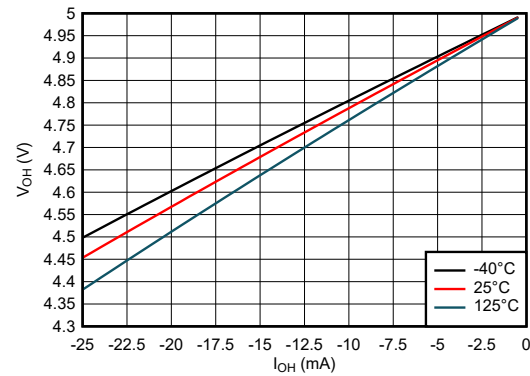


Figure 4-2. Output Voltage vs Current in HIGH State; 5V Supply

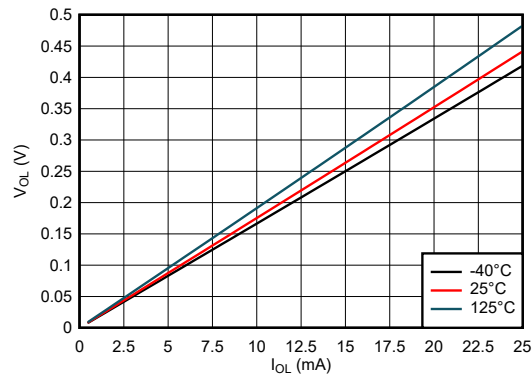
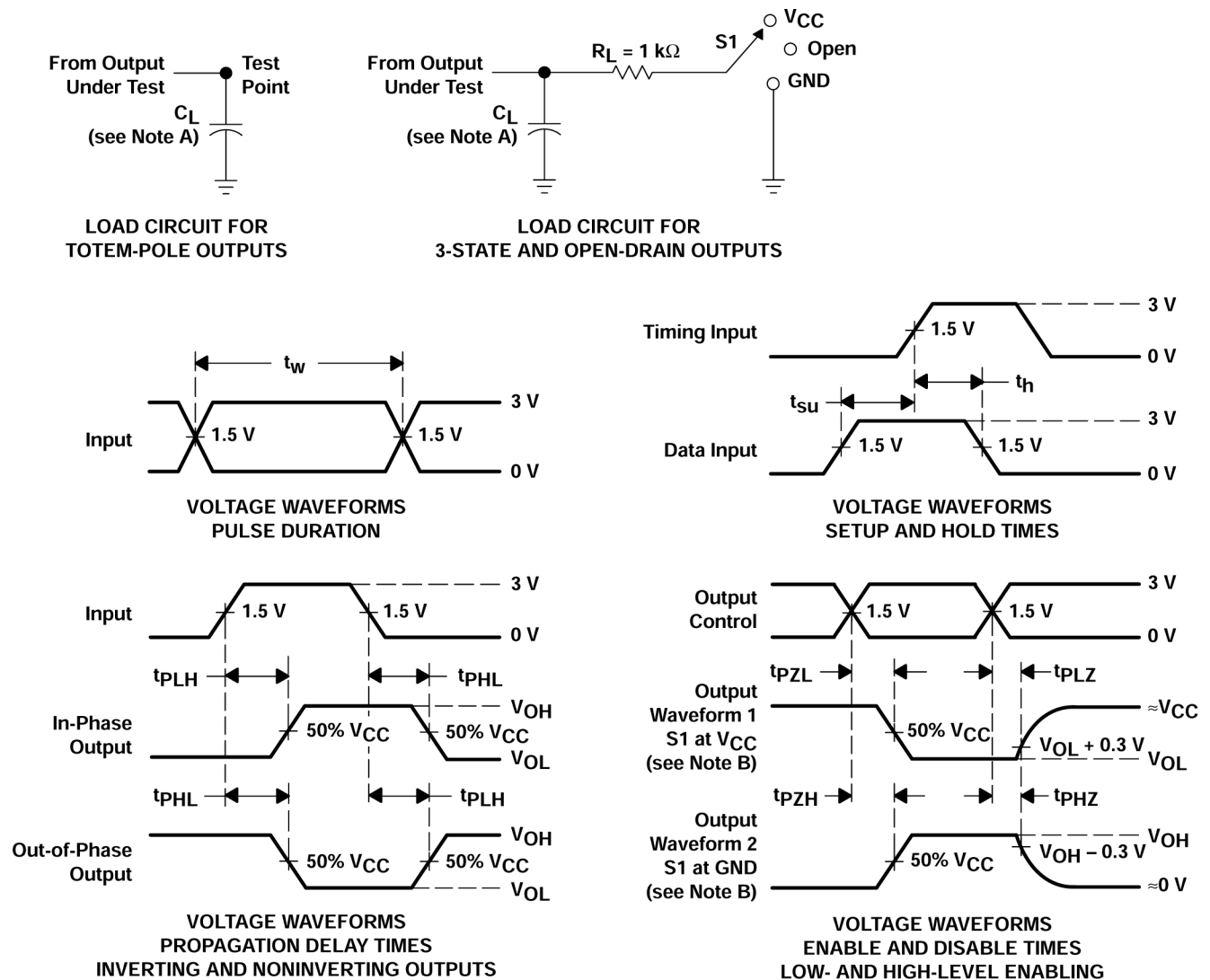


Figure 4-3. Output Voltage vs Current in LOW State; 5V Supply

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 5-1. Load Circuit and Voltage Waveforms**

| TEST              | S1       |
|-------------------|----------|
| $t_{PLH}/t_{PHL}$ | Open     |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND      |
| Open Drain        | $V_{CC}$ |

## 6 Detailed Description

### 6.1 Functional Block Diagram

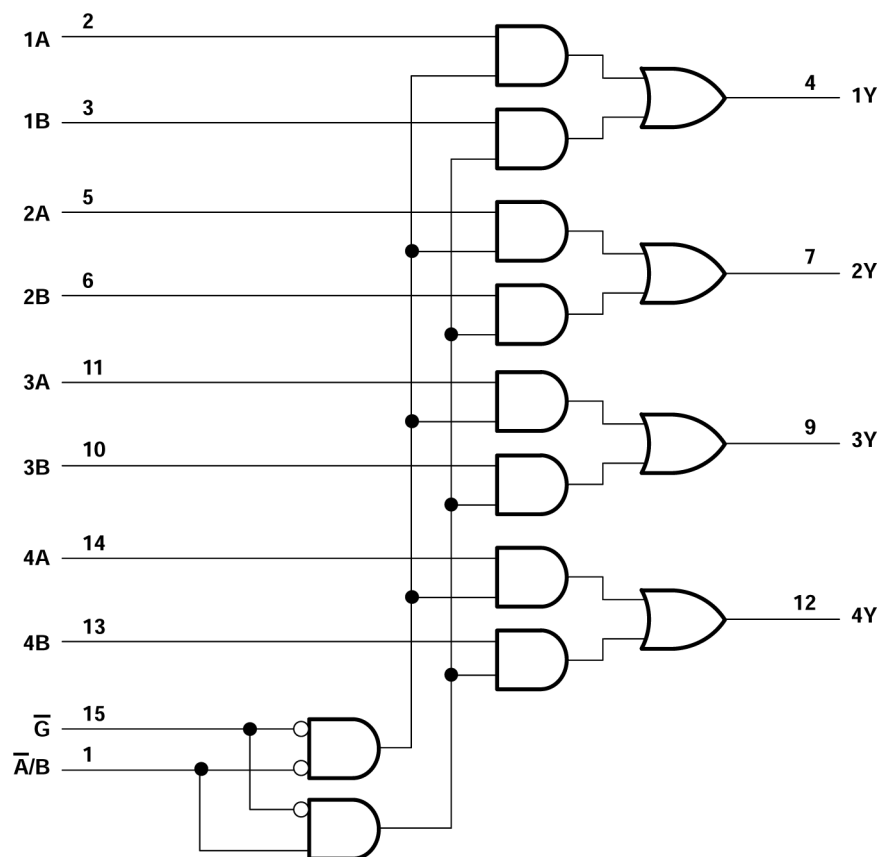


Figure 6-1. Logic Diagram (Positive Logic)

Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

### 6.2 Device Functional Modes

Table 6-1. Function Table

| INPUTS |     |   |   | OUTPUT Y |
|--------|-----|---|---|----------|
| G      | A/B | A | B |          |
| H      | X   | X | X | L        |
| L      | L   | L | X | L        |
| L      | L   | H | X | H        |
| L      | H   | X | L | L        |
| L      | H   | X | H | H        |



## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 4.2](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 $\mu$ F is recommended; if there are multiple  $V_{CC}$  pins, then 0.01 $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 $\mu$ F and a 1 $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

##### 7.2.1.1 Layout Example

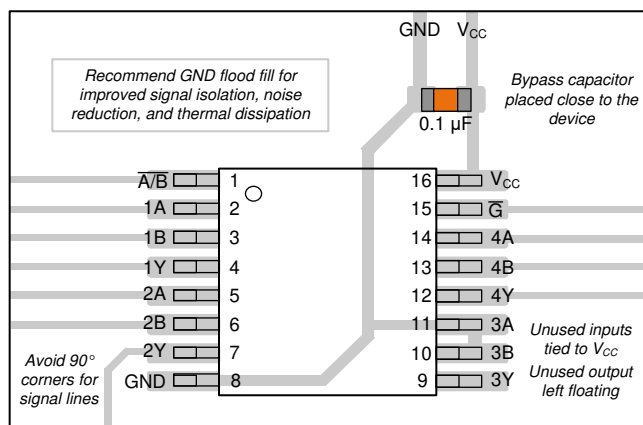


Figure 7-1. Example Layout for the SNx4AHCT157

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Documentation Support

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS       | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AHCT157 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74AHCT157 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision K (July 2003) to Revision L (April 2024)                                                                                                                                                                                                                                                    | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1    |
| • Updated thermal values for PW package from RθJA = 108 to 135.9, all values in °C/W .....                                                                                                                                                                                                                        | 4    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74AHCT157D</a>    | Obsolete      | Production           | SOIC (D)   16    | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | AHCT157             |
| <a href="#">SN74AHCT157DBR</a>  | Active        | Production           | SSOP (DB)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB157               |
| SN74AHCT157DBR.A                | Active        | Production           | SSOP (DB)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB157               |
| <a href="#">SN74AHCT157DGVR</a> | Active        | Production           | TVSOP (DGV)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB157               |
| SN74AHCT157DGVR.A               | Active        | Production           | TVSOP (DGV)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB157               |
| <a href="#">SN74AHCT157DR</a>   | Active        | Production           | SOIC (D)   16    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AHCT157             |
| SN74AHCT157DR.A                 | Active        | Production           | SOIC (D)   16    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AHCT157             |
| <a href="#">SN74AHCT157N</a>    | Active        | Production           | PDIP (N)   16    | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74AHCT157N        |
| SN74AHCT157N.A                  | Active        | Production           | PDIP (N)   16    | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74AHCT157N        |
| <a href="#">SN74AHCT157PW</a>   | Obsolete      | Production           | TSSOP (PW)   16  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HB157               |
| <a href="#">SN74AHCT157PWR</a>  | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | HB157               |
| SN74AHCT157PWR.A                | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HB157               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHCT157 :**

- Automotive : [SN74AHCT157-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

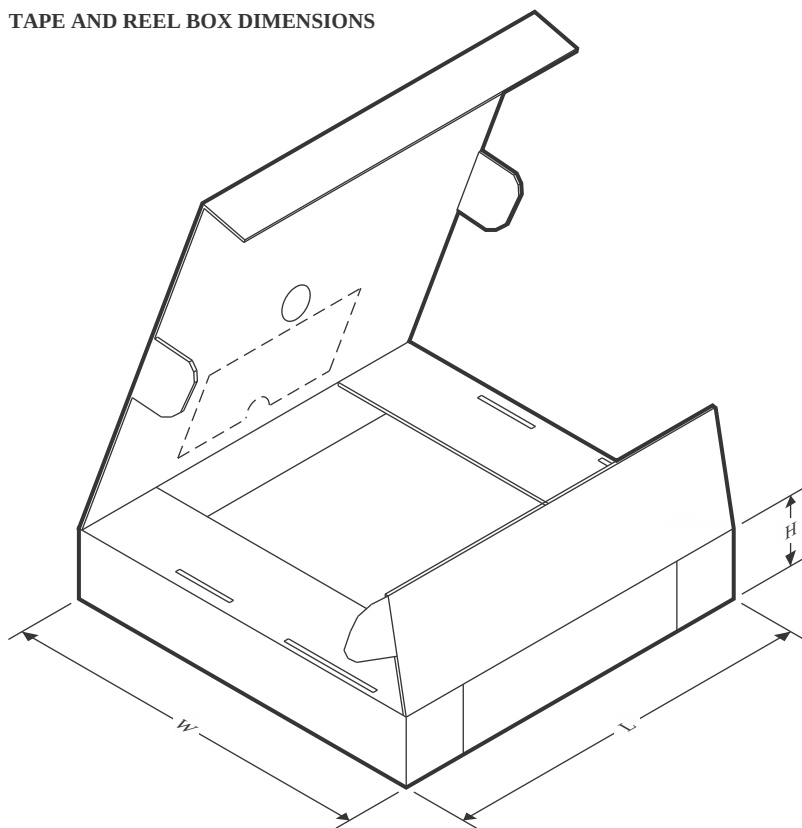
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

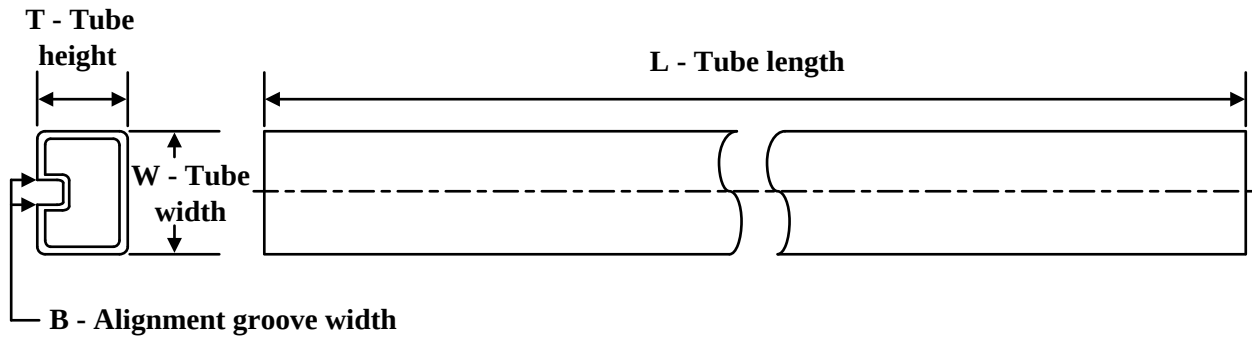
| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT157DBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74AHCT157DGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74AHCT157DR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74AHCT157PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT157DBR  | SSOP         | DB              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74AHCT157DGVR | TVSOP        | DGV             | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74AHCT157DR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74AHCT157PWR  | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


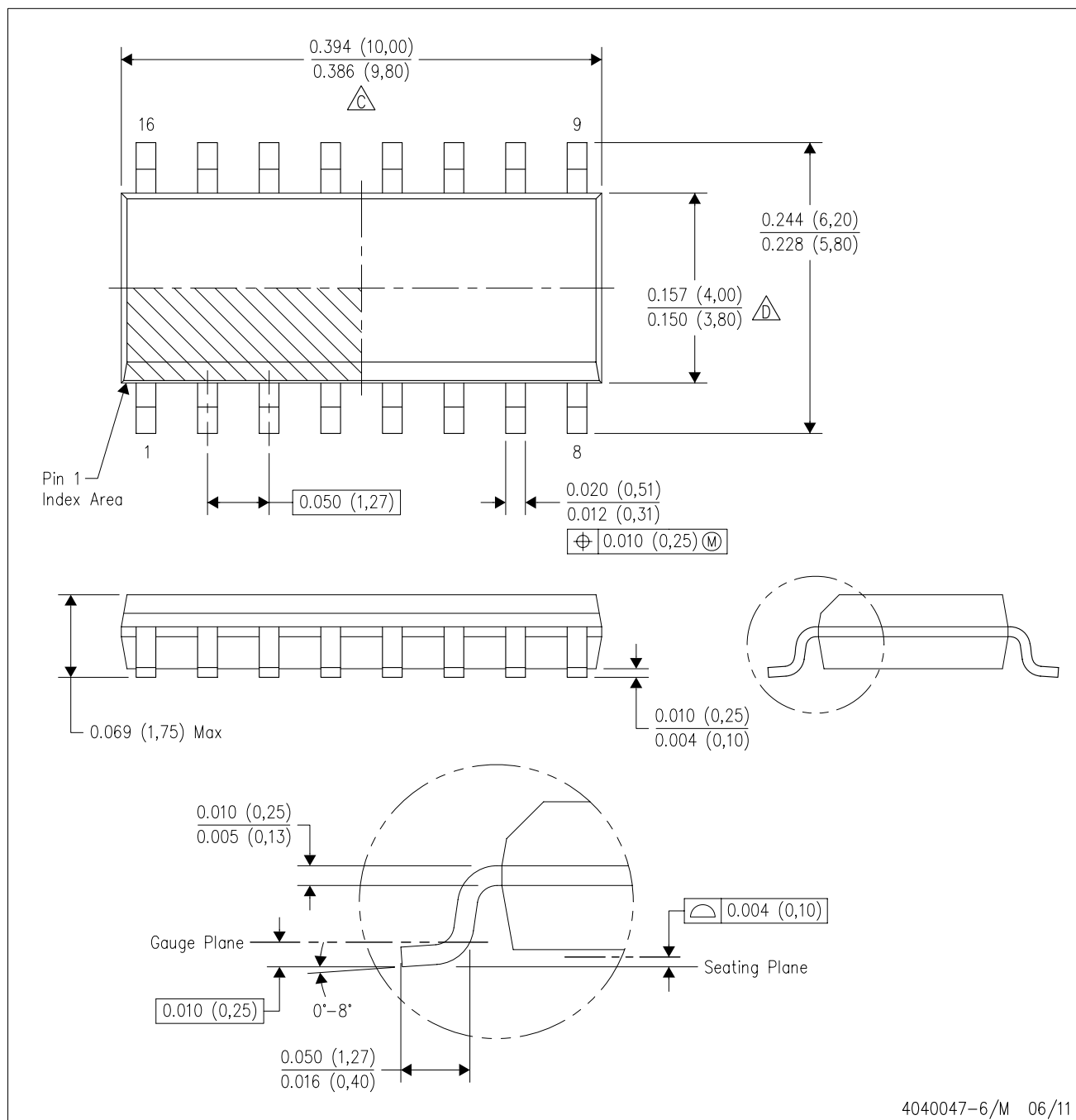
\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74AHCT157N   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AHCT157N   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AHCT157N.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AHCT157N.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

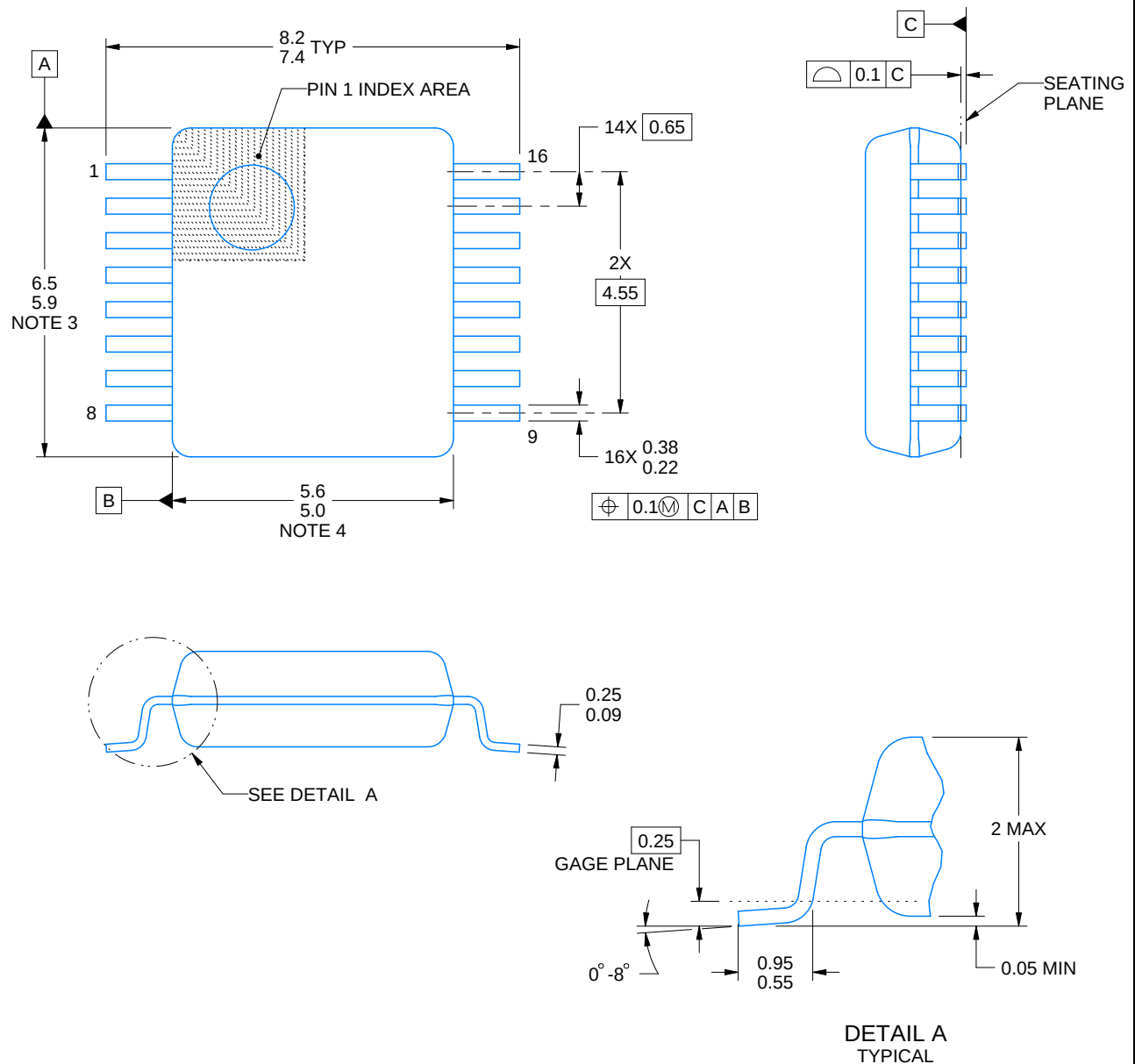


D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220763/A 05/2022

## NOTES:

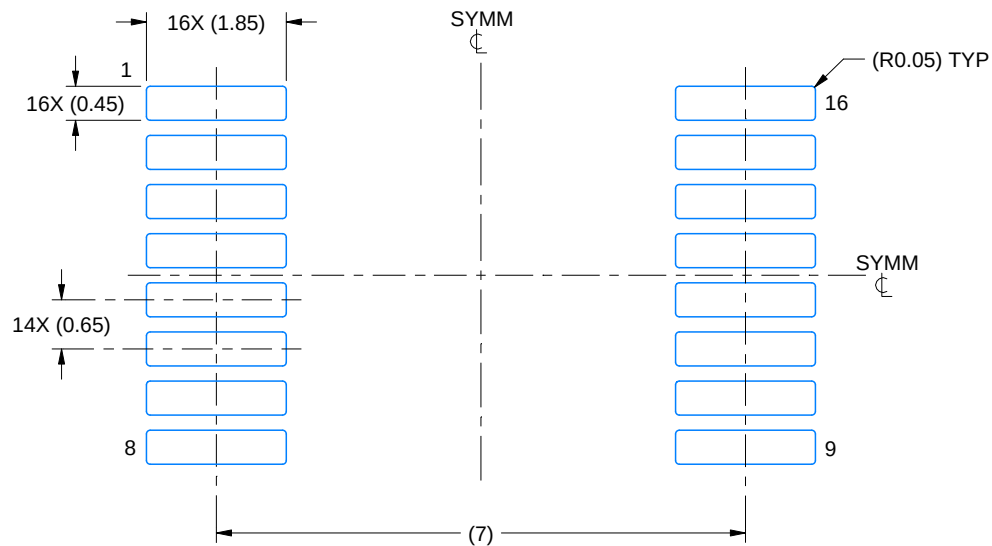
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

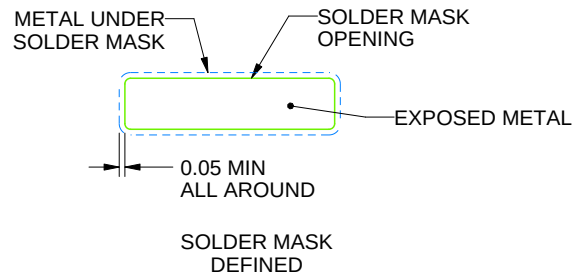
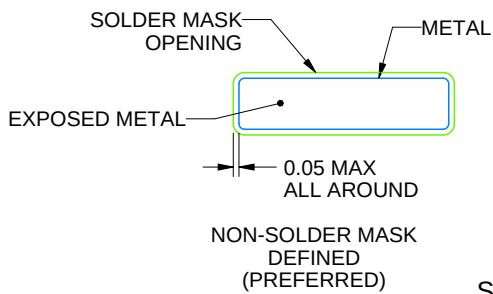
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

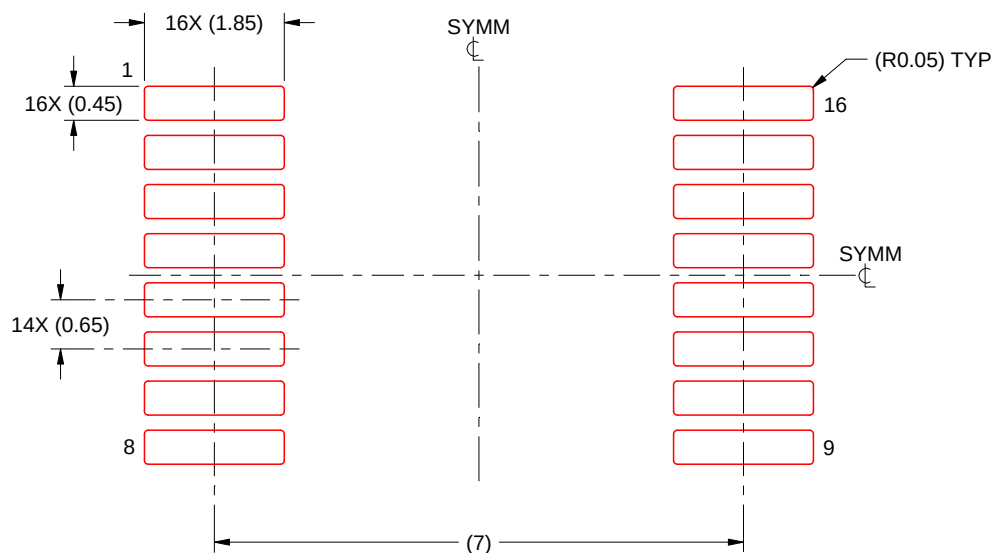
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

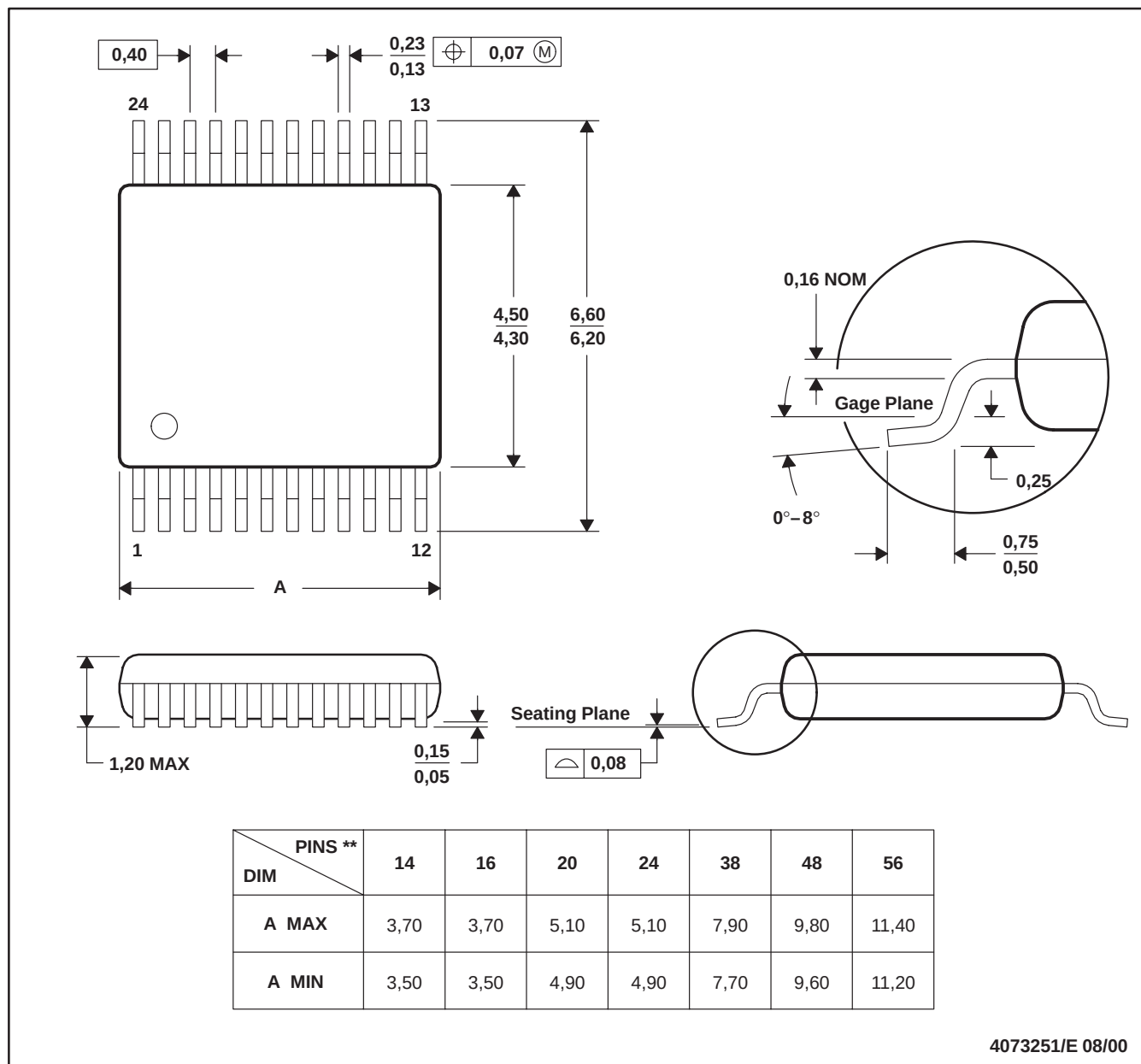
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

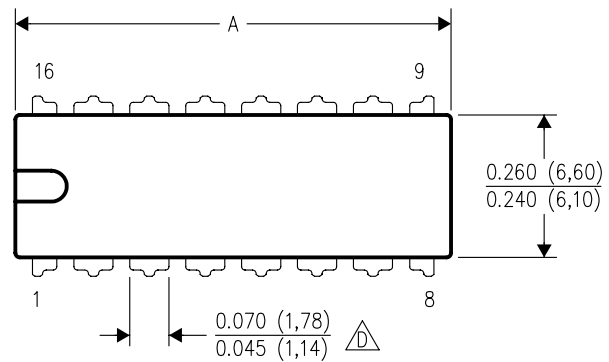


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

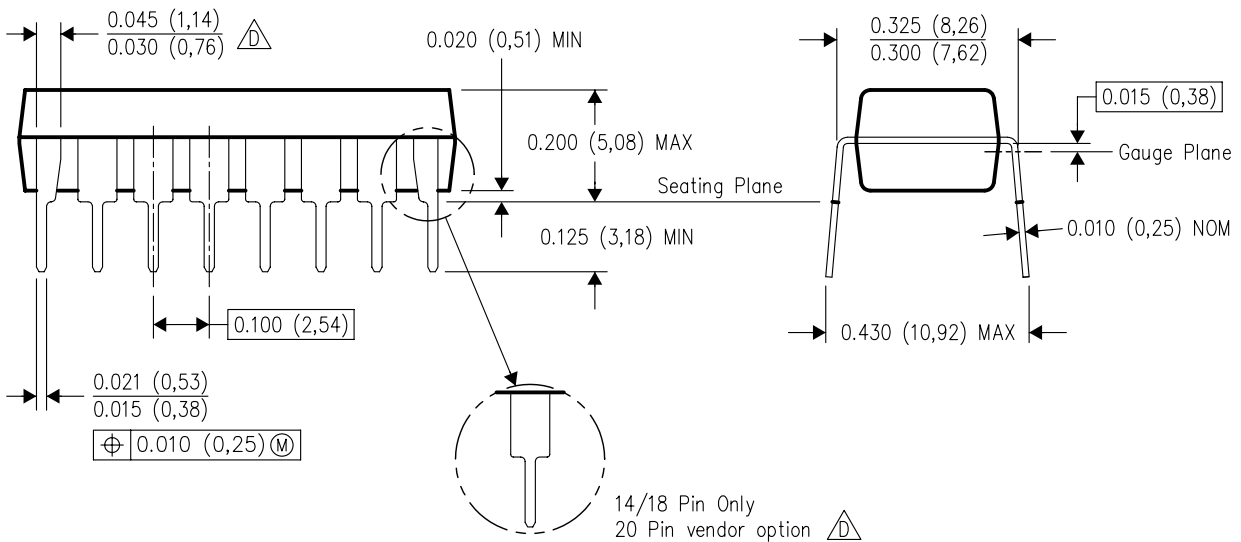
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



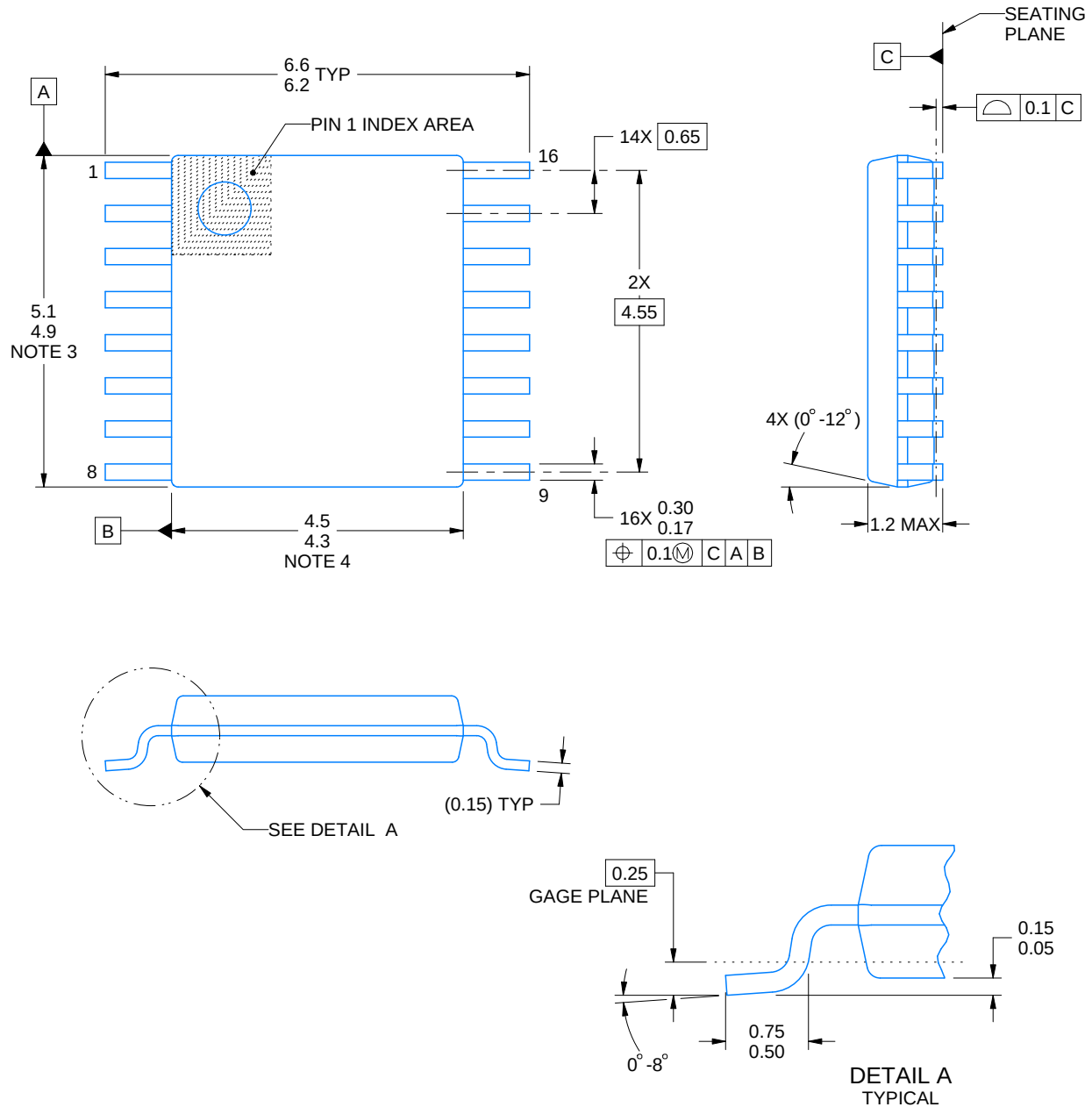
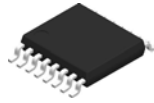
| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220204/B 12/2023

## NOTES:

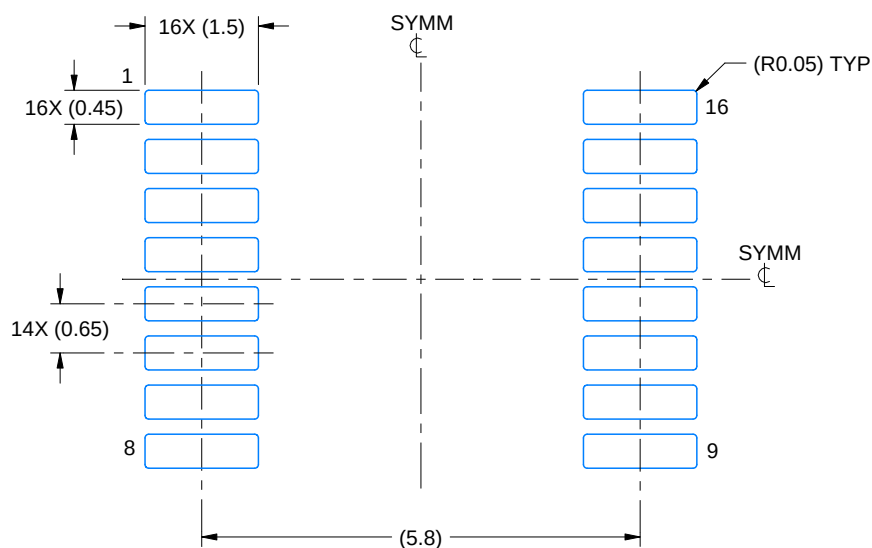
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

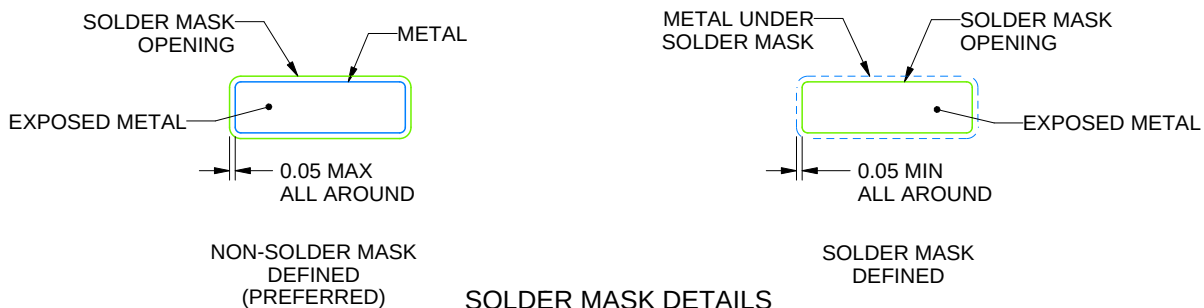
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

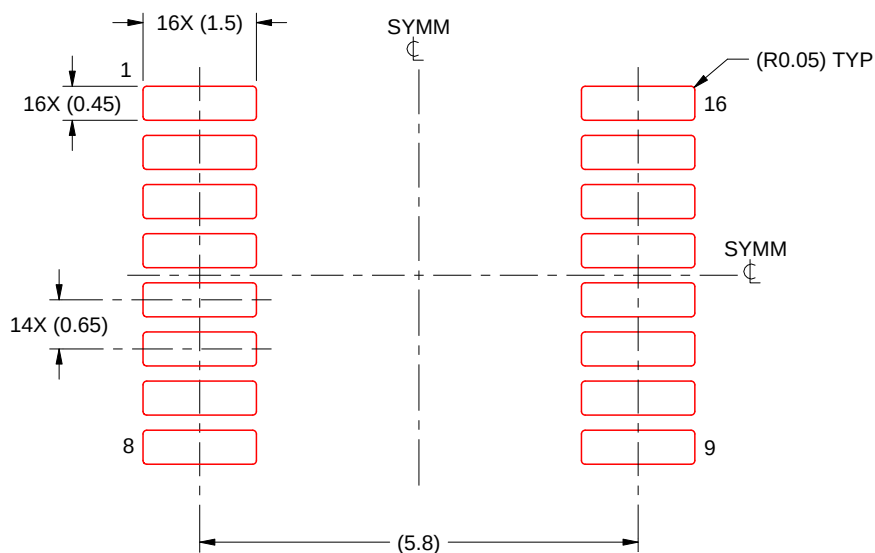


## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated