







**SN74AHC86, SN54AHC86** 

SCLS249L - OCTOBER 1995 - REVISED OCTOBER 2023

# **SNx4AHC86 Quadruple 2-Input Exclusive-OR Gates**

#### 1 Features

- Operating range 2-V to 5.5-V V<sub>CC</sub>
- Latch-up performance exceeds 250 mA per JESD 17
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)
  - 1000-V charged-device model (C101)

## 2 Applications

- Detect phase differences in input signals
- Create a selectable inverter or buffer

## 3 Description

The SNx4AHC86 devices are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A \overline{B}$  in positive logic.

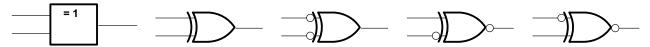
A common application is as a true or complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

#### **Device Information**

PART NUMBER	RATING	PACKAGE <sup>(1)</sup>
		BQA (WQFN, 14)
		D (SOIC, 14)
		DB (SSOP, 14)
SN74AHC86	Commercial	DGV (TVSOP, 14)
SIV/4AFIC60	Commercial	N (PDIP, 14)
		NS (SOP, 14)
		PW (TSSOP, 14)
		RGY (VQFN, 14)
		J (CDIP, 14)
SN54AHC86	Military	W (CFP, 14)
		FK (LCCC, 20)

For all available packages, see the orderable addendum at the end of the data sheet.

#### **EXCLUSIVE OR**



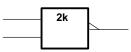
These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

#### LOGIC-IDENTITY ELEMENT



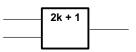
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

#### **EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

#### **ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

**Exclusive-OR Logic** 



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## **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (July 2023) to Revision L (October 2023)	Page
• Updated RθJA values: D = 86 to 124.5, PW = 113 to 147.7, all values in °C/W	
Added Application and Implementation section	9
Changes from Revision J (May 2013) to Revision K (July 2023)	Page
Changed the numbering format for tables, figures, and cross-references throughout to	the document
Added the Device Information table	
Added the Device and Documentation Support sections	13
Added the Mechanical, Packaging, and Orderable Information sections	13

Product Folder Links: SN74AHC86 SN54AHC86



## **5 Pin Configuration and Functions**

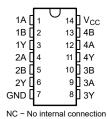


Figure 5-1. SN54AHC86 J or W Package, SN74AHC86 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)

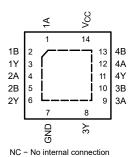


Figure 5-2. SN74AHC86 RGY Package, VQFN 14-Pin (Top View)

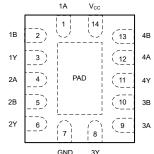


Figure 5-3. SN74AHC86 BQA Package, WQFN 14-Pin (Top View)

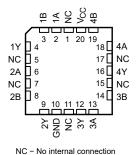


Figure 5-4. SN54AHC86 FK Package, LCCC 20-Pin (Top View)

Table 5-1. Pin Functions

	PIN			
NAME	D, DB, DGV, N, NS, PW, RGY, J, W, or BQA	FK	TYPE <sup>(1)</sup>	DESCRIPTION
1A	1	2	I	Channel 1, Input A
1B	2	3	I	Channel 1, Input B
1Y	3	4	0	Channel 1, Output Y
2A	4	6	I	Channel 2, Input A
2B	5	8	I	Channel 2, Input B
2Y	6	9	0	Channel 2, Output Y
GND	7	10	G	Ground
3Y	8	12	0	Channel 3, Output Y
3A	9	13	I	Channel 3, Input A
3B	10	14	I	Channel 3, Input B
4Y	11	16	0	Channel 4, Output Y
4A	12	18	1	Channel 4, Input A
4B	13	19	1	Channel 4, Input B
V <sub>CC</sub>	14	20	Р	Positive Supply
NC	_	1, 5, 7, 11, 15, 17	_	Not internally connected
Thermal pad <sup>(2)</sup>			_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

<sup>(1)</sup> Signal Types: I = Input, O = Output, I/O = Input or Output, G = ground, P = power.

<sup>(2)</sup> BQA package only



## **6 Specifications**

## **6.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, V <sub>CC</sub>	–0.5 to 7	V
Input voltage range, V <sub>I</sub> <sup>(2)</sup>	–0.5 to 7	V
Output voltage range, V <sub>O</sub> <sup>(2)</sup>	–0.5 to V <sub>CC</sub> + 0.5	V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20	mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20	mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25	mA
Continuous current through V <sub>CC</sub> or GND	±50	mA
Storage temperature range, T <sub>stg</sub>	-65 to 150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## **6.2 Recommended Operating Conditions**

			SN54AH	C86	SN74AH	C86	LINUT	
			MIN	MAX	MIN	UNIT		
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V	
		V <sub>CC</sub> = 2 V	1.5		1.5			
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3V	2.1		2.1		V	
		V <sub>CC</sub> = 5.5 V	3.85		3.85			
		V <sub>CC</sub> = 2 V		0.5		0.5		
V <sub>IL</sub>	Low-level Input voltage	V <sub>CC</sub> = 3 V		0.9		0.9	V	
		V <sub>CC</sub> = 5.5 V		1.65		1.65		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V	
Vo	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
		V <sub>CC</sub> = 2 V		-50		-50		
I <sub>OH</sub>	High-level output current	$V_{CC}$ = 3.3 V ± 0.3 V		-4		-4	mA	
		V <sub>CC</sub> = 5 V ± 0.5 V		-8		-8		
		V <sub>CC</sub> = 2 V		50		50		
l <sub>OL</sub>	Low-level output current	$V_{CC}$ = 3.3 V ± 0.3 V		4		4	mA	
		$V_{CC} = 5 V \pm 0.5 V$		8		8		
A4/A	loured Transition size on fall and	V <sub>CC</sub> = 3.3 V ± 0.3 V		100		100	0.1	
Δt/Δv	Input Transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20		20	ns/V	
T <sub>A</sub>	Operating free-air temperature	1	-55	125	-40	125	°C	

Product Folder Links: SN74AHC86 SN54AHC86

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



#### 6.3 Thermal Information

			DB <sup>(2)</sup>	DGV <sup>(2)</sup>	N <sup>(2)</sup>	NS <sup>(2)</sup>	PW <sup>(2)</sup>	RGY <sup>(3)</sup>	BQA	
THERMAL METRIC <sup>(1)</sup>		SOIC	SSOP	TVSOP	PDIP	SOP	TSSOP	VQFN	WQFN	UNIT
		14	14	14	14	14	14	14	14	
R <sub>θJA</sub>	Junction-to- ambient thermal resistance	124.5	96	127	80	76	147.7	47	88.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5

#### 6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

			T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C Recommended		UNIT
PARAMETER	TEST CONDITIONS	V <sub>cc</sub>										
						SN54AH	IC86	SN74AH	C86	SN74AH	C86	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
		2 V	1.9	2		1.9		1.9		1.9		
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		3.8		
	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		0.1		0.1	
		3 V			0.1		0.1		0.1		0.1	
V <sub>OL</sub>		4.5 V			0.1		0.1		0.1		0.1	V
	I <sub>OH</sub> = 4 mA	3 V			0.36		0.5		0.44		0.5	
	I <sub>OH</sub> = 8 mA	4.5 V			0.36		0.5		0.44		0.5	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(1)</sup>		±1		±1	μA
Icc	$V_1 = V_{CC} \text{ or } $ $I_0 = 0$	5.5 V			2		20		20		20	μΑ
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10				10			pF

<sup>(1)</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

## 6.5 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 7-1)

	FROM	то	LOAD	T <sub>A</sub> = 2	5°C	T <sub>A</sub> = -59		T <sub>A</sub> = -40		T <sub>A</sub> = -4	°C	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	,		SN54AHC86		SN74AHC86		Recommended SN74AHC86		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	V	C <sub>L</sub> = 15 pF	7 <sup>(1)</sup>	11 <sup>(1)</sup>	1 <sup>(1)</sup>	13 <sup>(1)</sup>	1	13	1	13	no
t <sub>PHL</sub>	AOIB	ľ	C <sub>L</sub> = 15 pr	7 <sup>(1)</sup>	11 <sup>(1)</sup>	1 <sup>(1)</sup>	13 <sup>(1)</sup>	1	13	1	13	ns
t <sub>PLH</sub>	A or B		C <sub>L</sub> = 50 pF	9.5	14.5	1	16.5	1	16.5	1	16.5	ns
t <sub>PHL</sub>			OL - 30 pi	9.5	14.5	1	16.5	1	16.5	1	16.5	113

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.



## **6.6 Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

						T <sub>A</sub> = -59		T <sub>A</sub> = -40		T <sub>A</sub> = -40 125		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		SN54AHC86		SN74AHC86		Recommended SN74AHC86		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	V	C = 15 = 5	4.8(1)	6.8 <sup>(1)</sup>	1 <sup>(1)</sup>	8(1)	1	8	1	8	
t <sub>PHL</sub>	AOIB	Ť	C <sub>L</sub> = 15 pF	4.8(1)	6.8 <mark>(1)</mark>	1 <sup>(1)</sup>	8(1)	1	8	1	8	ns
t <sub>PLH</sub>	A or B	V	C <sub>L</sub> = 50 pF	6.3	8.8	1	10	1	10	1	10	ns
t <sub>PHL</sub>		ı	OL - 30 pi	6.3	8.8	1	10	1	10	1	10	113

## **6.7 Noise Characteristics**

 $V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}^{(1)}$ 

	DADAMETED	SN	SN74AHC86			
	PARAMETER	MIN	TYP	MAX		
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.3	0.8	V	
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.3	-0.8	V	
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>	4.4			V	
V <sub>IH(D)</sub>	High-level dynamic input voltage	3.5			V	
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1.5	V	

<sup>(1)</sup> Characteristics are for surface-mount packages only.

## **6.8 Operating Characteristics**

 $V_{CC}$  = 5 V,  $T_A$  = 25°C

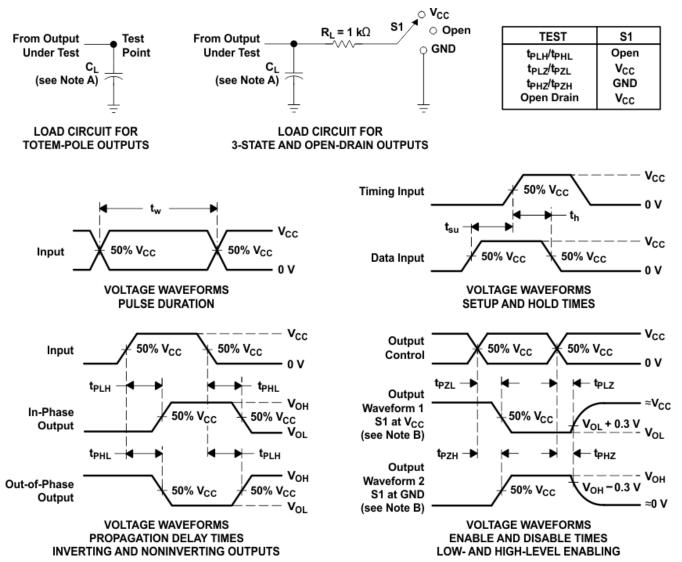
	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load, f = 1 MHz	18	pF

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### 7 Parameter Measurement Information



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

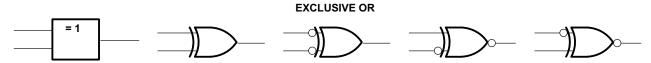
Figure 7-1. Load Circuit and Voltage Waveforms



## **8 Detailed Description**

## 8.1 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

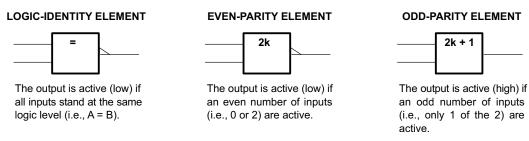


Figure 8-1. Exclusive-OR Logic

#### 8.2 Device Functional Modes

Table 8-1. Function Table (Each Gate)

INP	OUTPUT	
A	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

Product Folder Links: SN74AHC86 SN54AHC86



## 9 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Figure 9-1. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74LV4T08-Q1 is used to directly control the RESET pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

## 9.2 Typical Application

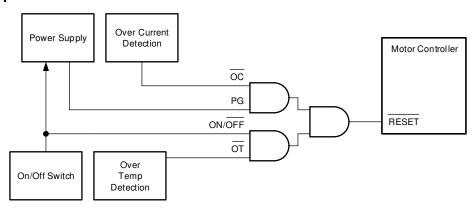


Figure 9-1. Typical Application Block Diagram

#### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I<sub>CC</sub>, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4AHC86 plus the maximum supply current, I<sub>CC</sub>, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SNx4AHC86 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SNx4AHC86 can drive a load with total resistance described by  $R_L \ge V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OL}$ . When outputting in the HIGH state, the output



voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption* and *Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.1.1 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4AHC86 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

Refer to the Feature Description section for additional information regarding the inputs for this device.

### 9.2.1.2 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V<sub>OI</sub> specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V<sub>CC</sub> or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

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#### 9.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V<sub>CC</sub> to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V<sub>CC</sub> and GND pins. An example layout is shown in the *Layout* section.
- 2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC1G04-Q1 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ , so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.3 Application Curves

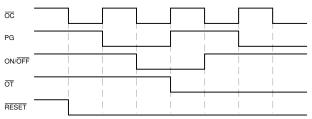


Figure 9-2. Application Timing Diagram

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 9.4 Layout

## 9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



## 9.4.1.1 Layout Example

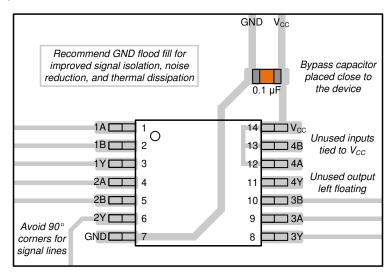


Figure 9-3. Example Layout for the SNx4AHC86

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 10.1 Documentation Support (Analog)

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 10.4 Trademarks

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All trademarks are the property of their respective owners.

#### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9681601Q2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681601Q2A SNJ54AHC 86FK
5962-9681601QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681601QC A SNJ54AHC86J
5962-9681601QDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681601QD A SNJ54AHC86W
SN74AHC86BQAR	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86BQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 125	AHC86
SN74AHC86DBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86
SN74AHC86DBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86
SN74AHC86DGVR	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86
SN74AHC86DGVR.A	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86
SN74AHC86DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86DRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC86N
SN74AHC86N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC86N
SN74AHC86NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC86
SN74AHC86PW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 125	HA86
SN74AHC86PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86
SN74AHC86PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA86
SN74AHC86RGYR	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA86



-55 to 125

-55 to 125

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SNJ54AHC86J

5962-9681601QD A SNJ54AHC86W

5962-9681601QD A SNJ54AHC86W



SNJ54AHC86W

SNJ54AHC86W.A

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Orderable part number	Status	Material type (2)	Package   Pins	Package qty   Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AHC86RGYR.A	Active	Production	VQFN (RGY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA86
SNJ54AHC86FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681601Q2A SNJ54AHC 86FK
SNJ54AHC86FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9681601Q2A SNJ54AHC 86FK
SNJ54AHC86J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681601Q0 A SNJ54AHC86J
SNJ54AHC86J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681601Q

Active

Active

Production

Production

CFP (W) | 14

CFP (W) | 14

No

No

**SNPB** 

**SNPB** 

N/A for Pkg Type

N/A for Pkg Type

25 | TUBE

25 | TUBE

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

## **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54AHC86, SN74AHC86:

Catalog: SN74AHC86

Military: SN54AHC86

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

**PACKAGE MATERIALS INFORMATION** 

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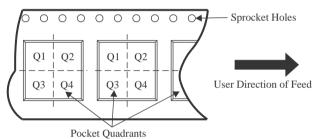
## **TAPE AND REEL INFORMATION**





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC86DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC86DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC86DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC86NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC86RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC86DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC86DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC86DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC86DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC86NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC86PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC86RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9681601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9681601QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC86FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC86FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC86W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHC86W.A	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



## DGV (R-PDSO-G\*\*)

## 24 PINS SHOWN

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
   The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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