







SN74AHC132

SCLS365K - MAY 1996 - REVISED FEBRUARY 2024

SN74AHC132 Quadruple Positive-NAND Gates with Schmitt-Trigger Inputs

1 Features

- Operating range 2V to 5.5V V_{CC}
- Operation from very slow input transitions
- Temperature-compensated threshold levels
- High noise immunity
- Same pinouts as SNx4AHC00
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000V human-body model
 - 1000V charged-device model

2 Applications

- Electronic points of sale
- Telecom infrastructure
- **Network switches**
- Tests and measurements

3 Description

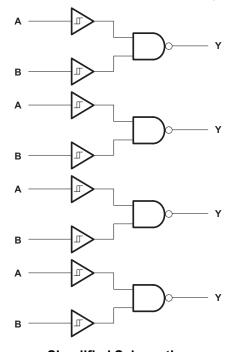
The SN7AHC132 device is a quadruple positive-NAND gate designed for 2V to 5.5V V_{CC} operation. This device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Schmitt-trigger inputs provide added noise immunity and support for slow input signal transitions.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)								
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm								
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm								
	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm								
SN7AHC132	DGV (TVSOP, 14)	3.6mm × 6.4mm	3.6mm × 4.4mm								
SN/AHC132	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm								
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.5mm × 3.5mm								
	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35mm								
	NS (SOP, 14)	10.2mm × 7.8mm	5.3mm × 10.3mm								

- For more information, see Section 11.
- The package size (length × width) is a nominal value and includes pins, where applicable
- The body size (length × width) is a nominal value and does not include pins.



Simplified Schematics



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4 Pin Configuration and Functions

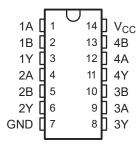


Figure 4-1. SN74AHC132 D, DB, DGV, N, NS, or PW Package, 14-Pin (Top View)

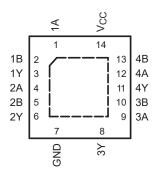


Figure 4-2. SN74AHC132 RGY Package, 14-Pin VQFN (Top View)

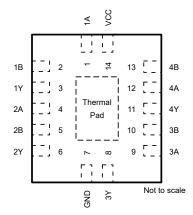


Figure 4-3. SN74AHC132 BQA Package, 14-Pin WQFN (Top View)

			_	4.
Table	4-1.	Pin	Fun	ctions

Р	IN	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	ITPE("	DESCRIPTION
1A	1	I	1A Input
1B	2	I	1B Input
1Y	3	0	1Y Output
2A	4	I	2A Input
2B	5	I	2B Input
2Y	6	0	2Y Output
3Y	8	0	3Y Output
3A	9	I	3A Input
3B	10	I	3B Input
4Y	11	0	4Y Output
4A	12	I	4A Input
4B	13	I	4B Input
GND	7	_	Ground Pin
V _{CC}	14	_	Power Pin
Thermal Pa	d ⁽²⁾	_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

- (1) I = input, O = output
- (2) For BQA only.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_{O} = 0$ to V_{CC}		±25	mA
	Continuous current through V _{CC} or GND	·		±50	mA

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature rang	ge	-65	150	°C
V		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
V _(ESD) Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	V	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74AHC	132	UNIT			
			MIN	MIN MAX				
V _{CC}	Supply voltage		2	5.5	V			
VI	Input voltage		0	5.5	V			
Vo	Output voltage		0	V _{CC}	V			
I _{OH} I		V _{CC} = 2 V		-50	μA			
	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	m A			
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA			
		V _{CC} = 2 V		50	μA			
I_{OL}	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA			
		V _{CC} = 5 V ± 0.5 V		8	IIIA			
T _A	Operating free-air temperature		-40	125	°C			

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Product Folder Links: SN74AHC132

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



5.4 Thermal Information

					SN74A	HC132				
	THERMAL METRIC ⁽¹⁾		D	DB	DR	N	NS	PW	RGY	UNIT
		14 PINS								
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.3	124.6	107.1	90.6	57.4	90.7	147.7	57.5	
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.9	79.7	59.6	50.9	44.9	48.3	77.4	57.5	
R _{θJB}	Junction-to-board thermal resistance	56.8	81.2	54.4	44.8	37.2	49.4	90.9	33.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	9.9	39.3	20.5	14.7	30.1	14.6	27.2	3.4	C/VV
ΨЈВ	Junction-to-board characterization parameter	56.7	80.8	53.8	44.5	37.1	49.1	90.2	33.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	33.4	N/A	N/A	N/A	N/A	N/A	N/A	13.9	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	TA	= 25°C		SN74AH0	C132	-40°C to 12 SN74AHC	UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{T+}		3 V	1.2		2.2	1.2	2.2	1.2	2.2	
Positive-going		4.5 V	1.75		3.15	1.75	3.15	1.75	3.15	V
input threshold voltage		5.5 V	2.15		3.85	2.15	3.85	2.15	3.85	
V _T _		3 V	0.9		1.9	0.9	1.9	0.9	1.9	
Negative-going		4.5 V	1.35		2.75	1.35	2.75	1.35	2.75	V
input threshold voltage		5.5 V	1.65		3.35	1.65	3.35	1.65	3.35	
ΔV_{T}		3 V	0.3		1.2	0.3	1.2	0.3	1.2	
Hysteresis		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	V
$(V_{T^+} - V_{T^-})$		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
		2 V	1.9	2		1.9		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
		2 V			0.1		0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
V_{OL}		4.5 V			0.1		0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.44		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μΑ
Icc	V _I = V _{CC} or GND I _O = 0	5.5 V			2		20		20	μΑ
C _i	V _I = V _{CC} or GND	5 V		1.9	10		10		10	pF



5.6 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see (1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE		T _A = 25°C		SN74AH0	132	T _A = -40°C to SN74AH0		UNIT
(INPOT) (OUTPOT) CA	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t _{PLH}	A or B		C _L = 15 pF		5.6 ⁽¹⁾	11.9 ⁽¹⁾	1	14	1	15	ns
t _{PHL}	AOID	'			5.6 ⁽¹⁾	11.9 ⁽¹⁾	1	14	1	15	
t _{PLH}	A or B	A or B Y	C _L = 50 pF		7.6	15.4	1	17.5	1	19	ns
t _{PHL}	A or B				7.6	15.4	1	17.5	1	19	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see (1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	Т	_A = 25°C		SN74AHC	132		C to 125°C AHC132	UNIT	
	(IIVI O1)	(001101)	OAI AOIIANOL	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH}	A or B	A == D	V	C _I = 15 pF		3.9 ⁽¹⁾	7.7 ⁽¹⁾	1	9	1	10	ns
t _{PHL}		Ť	CL = 15 pr		3.9(1)	7.7 ⁽¹⁾	1	9	1	10		
t _{PLH}	A or B	V	C _I = 50 pF		5.3	9.7	1	11	1	12	ns	
t _{PHL}		AUB	1	OL = 30 pr		5.3	9.7	1	11	1	12	115

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.8 Noise Characteristics

 $V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}^{(1)}$

	PARAMETER	SN74AHC132					
	PARAINETER	MIN	TYP	MAX	UNIT		
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.45	0.8	V		
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.35	-0.8	V		
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.8		V		
V _{IH(D)}	High-level dynamic input voltage	3.5			V		
V _{IL(D)}	Low-level dynamic input voltage			1.5	V		

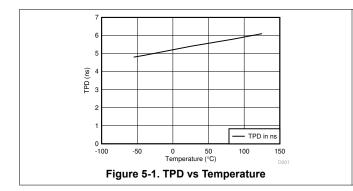
(1) Characteristics are for surface-mount packages only.

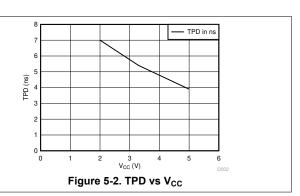
5.9 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST	CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11	pF

5.10 Typical Characteristics



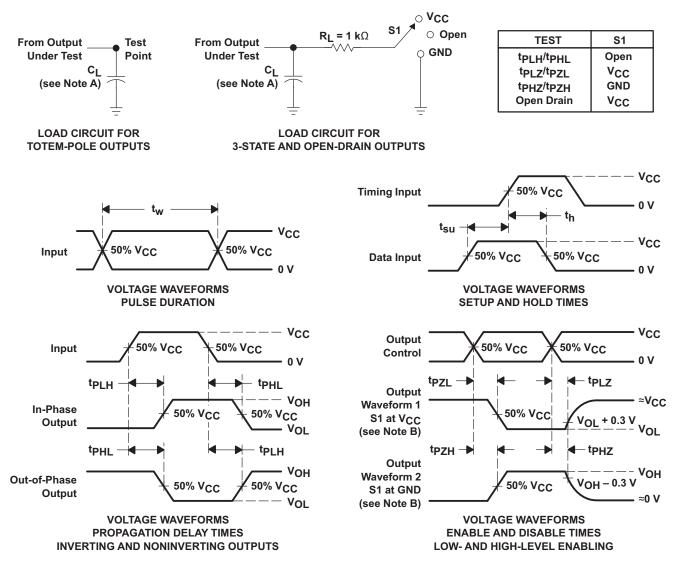


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6 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_\Gamma \leq 3 \ ns$, $t_f \leq 3 \ ns$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms



7 Detailed Description

7.1 Overview

The SN74AHC132 is a quadruple 2-input positive-NAND gate with low drive that produces slow rise and fall times. This reduces ringing on the output signal.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

7.2 Functional Block Diagram

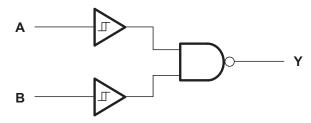


Figure 7-1. Logic Diagram, Each Gate (Positive Logic)

7.3 Feature Description

- · Wide operating voltage range
 - Operates from 2 V to 5.5 V
- · Allows down voltage translation
 - Inputs accept voltages to 5.5 V

7.4 Device Functional Modes

Table 7-1. Function Table (Each Gate)

INF	PUTS	OUTPUT
Α	В	Y
Н	Н	L
L	X	Н
X	L	Н

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC132 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} , thus making the device an excellent choice for down translation.

8.2 Typical Application

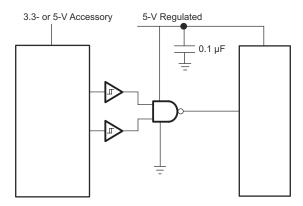


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

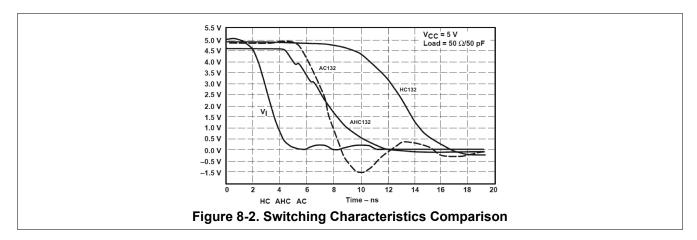
- 1. Recommended input conditions:
 - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- 2. Recommend output conditions:
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC}.

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8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply-voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, $0.1\mu F$ is recommended. If there are multiple V_{CC} pins, then a $0.01~\mu F$ or a $0.022~\mu F$ is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A $0.1~\mu F$ and a $1~\mu F$ are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in the *Layout Examples* are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

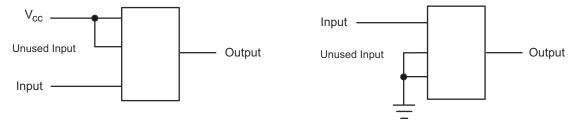


Figure 8-3. Layout Diagram

Product Folder Links: SN74AHC132

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note
- Texas Instruments, Implications of Slow or Floating CMOS Inputs application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision I (August 2023) to Revision J (October 2023)

Page

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN74AHC132BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC132
SN74AHC132BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC132
SN74AHC132D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	AHC132
SN74AHC132DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA132
SN74AHC132DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA132
SN74AHC132DGVR	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA132
SN74AHC132DGVR.A	Active	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA132
SN74AHC132DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC132
SN74AHC132DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC132
SN74AHC132N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC132N
SN74AHC132N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC132N
SN74AHC132NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC132
SN74AHC132NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC132
SN74AHC132PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	HA132
SN74AHC132PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HA132
SN74AHC132PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA132
SN74AHC132RGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA132
SN74AHC132RGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA132

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

INSTRUMENTS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC132BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC132DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC132DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC132DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC132NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC132PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC132RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC132BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC132DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC132DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC132DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC132DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC132NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC132PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC132RGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHC132N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC132N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC132N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC132N.A	N	PDIP	14	25	506	13.97	11230	4.32

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
 The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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