SNx4AHC125 Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- Operating range of 2V to 5.5V
- Latch-up performance exceeds 250mA per JESD 17
- Four individual output enable pins

2 Applications

- Flow Meters
- Programmable Logic Controllers
- Power Over Ethernet (PoE)
- Motor Drives and Controls
- Electronic Point-of-Sale

3 Description

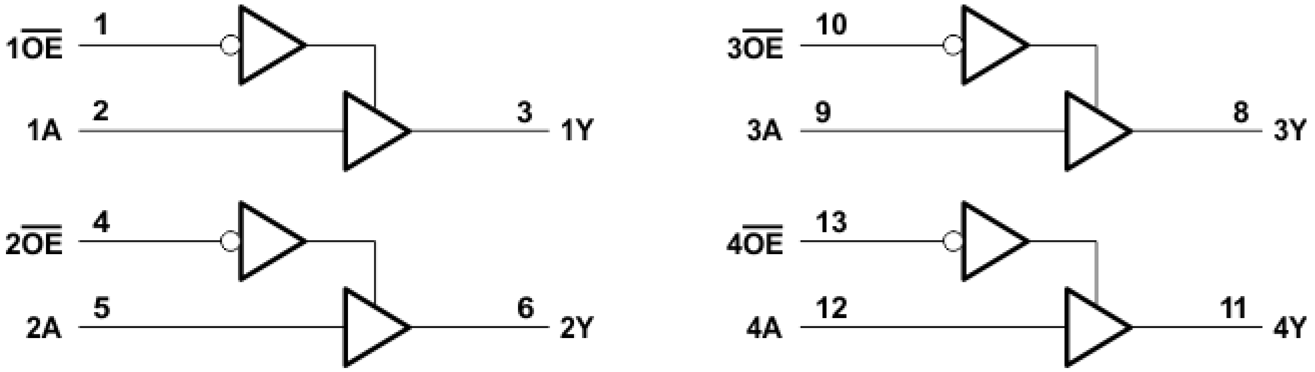
The SNx4AHC125 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE[2]
SN54AHC125	J (CDIP, 14)	8.89mm 8.89mm
	W (CFP, 14)	19.56mm × 6.67mm
	FK (LCCC, 20)	9.21mm × 5.97mm
SN74AHC125	DB (SSOP, 14)	6.20mm 5.30mm
	D (SOIC, 14)	8.65mm × 3.91mm
	NS (SO, 14)	10.30mm × 5.30mm
	DGV (TVSOP, 14)	3.60mm × 4.40mm
	PW (TSSOP, 14)	5.00mm × 4.40mm
	N (PDIP, 14)	19.30mm × 6.35mm
	RGY (VQFN, 14)	3.50mm × 3.50mm
	BQA (WQFN, 14)	3mm × 2.5mm

(1) For more information, see Section 11.
(2) The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

Logic Diagram (Positive Logic)

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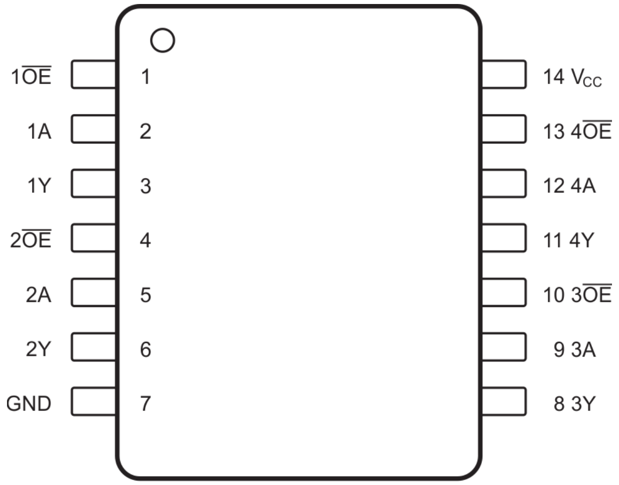
4 Pin Configuration and Functions



Not to scale

Figure 4-1. D, DB, DGV, N, NS, J, W, or PW Package 14-Pin SOIC, SSOP, TVSOP, PDIP, SO, CDIP, CFP, or TSSOP Top View

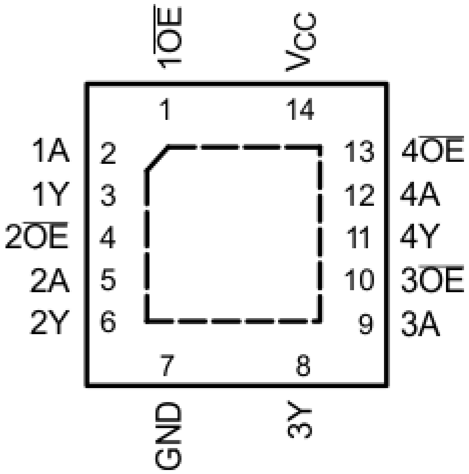


Figure 4-2. RGY or BQA Package 14-Pin VQFN Top View

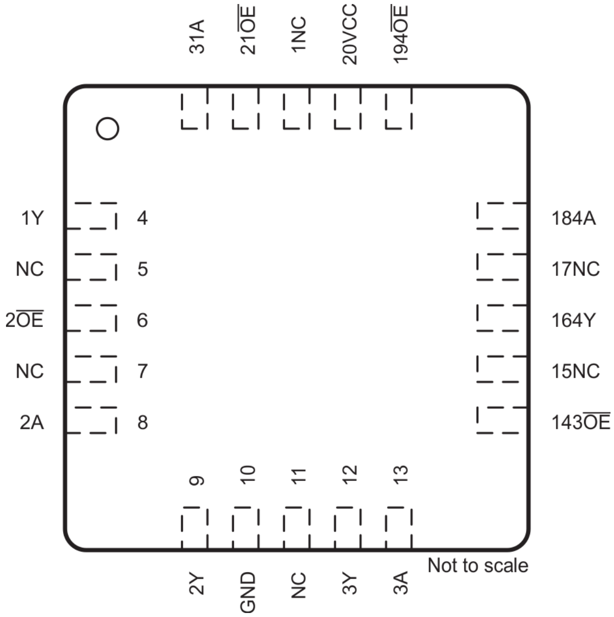


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Figure 4-3. FK Package 20-Pin LCCC Top View

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, PDIP, SO, CDIP, CFP, TSSOP, VQFN	LCCC		
1 $\overline{\text{OE}}$	1	2	I	Output enable for gate 1
1A	2	3	I	Gate 1 input
1Y	3	4	O	Gate 1 output
2 $\overline{\text{OE}}$	4	6	I	Output enable for gate 2
2A	5	8	I	Gate 2 input
2Y	6	9	O	Gate 2 output
3 $\overline{\text{OE}}$	10	14	I	Output enable for gate 3
3A	9	13	I	Gate 3 input
3Y	8	12	O	Gate 3 output
4 $\overline{\text{OE}}$	13	19	I	Output enable for gate 4
4A	12	18	I	Gate 4 input
4Y	11	16	O	Gate 4 output
GND	7	10	—	Ground pin
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection
V_{CC}	14	20	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–0.5	7	V
Input voltage(2)		–0.5	7	V
Output voltage(2)		–0.5	V_{CC} + 0.5	V
Input clamp current	$V_I < 0$		–20	mA
Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Continuous output current	V_O = 0 to V_{CC}		±25	mA
Continuous current through V_{CC} or GND			±50	mA
Virtual operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level Input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ±0.3 V		–4	mA
		V_{CC} = 5 V ±0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ±0.3 V		4	mA
		V_{CC} = 5 V ±0.5 V		8	
Δt/Δv	Input Transition rise or fall rate	V_{CC} = 3.3 V ±0.3 V		100	ns/V
		V_{CC} = 5 V ±0.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		SNx4AHC125								UNIT
		D (SOIC)	DB (SSOP)	NS (SO)	DGV (TVSOP)	PW (TSSOP)	N (PDIP)	RGY (VQFN)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	107.3	89.9	134.6	147.7	56.3	87.1	88.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	59.3	47.7	53.9	77.4	43.9	92.6	90.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81	54.7	48.6	63.8	90.9	36.1	62.5	56.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	37	24	17.5	6.3	27.2	29.2	22.8	9.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	80.6	54.1	48.3	63.2	90.2	36	61.7	56.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	45.1	33.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 μA	V_{CC} = 2 V	T_A = 25°C	1.9	2		V
			T_A = –55°C to 125°C (SN54AHC125)	1.9			
			T_A = –40°C to 85°C (SN74AHC125)	1.9			
			T_A = –40°C to 125°C (recommended SN74AHC125)	1.9			
		V_{CC} = 3 V	T_A = 25°C	2.9	3		
			T_A = –55°C to 125°C (SN54AHC125)	2.9			
			T_A = –40°C to 85°C (SN74AHC125)	2.9			
			T_A = –40°C to 125°C (recommended SN74AHC125)	2.9			
		V_{CC} = 4.5 V	T_A = 25°C	4.4	4.5		
			T_A = –55°C to 125°C (SN54AHC125)	4.4			
			T_A = –40°C to 85°C (SN74AHC125)	4.4			
			T_A = –40°C to 125°C (recommended SN74AHC125)	4.4			
	I_{OH} = –4 mA and V_{CC} = 3 V		T_A = 25°C	2.58			
			T_A = –55°C to 125°C (SN54AHC125)	2.48			
			T_A = –40°C to 85°C (SN74AHC125)	2.48			
			T_A = –40°C to 125°C (recommended SN74AHC125)	2.48			
	I_{OH} = –8 mA and V_{CC} = 4.5 V		T_A = 25°C	3.94			
			T_A = –55°C to 125°C (SN54AHC125)	3.8			
			T_A = –40°C to 85°C (SN74AHC125)	3.8			
			T_A = –40°C to 125°C (recommended SN74AHC125)	3.8			

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	I_{OL} = 50 µA	V_{CC} = 2 V	T_A = 25°C			0.1	V
			T_A = –55°C to 125°C (SN54AHC125)			0.1	
			T_A = –40°C to 85°C (SN74AHC125)			0.1	
			T_A = –40°C to 125°C (recommended SN74AHC125)			0.1	
		V_{CC} = 3 V	T_A = 25°C			0.1	
			T_A = –55°C to 125°C (SN54AHC125)			0.1	
			T_A = –40°C to 85°C (SN74AHC125)			0.1	
			T_A = –40°C to 125°C (recommended SN74AHC125)			0.1	
		V_{CC} = 4.5 V	T_A = 25°C			0.1	
			T_A = –55°C to 125°C (SN54AHC125)			0.1	
			T_A = –40°C to 85°C (SN74AHC125)			0.1	
			T_A = –40°C to 125°C (recommended SN74AHC125)			0.1	
	I_{OH} = 4 mA and V_{CC} = 3 V		T_A = 25°C			0.36	
			T_A = –55°C to 125°C (SN54AHC125)			0.5	
			T_A = –40°C to 85°C (SN74AHC125)			0.44	
			T_A = –40°C to 125°C (recommended SN74AHC125)			0.5	
	I_{OH} = 8 mA and V_{CC} = 4.5 V		T_A = 25°C			0.36	
			T_A = –55°C to 125°C (SN54AHC125)			0.5	
			T_A = –40°C to 85°C (SN74AHC125)			0.44	
			T_A = –40°C to 125°C (recommended SN74AHC125)			0.5	
I_I	V_I = 5.5 V or GND and V_{CC} = 0 V to 5.5 V		T_A = 25°C			±0.1	µA
			T_A = –55°C to 125°C (SN54AHC125)			±1(1)	
			T_A = –40°C to 85°C (SN74AHC125)			±1	
			T_A = –40°C to 125°C (recommended SN74AHC125)			±1	
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5 V		T_A = 25°C			±0.25	µA
			T_A = –55°C to 125°C (SN54AHC125)			±2.5	
			T_A = –40°C to 85°C (SN74AHC125)			±2.5	
			T_A = –40°C to 125°C (recommended SN74AHC125)			±2.5	
I_{CC}	V_I = V_{CC} or GND, I_O = 0, and V_{CC} = 5.5 V		T_A = 25°C			4	µA
			T_A = –55°C to 125°C (SN54AHC125)			40	
			T_A = –40°C to 85°C (SN74AHC125)			40	
			T_A = –40°C to 125°C (recommended SN74AHC125)			40	
C_i	V_I = V_{CC} or GND and V_{CC} = 5 V		T_A = 25°C		4	10	pF
			T_A = –40°C to 85°C (SN74AHC125)			10	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range and V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}, t_{PLH}	A	Y	C_L = 15 pF	T_A = 25°C		5.6(1)	8(1)	ns
				T_A = –55°C to 125°C (SN54AHC125)	1(1)		9.5(1)	
				T_A = –40°C to 85°C (SN74AHC125)	1		9.5	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		9.5	
t_{PZL}, t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		5.4(1)	8(1)	ns
				T_A = –55°C to 125°C (SN54AHC125)	1(1)		9.5(1)	
				T_A = –40°C to 85°C (SN74AHC125)			9.5	
				T_A = –40°C to 125°C (recommended SN74AHC125)			9.5	
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		7.0(1)	9.7(1)	ns
				T_A = –55°C to 125°C (SN54AHC125)	1(1)		11.5(1)	
				T_A = –40°C to 85°C (SN74AHC125)	1(1)		11.5(1)	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1(1)		11.5(1)	
t_{PHL}, t_{PLH}	A	Y	C_L = 50 pF	T_A = 25°C		8.1	11.5	ns
				T_A = –55°C to 125°C (SN54AHC125)	1		13	
				T_A = –40°C to 85°C (SN74AHC125)	1		13	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		13	
t_{PZL}, t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		7.9	11.5	ns
				T_A = –55°C to 125°C (SN54AHC125)	1		13	
				T_A = –40°C to 85°C (SN74AHC125)	1		13	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		13	
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		9.5	13.2	ns
				T_A = –55°C to 125°C (SN54AHC125)	1		15	
				T_A = –40°C to 85°C (SN74AHC125)	1		15	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		15	
tsk(o)	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C			1.5(2)	ns
				T_A = –40°C to 85°C (SN74AHC125)			1.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range and V_{CC} = 5 V ± 0.5 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	Y	C_L = 15 pF	T_A = 25°C		3.8(1)	5.5(1)	ns
				T_A = –55°C to 125°C (SN54AHC125)	1(1)		6.5(1)	
				T_A = –40°C to 85°C (SN74AHC125)	1		6.5	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		6.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		3.6(1)	5.1(1)	ns
				T_A = –55°C to 125°C (SN54AHC125)	1(1)		6(1)	
				T_A = –40°C to 85°C (SN74AHC125)	1		6	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		4.6(1)	6.8(1)	ns
				T_A = –55°C to 125°C (SN54AHC125)	1(1)		8(1)	
				T_A = –40°C to 85°C (SN74AHC125)	1(1)		8(1)	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1(1)		8(1)	
t_{PLH}, t_{PHL}	A	Y	C_L = 50 pF	T_A = 25°C		5.3	7.5	ns
				T_A = –55°C to 125°C (SN54AHC125)	1		8.5	
				T_A = –40°C to 85°C (SN74AHC125)	1		8.5	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		8.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		5.1	7.1	ns
				T_A = –55°C to 125°C (SN54AHC125)	1		8	
				T_A = –40°C to 85°C (SN74AHC125)	1		8	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		6.1	8.8	ns
				T_A = –55°C to 125°C (SN54AHC125)	1		10	
				T_A = –40°C to 85°C (SN74AHC125)	1		10	
				T_A = –40°C to 125°C (recommended SN74AHC125)	1		10	
tsk(o)	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C			1(2)	ns
				T_A = –40°C to 85°C (SN74AHC125)			1	

5.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, and T_A = 25°C[1]

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic (V_{OL})		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic (V_{OL})		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic (V_{OH})	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load and f = 1 MHz	9.5	pF

5.10 Typical Characteristics

Figure 5-1 shows I_{CC} for varying V_{IN} values when V_{CC} is 5 V ±0.5 V and T_A = 25°C.

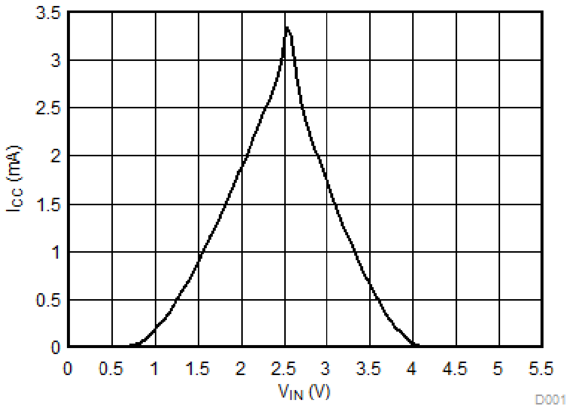
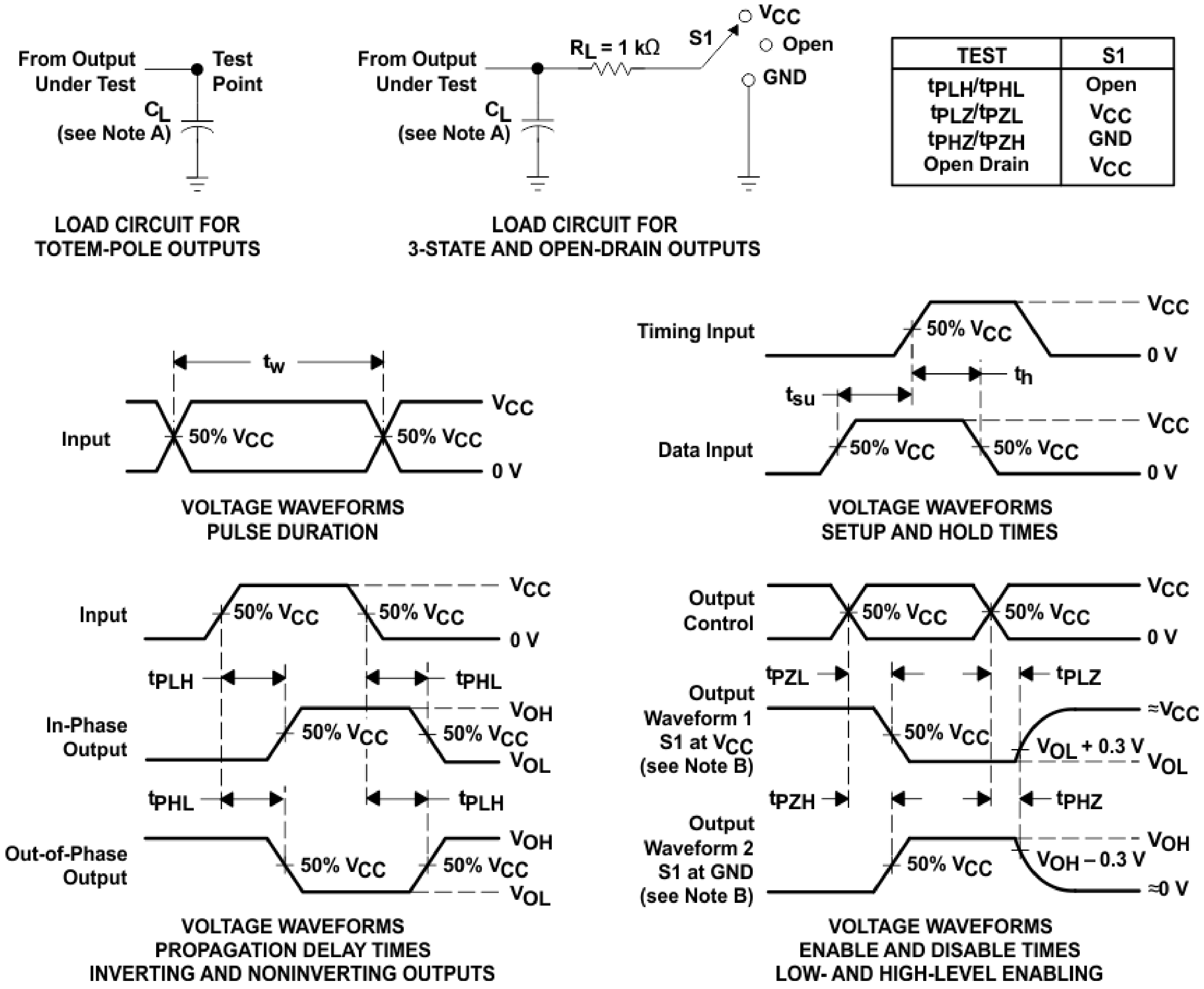


Figure 5-1. V_{IN} vs I_{CC}

6 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

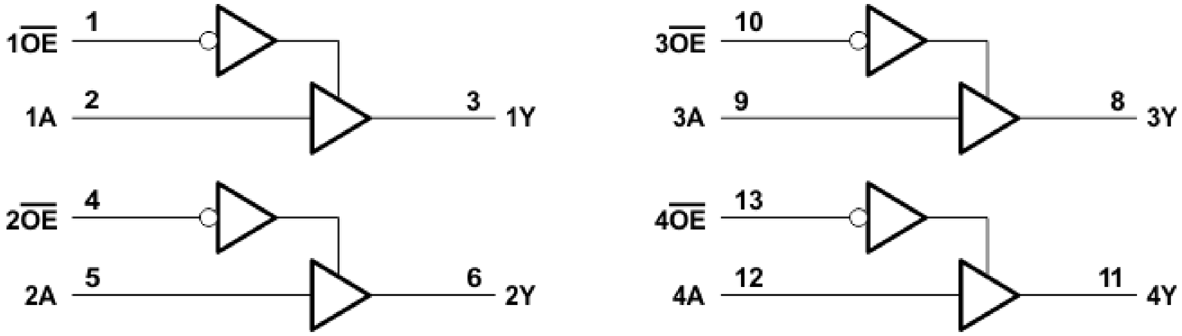
Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC125 devices have four integrated bus buffer gates. Each gate can be individually controlled from their respective output enable pins or tied together and controlled simultaneously. This allows for control of up to four different lines from one device. Often times a microcontroller have multiple function options for a single pin. By using GPIO pins to enable specific buffers, the SNx4AHC125 can act as a multiplexer to select a specific data line depending on what pin function is selected on the microcontroller. At the same time, the lines that are not selected are isolated from the pin.

7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

7.3 Feature Description

Each buffer has its own output enable. This allows for control of each buffer individually. When the output enable is LOW, the input is passed to the output. When the output enable is HIGH, the output is high impedance. This feature is useful in applications that might require isolation.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SNx4AHC125.

**Table 7-1. Function Table
(Each Buffer)**

INPUTS		OUTPUT
$\overline{\text{OE}}$	A	Y
L	H	H
L	L	L
H	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The wide operating range of the SNx4AHC125 devices allows for implementation into a variety of applications. In addition to the wide operating range, these devices differentiate from similar devices because they have four buffers that can be individually controlled through their independent output enable ($\overline{OE}$) pins. Each buffer is either enabled and passes data from A to Y, or disabled and set to a high-impedance state.

8.2 Typical Application

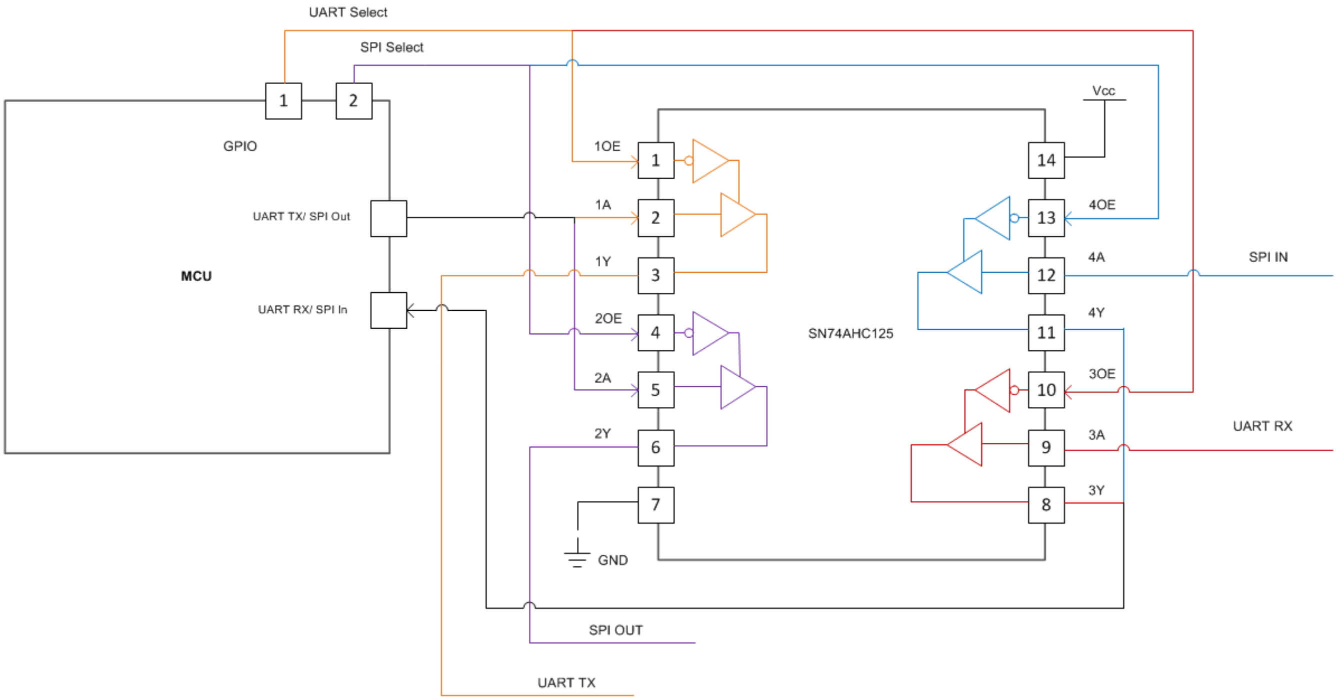


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Figure 8-1. Digital MUX

8.2.1 Design Requirements

It is best to set V_{CC} for the SN74AHC125 to the same level as the microcontroller logic levels. This allows for optimal performance. The SN74AHC125 can safely handle input levels from –0.5 V to 7 V. However, if the logic levels that are being received vary from the V_{CC} level of the device then errors can occur. For example, if V_{CC} is 5.5 V then the minimum high-level input voltage (V_{IH}) level is 3.85 V. This means if the microcontroller is sending a HIGH signal, but HIGH = 3.3 V, it would be too low a level for the SNx4AHC125 to register it as what it must be. In this case V_{CC} would need to be lowered in order to lower the V_{IH} minimum. The opposite is also true for low-level input voltage (V_{IL}). If VCC is set to 2 V, then V_{IL} maximum is 0.5 V. Depending on the microcontroller logic levels, a LOW signal may not go low enough for the SNx4AHC125 to register it.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For V_{IH} and V_{IL} levels at varying V_{CC}, see *Recommended Operating Conditions*.
   - Be mindful of rise time and fall time specifications for the output enable pins to ensure that the right buffers are enabled and the others are disabled in time. This minimizes interference on the microcontroller pin and to exterior circuitry. See *Switching Characteristics, V_{CC} = 3.3 V ±0.3 V* and *Switching Characteristics, V_{CC} = 5 V ±0.5 V* table for more details.
2. Recommended Output Conditions:
   - Load currents must not exceed I_O maximum per output and must not exceed continuous current through V_{CC} or GND total current for the part. These limits are located in the *Absolute Maximum Ratings*.
   - Outputs must not be pulled above V_{CC}.

8.2.3 Application Curves

Typical device at 25°C

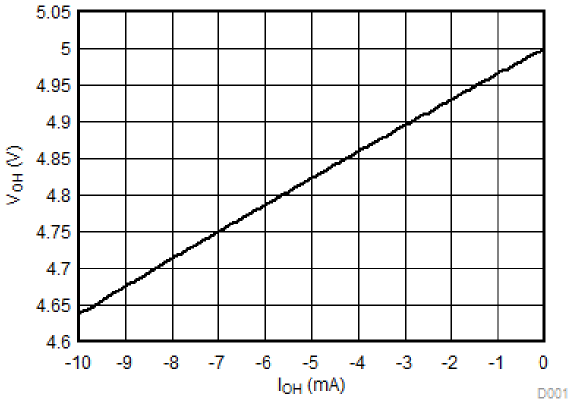


Figure 8-2. I_{OH} vs V_{OH}

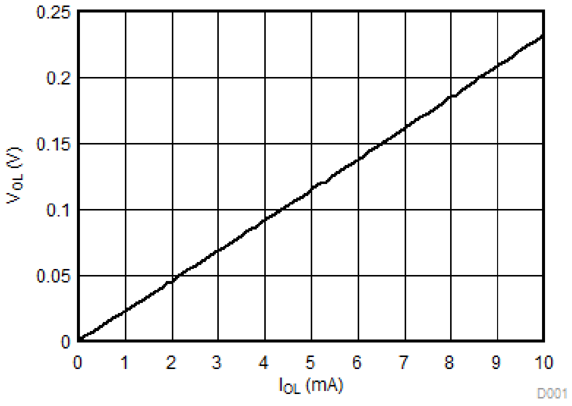


Figure 8-3. I_{OL} vs V_{OL}

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} (whichever make more sense or is more convenient).

8.4.1.1 Layout Example

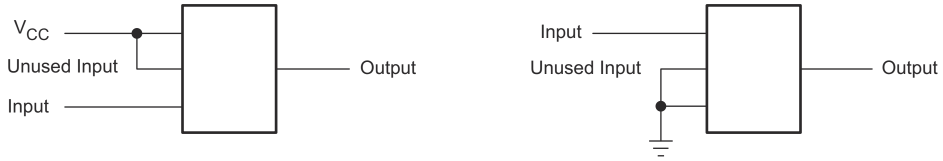


Figure 8-4. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

9.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC125	Click here	Click here	Click here	Click here	Click here
SN74AHC125	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (October 2023) to Revision O (February 2024) **Page**

- Updated thermal values for RGY package from RθJA = 55.1 to 87.1, RθJC(top) = 52.3 to 92.6, RθJB = 49.4 to 30.9, ΨJT = 14.6 to 2.4, ΨJB = 31 to 61.7, RθJC(bot) = 12.7 to 45.1, all values in °C/W 6

Changes from Revision M (June 2023) to Revision N (October 2023)	**Page**
• Updated D and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9686801Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801Q2A SNJ54AHC125FK
5962-9686801QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801QCA SNJ54AHC125J
5962-9686801QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801QDA SNJ54AHC125W
SN74AHC125BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC125
SN74AHC125BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SELECTIVE AG (TOP SIDE)	Level-1-260C-UNLIM	-40 to 125	AHC125
SN74AHC125D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	AHC125
SN74AHC125DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125DGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125DGVR.A	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125
SN74AHC125DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125
SN74AHC125N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC125N
SN74AHC125N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC125N
SN74AHC125NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC125N
SN74AHC125NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125
SN74AHC125NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125
SN74AHC125PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125RGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125RGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SN74AHC125RGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC125RGYRG4.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125
SNJ54AHC125FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801Q2A SNJ54AHC125FK
SNJ54AHC125FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801Q2A SNJ54AHC125FK
SNJ54AHC125J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801QCA SNJ54AHC125J
SNJ54AHC125J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801QCA SNJ54AHC125J
SNJ54AHC125W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801QDA SNJ54AHC125W
SNJ54AHC125W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686801QDA SNJ54AHC125W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC125, SN74AHC125 :

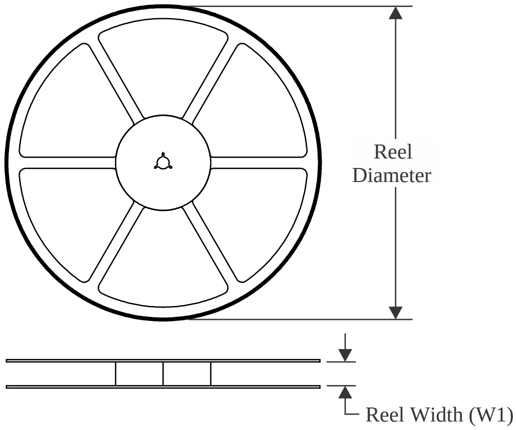
- Catalog : SN74AHC125
- Automotive : SN74AHC125-Q1, SN74AHC125-Q1
- Enhanced Product : SN74AHC125-EP, SN74AHC125-EP
- Military : SN54AHC125

NOTE: Qualified Version Definitions:

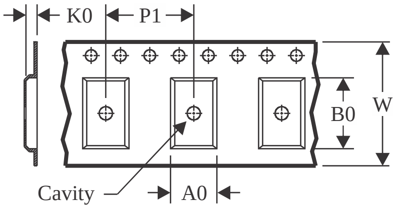
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

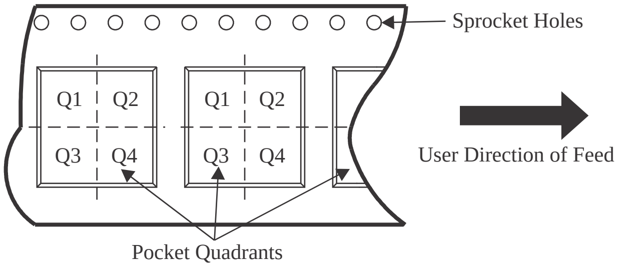


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

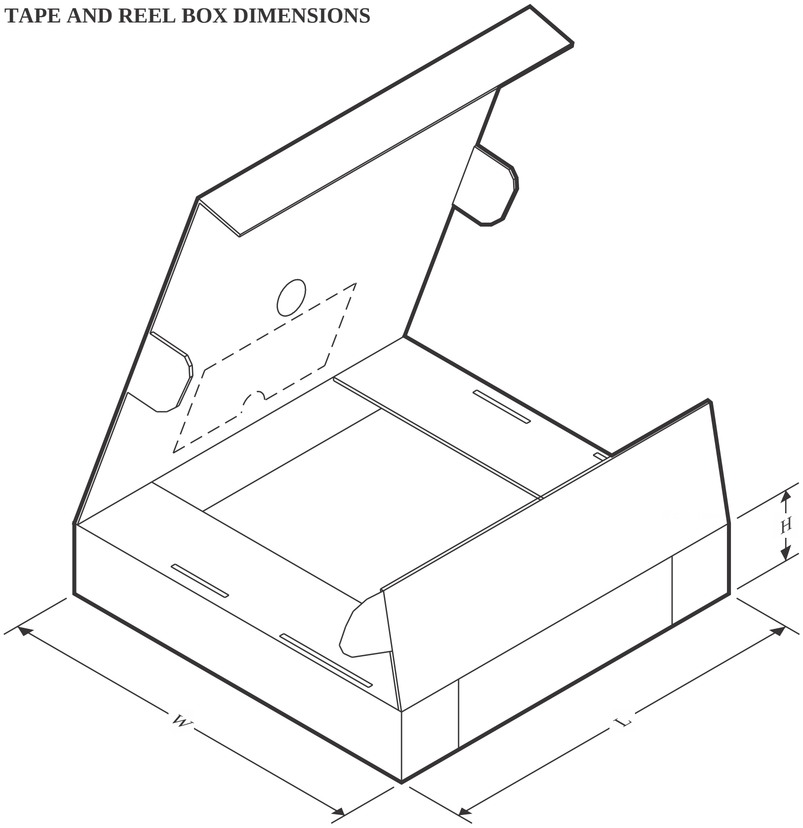
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC125DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC125RGYRG4	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

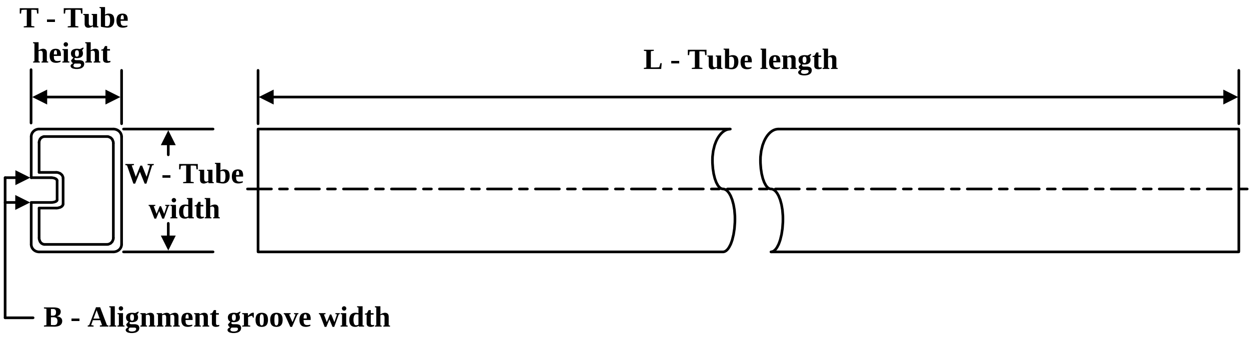
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC125DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AHC125DGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74AHC125DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC125DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC125DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC125NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHC125PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0
SN74AHC125RGYRG4	VQFN	RGY	14	3000	360.0	360.0	36.0

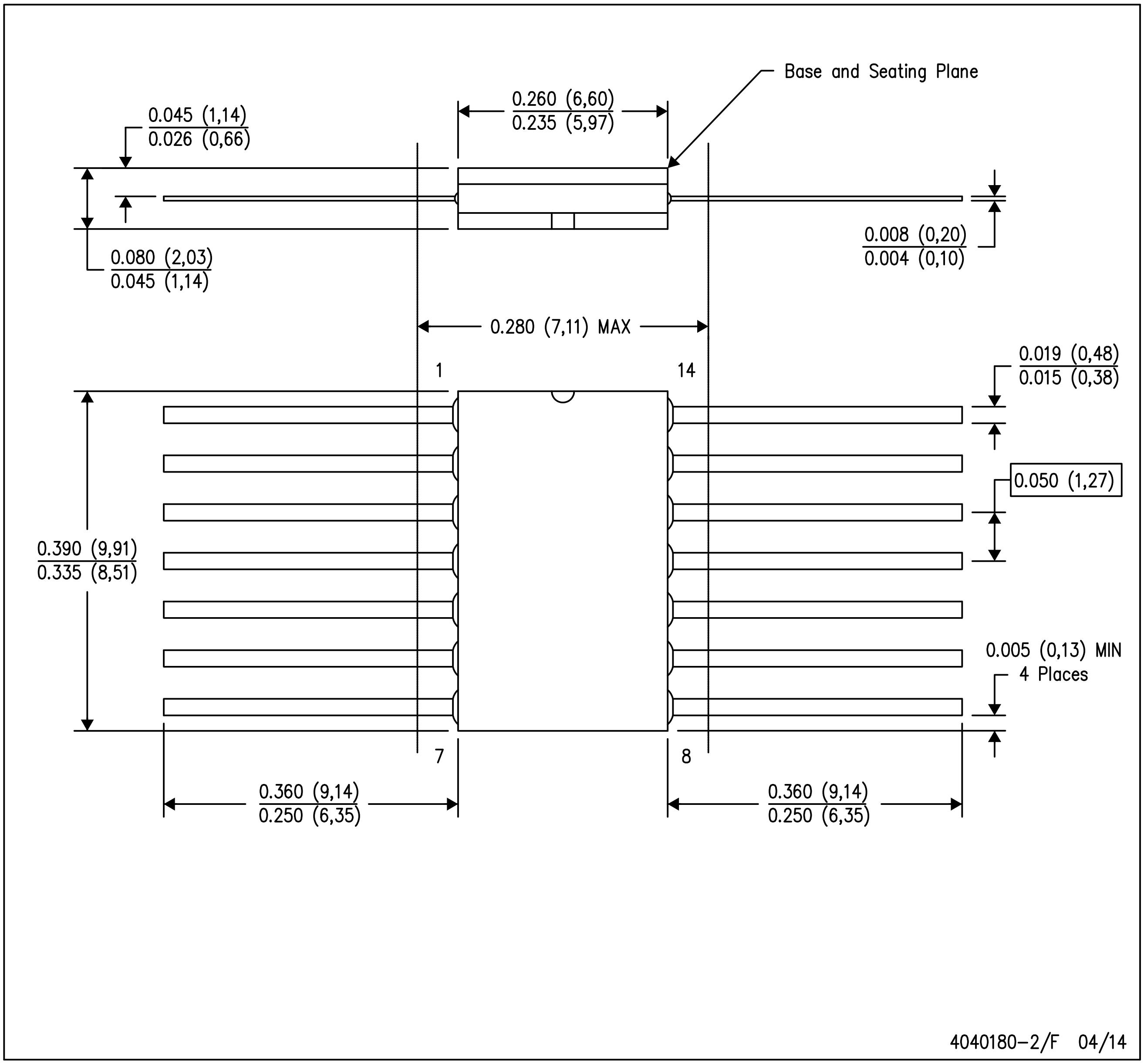
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9686801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686801QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC125FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC125FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC125W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AHC125W.A	W	CFP	14	25	506.98	26.16	6220	NA

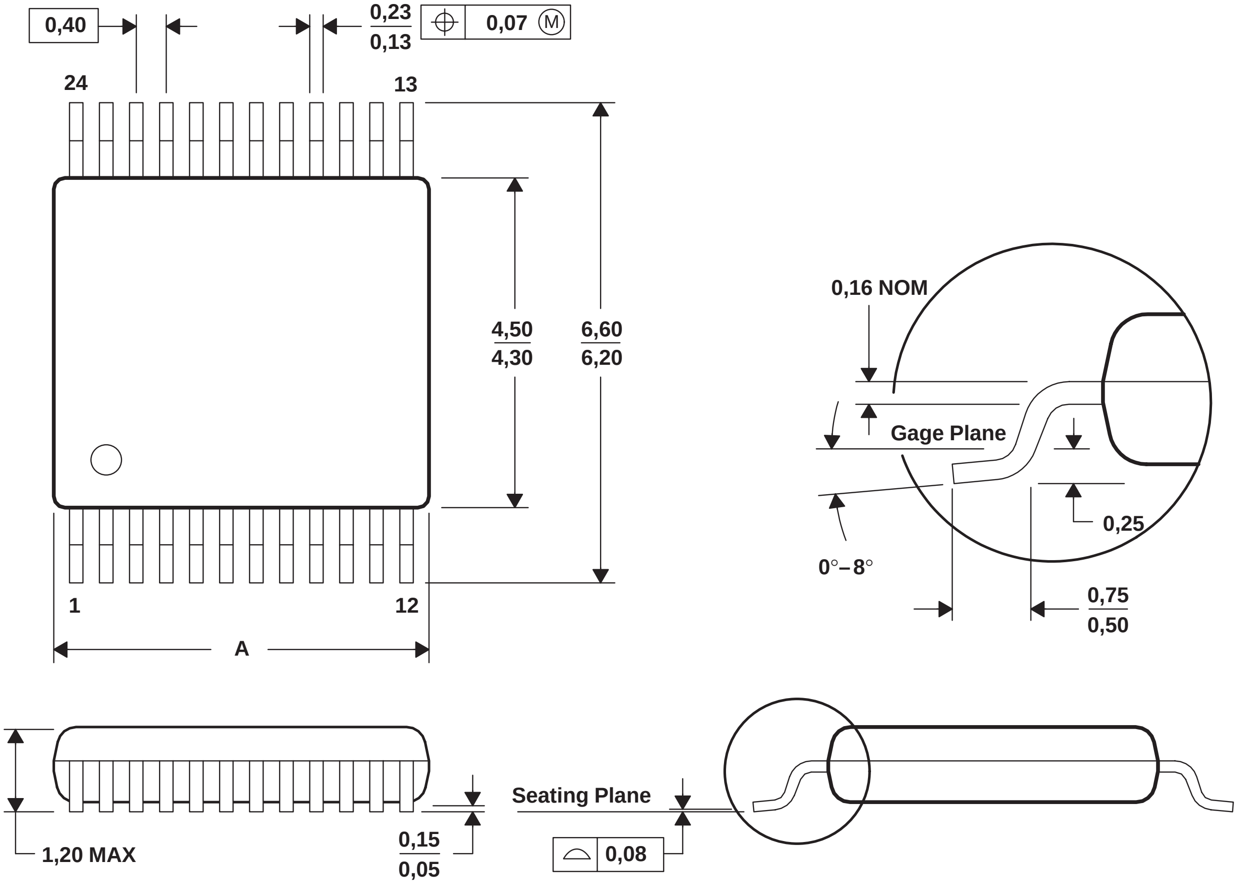
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

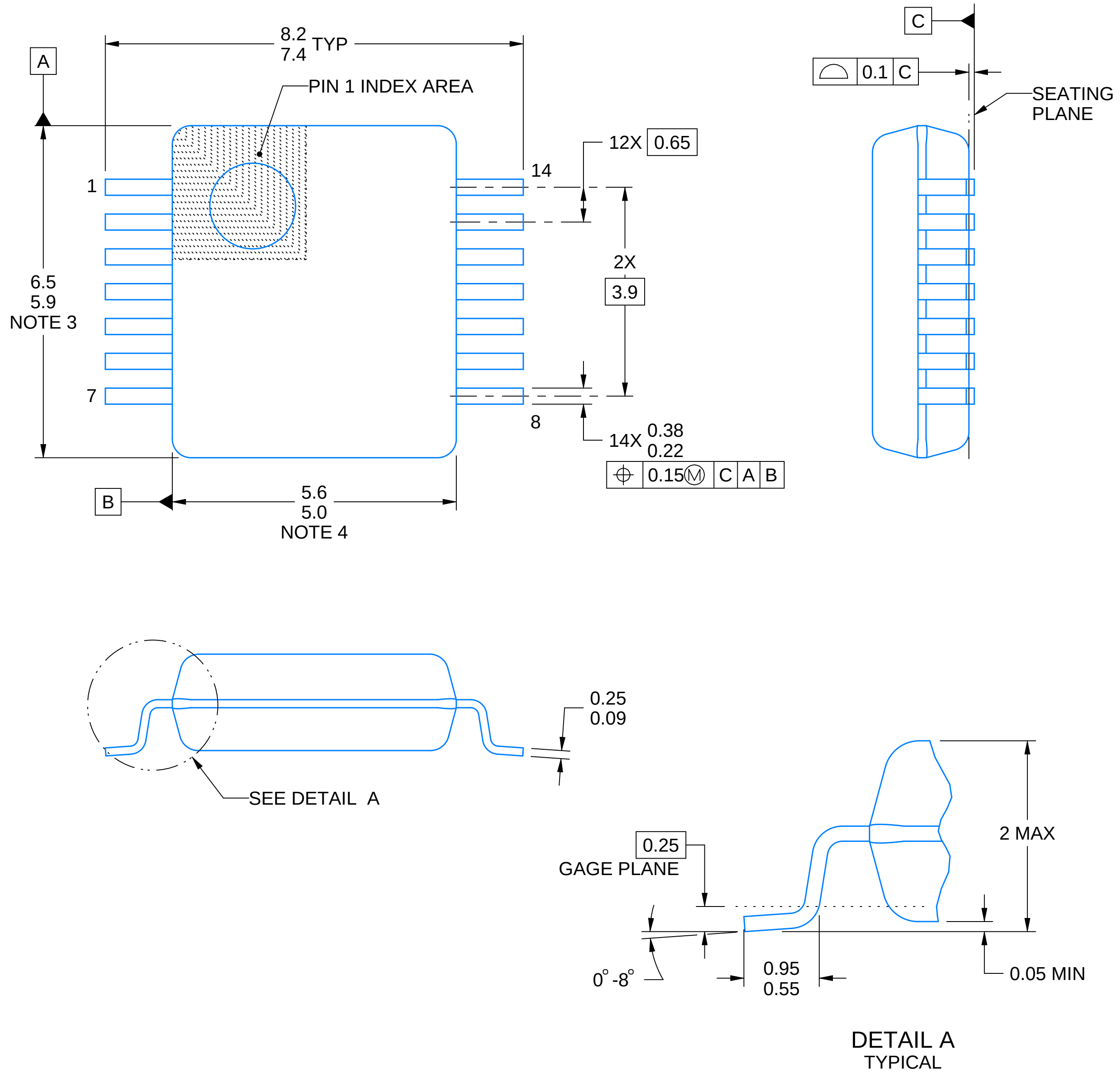
24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

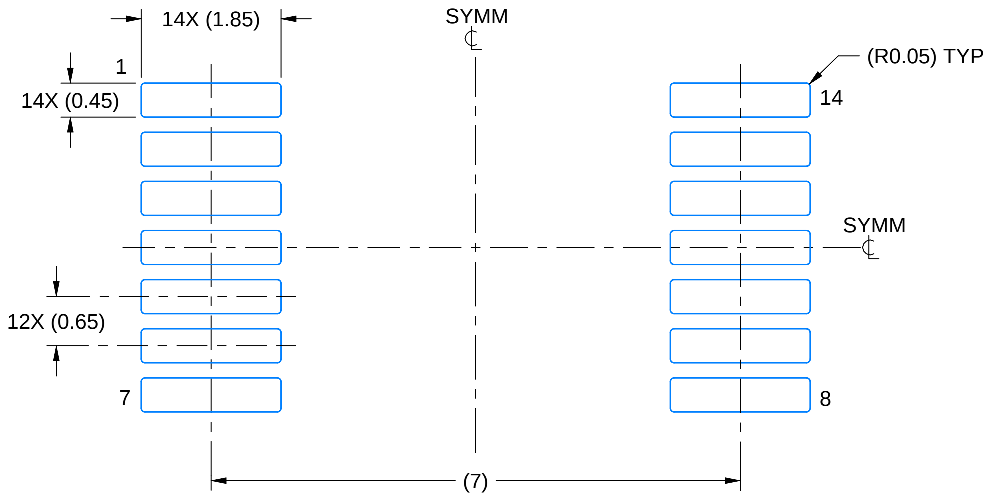
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194



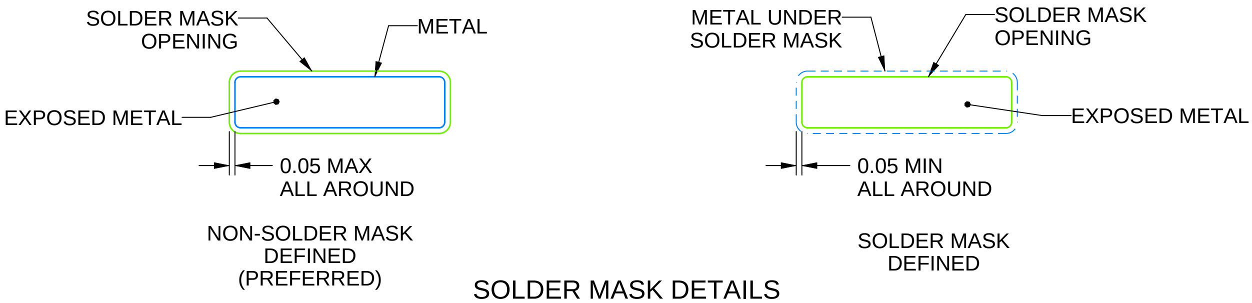
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

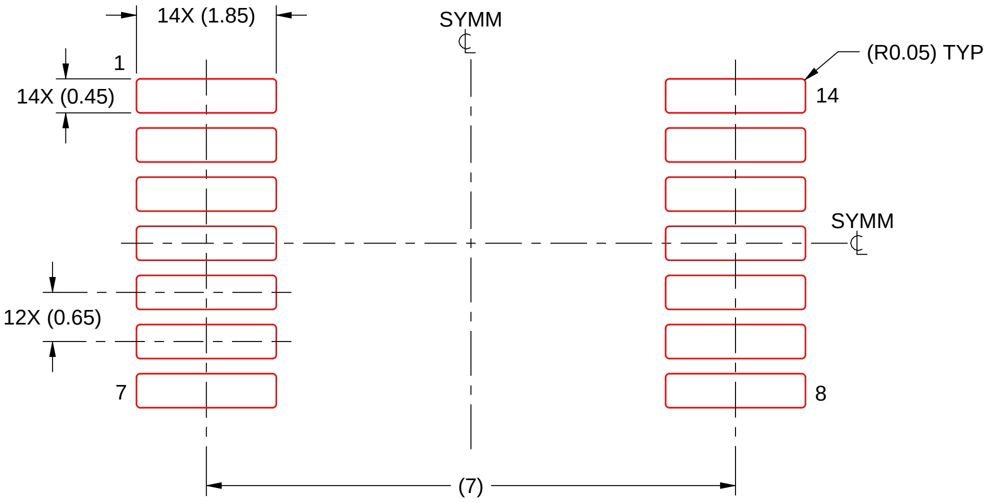


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

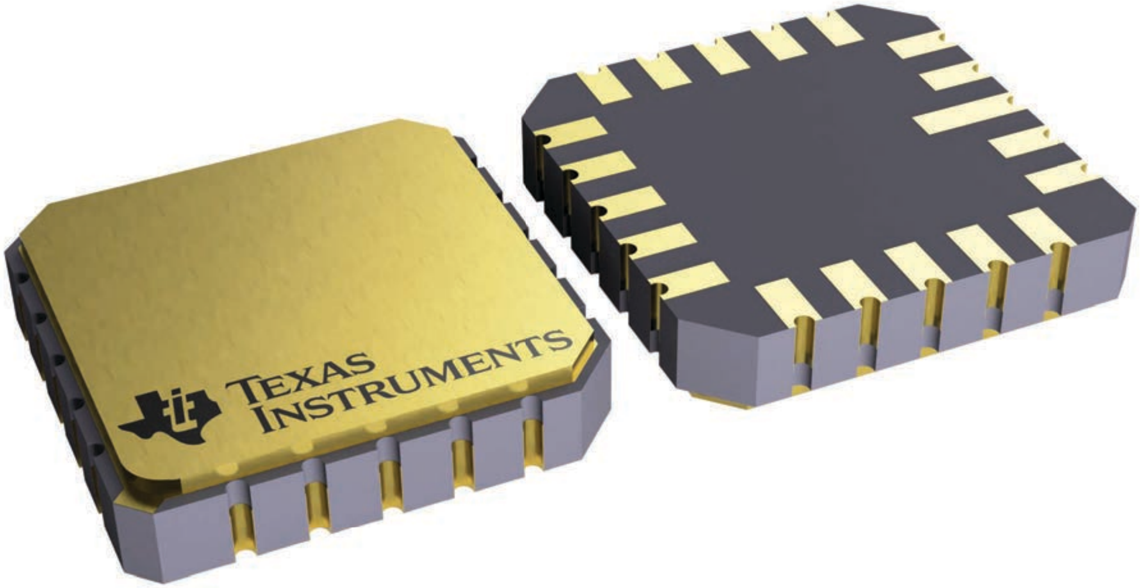
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20 **LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch LEADLESS CERAMIC CHIP CARRIER

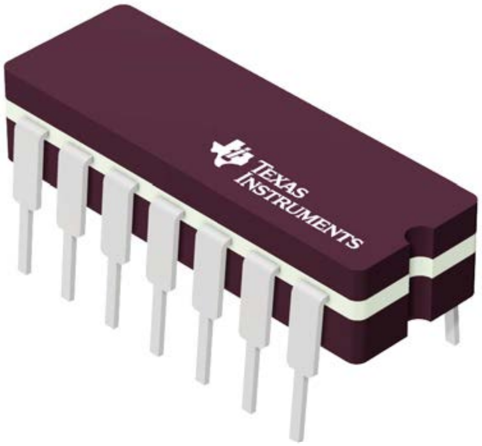
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



J 14

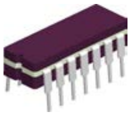
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

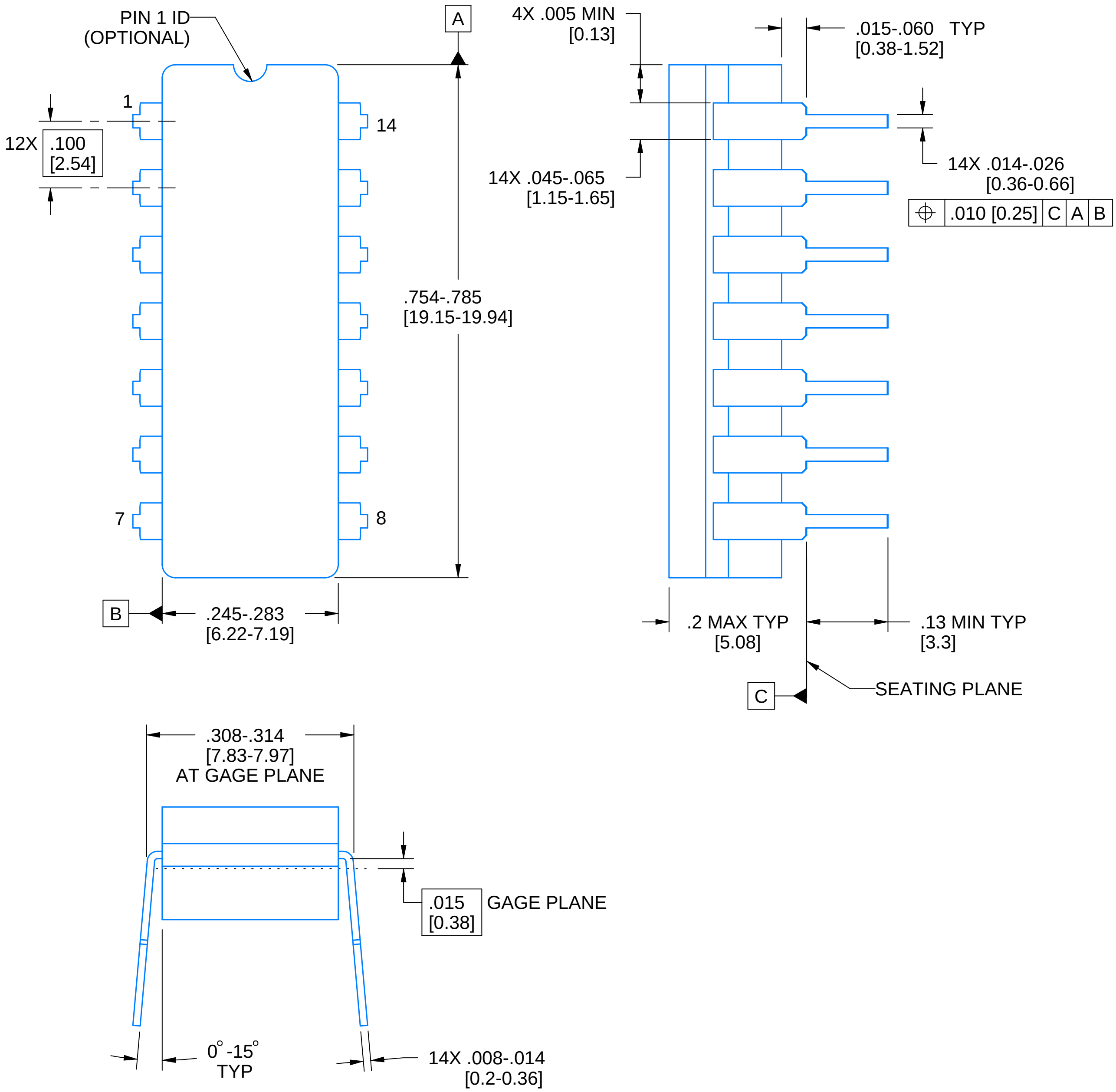


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

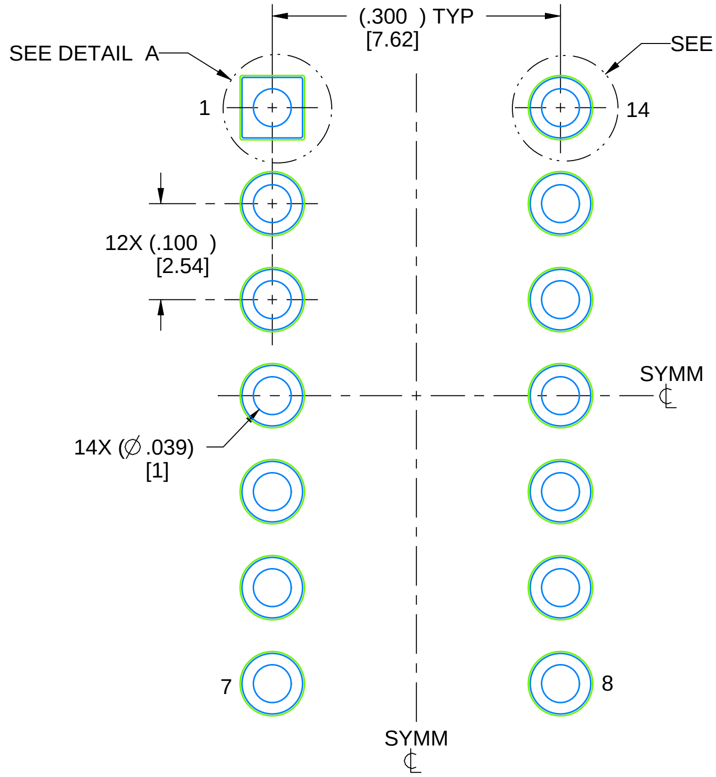
CERAMIC DUAL IN LINE PACKAGE



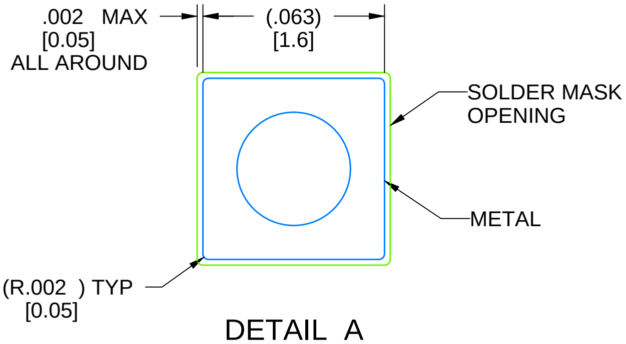
4214771/A 05/2017

NOTES:

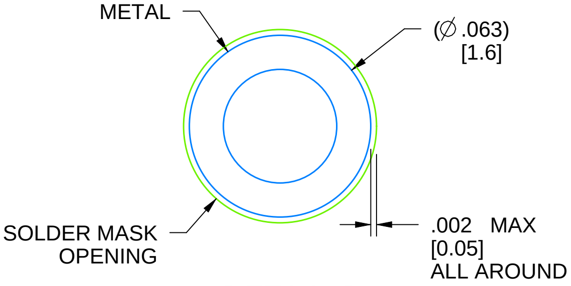
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

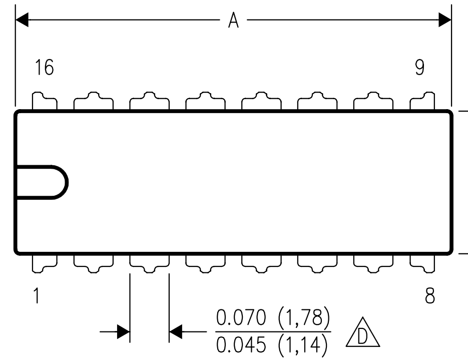


DETAIL B
13X, SCALE: 15X

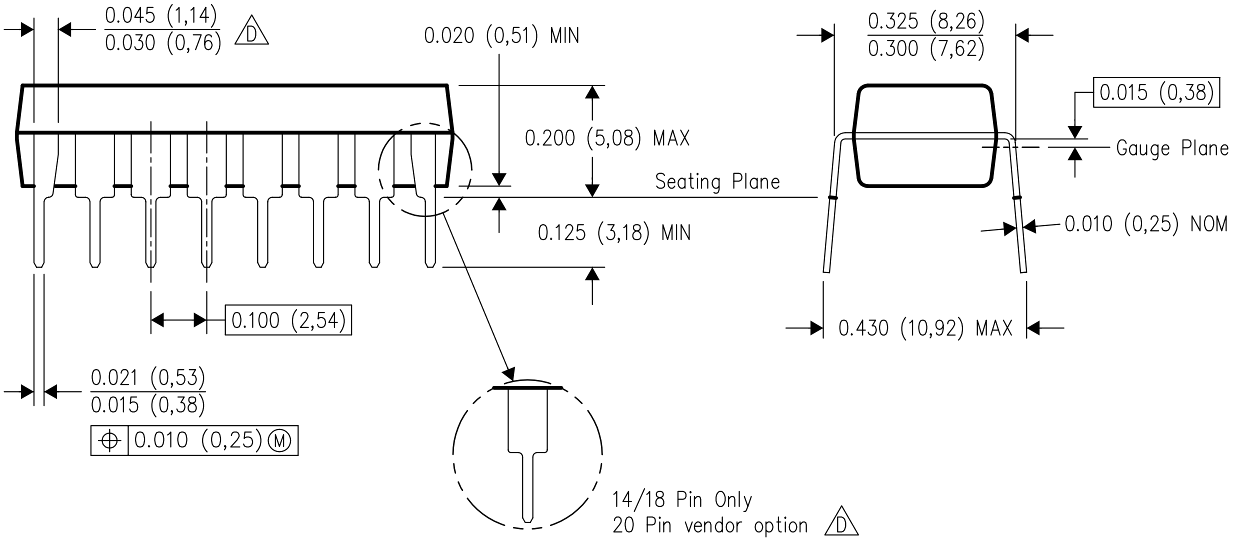
4214771/A 05/2017

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

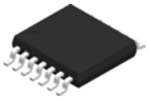


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

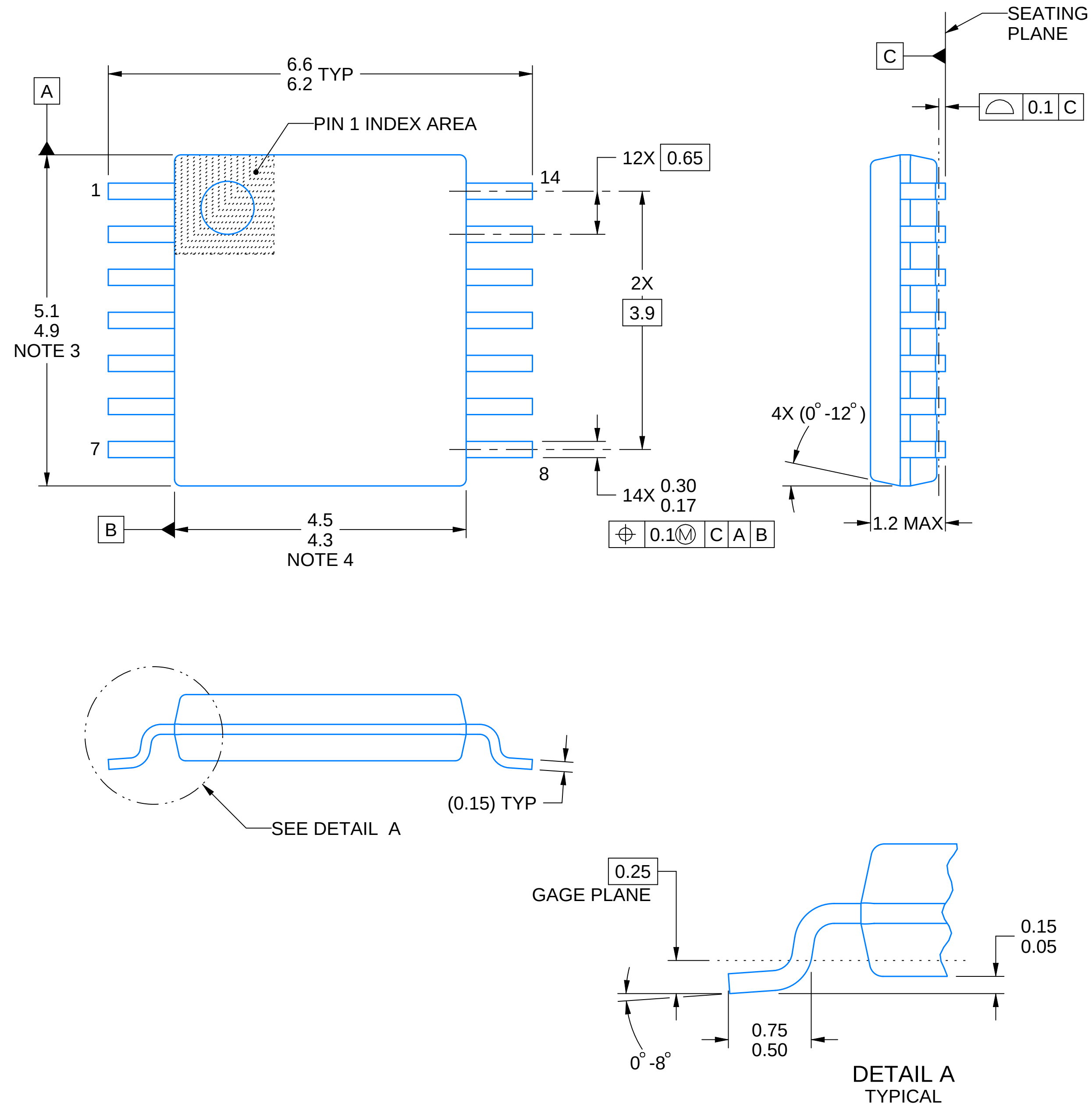
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

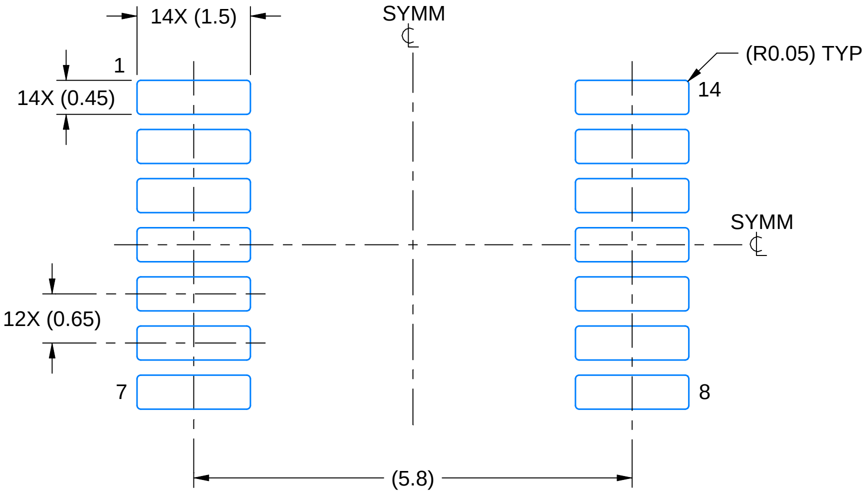
SMALL OUTLINE PACKAGE



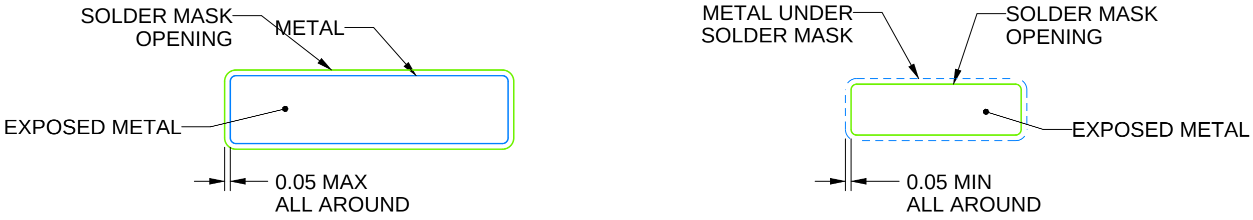
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)

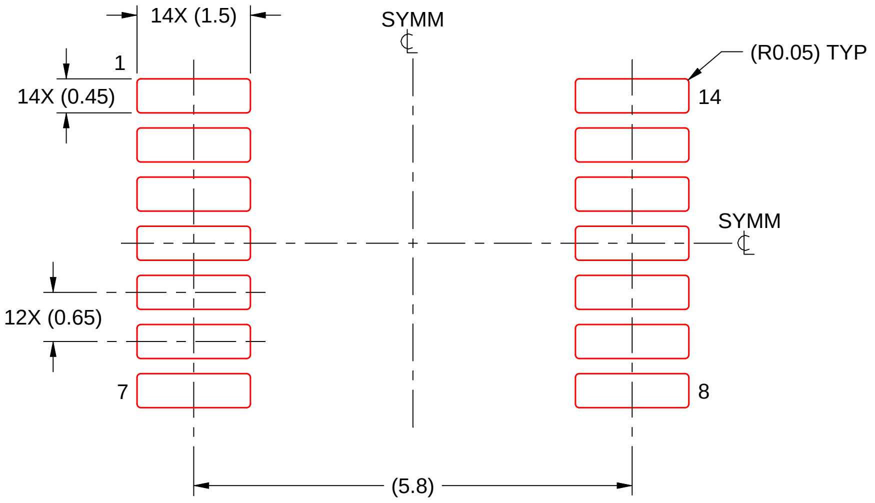
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

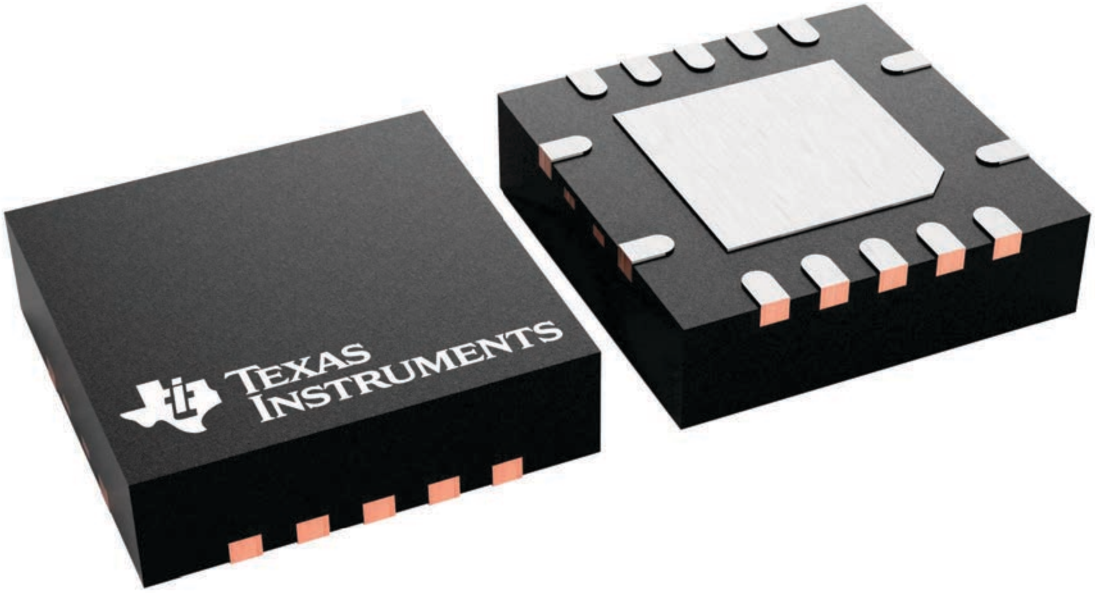
RGY 14

VQFN - 1 mm max height

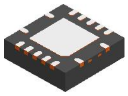
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



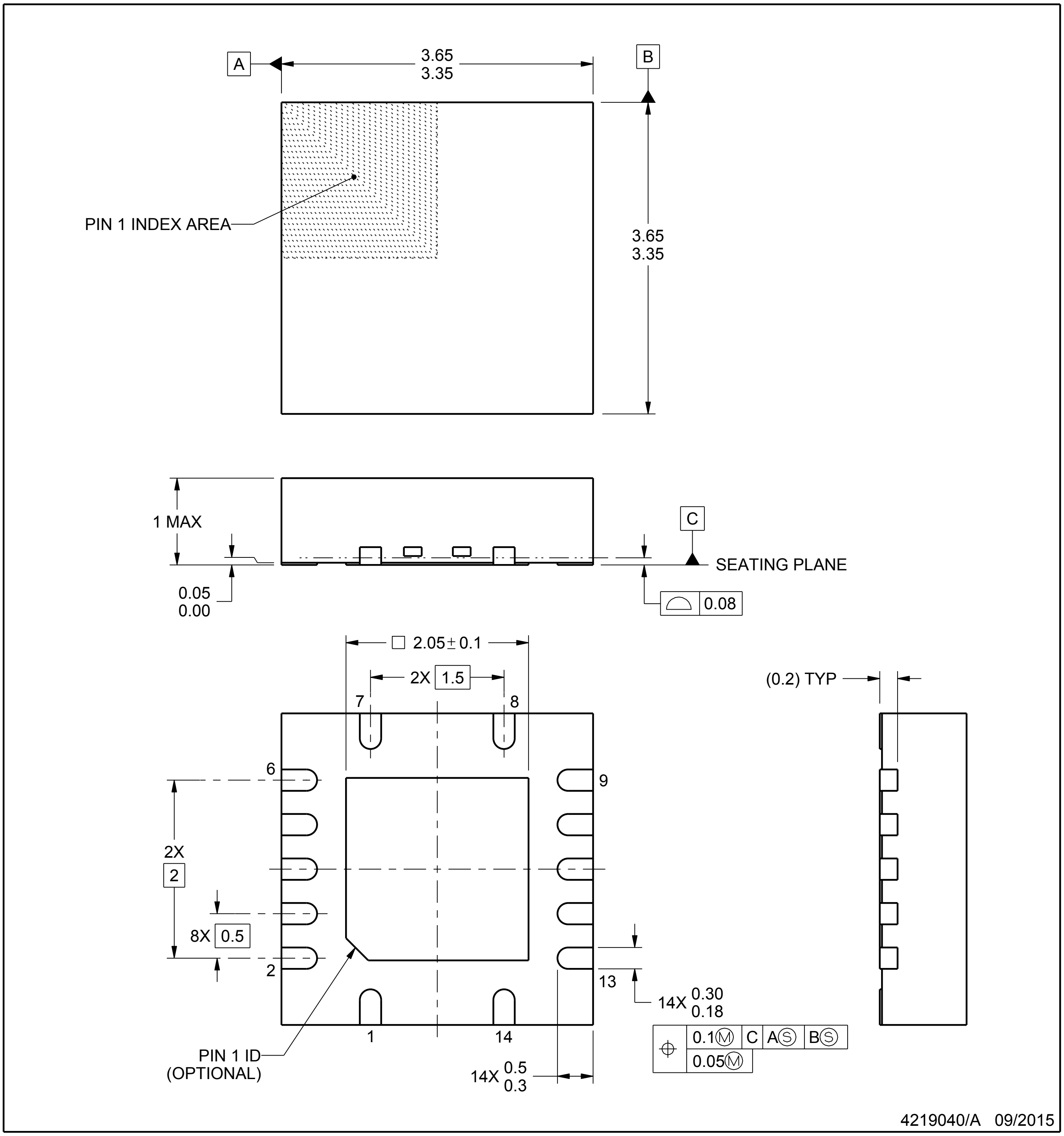
PACKAGE OUTLINE



RGY0014A

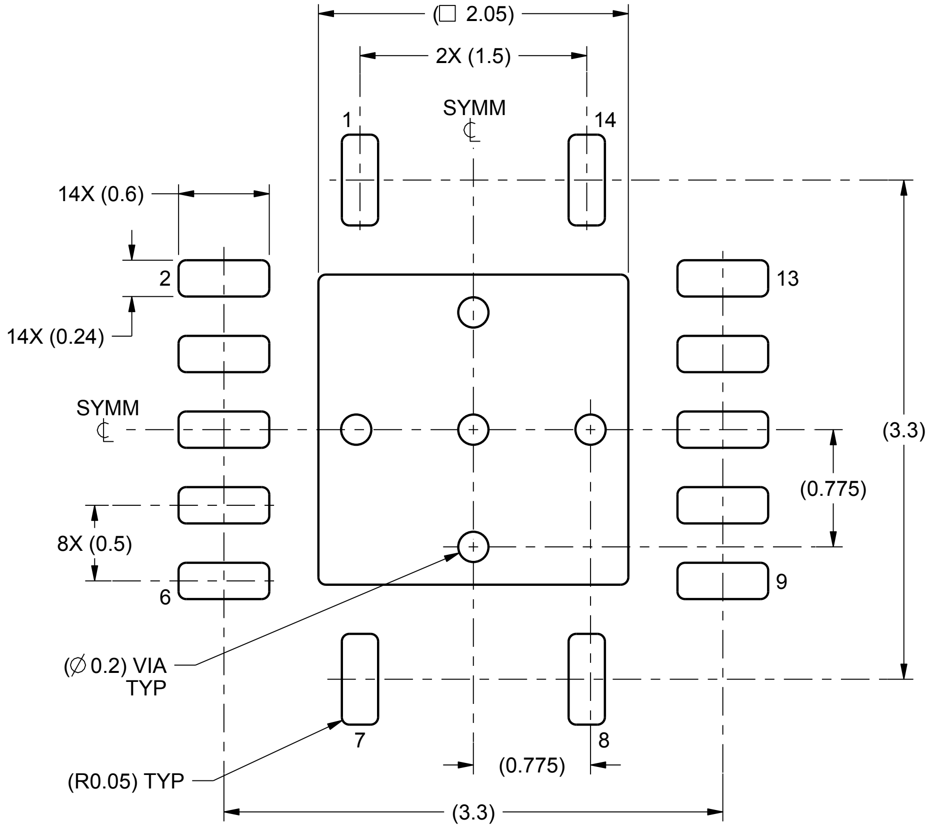
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

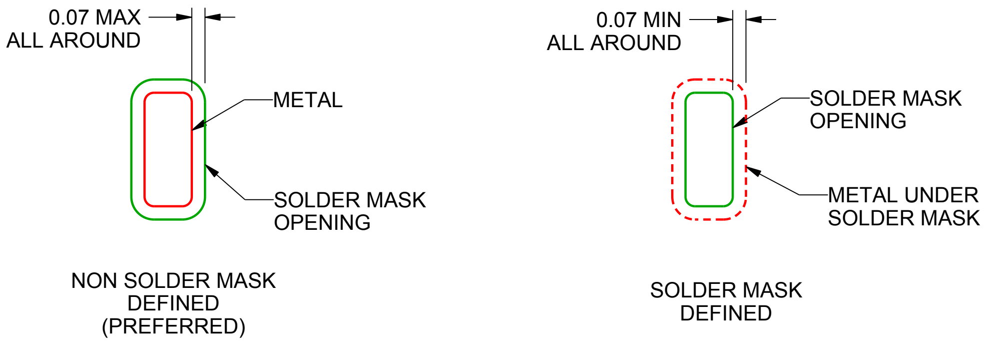


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

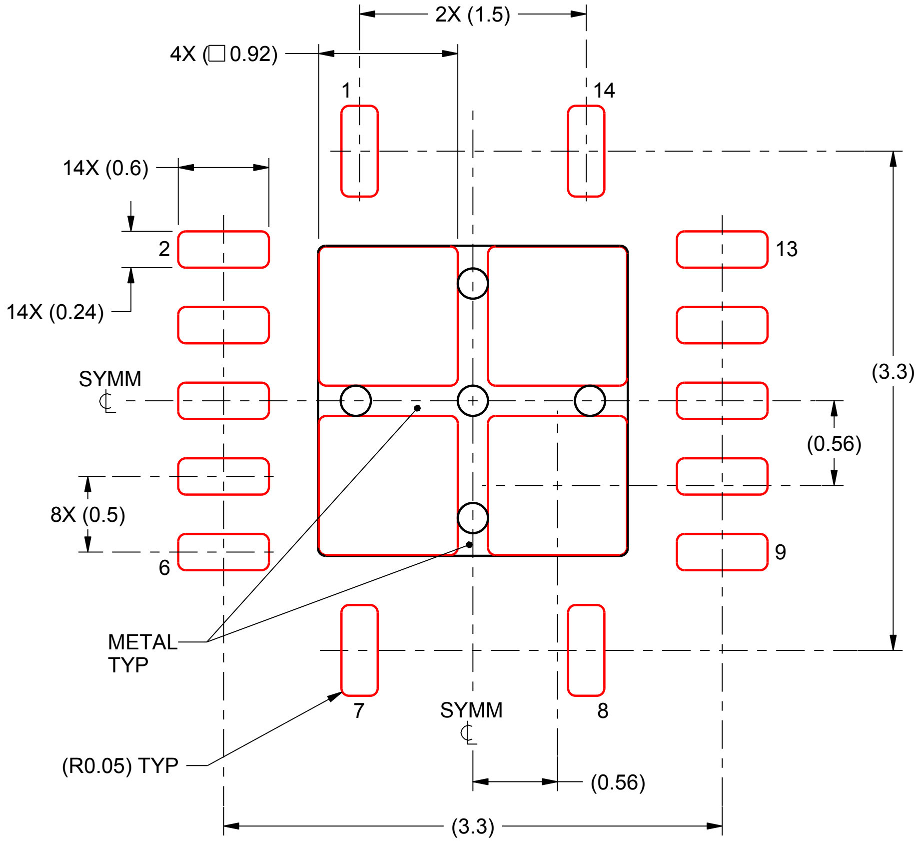


SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



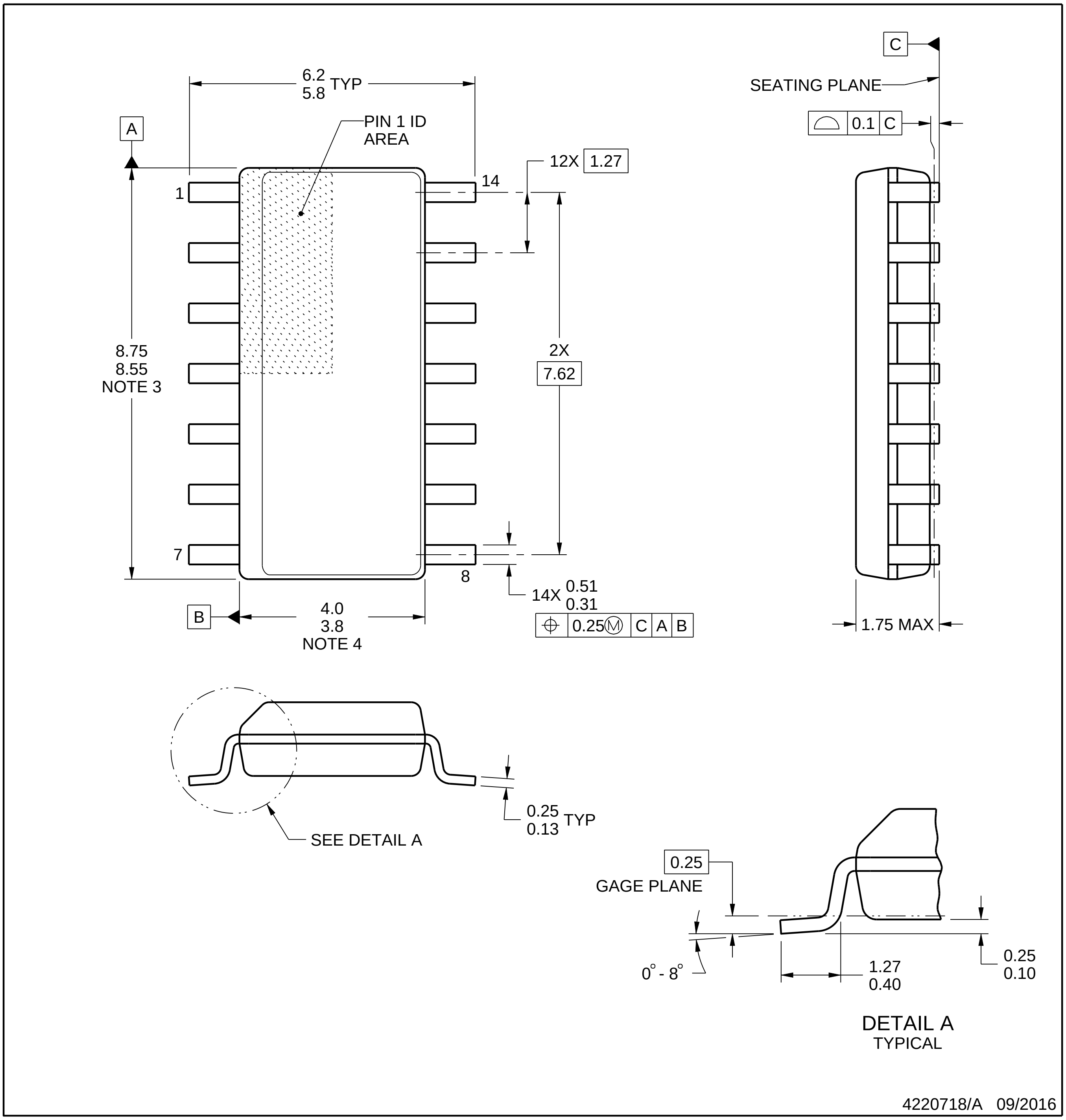
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

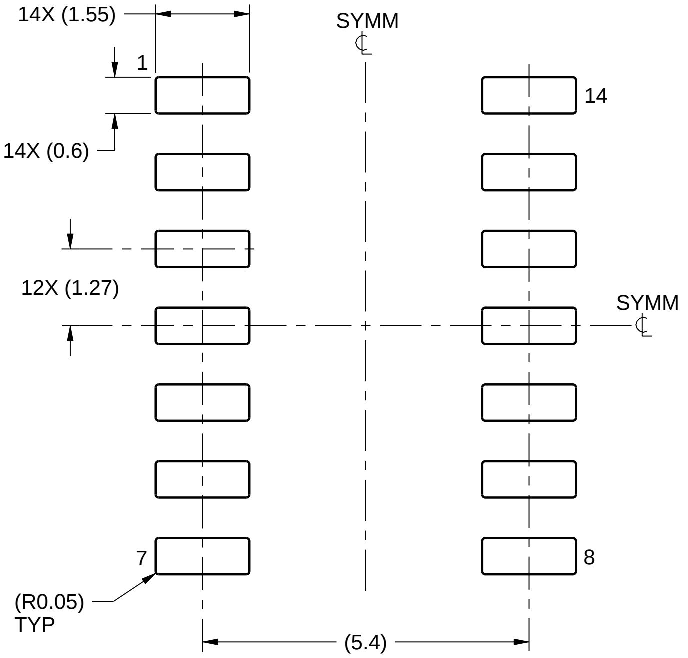
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

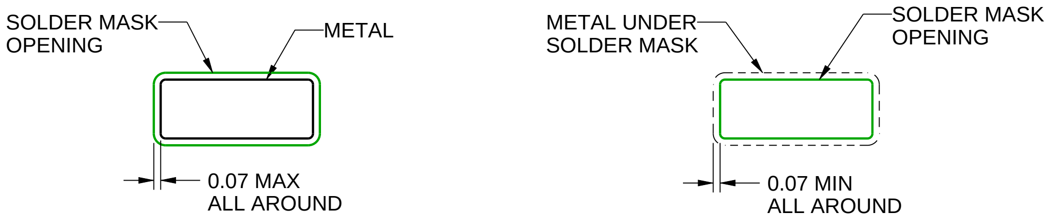


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



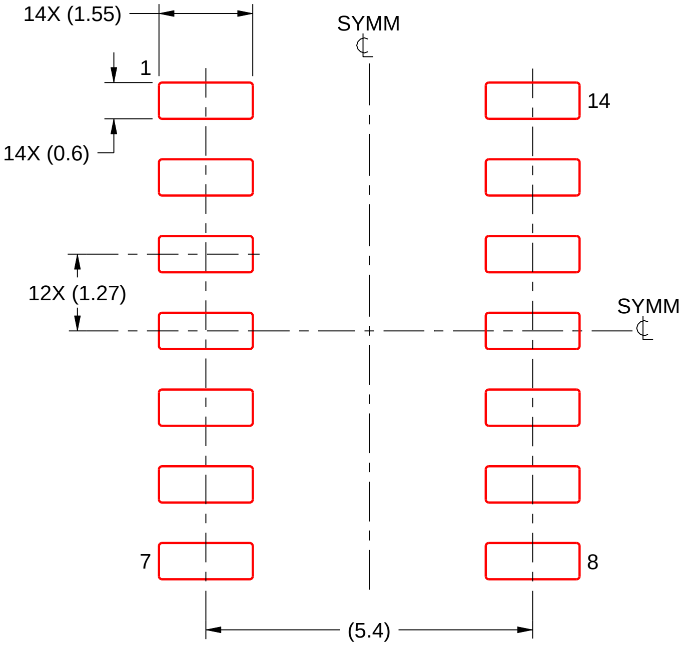
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

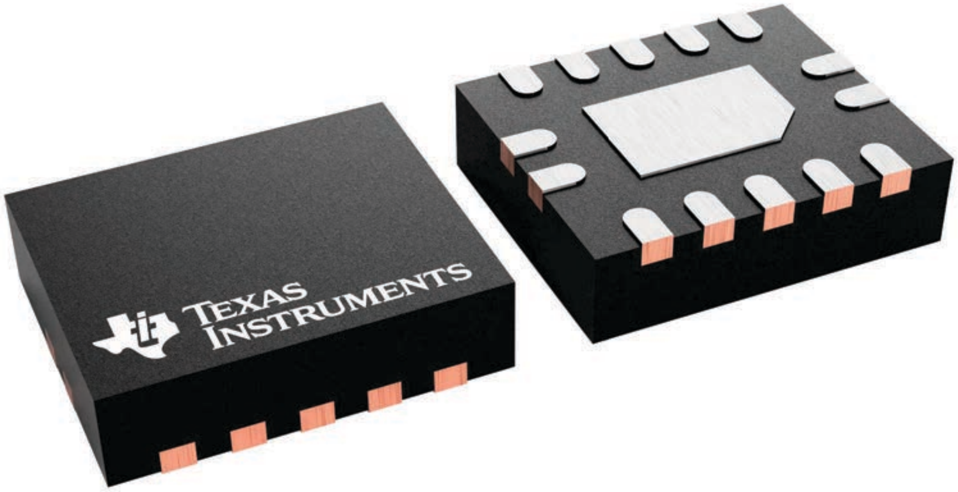
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

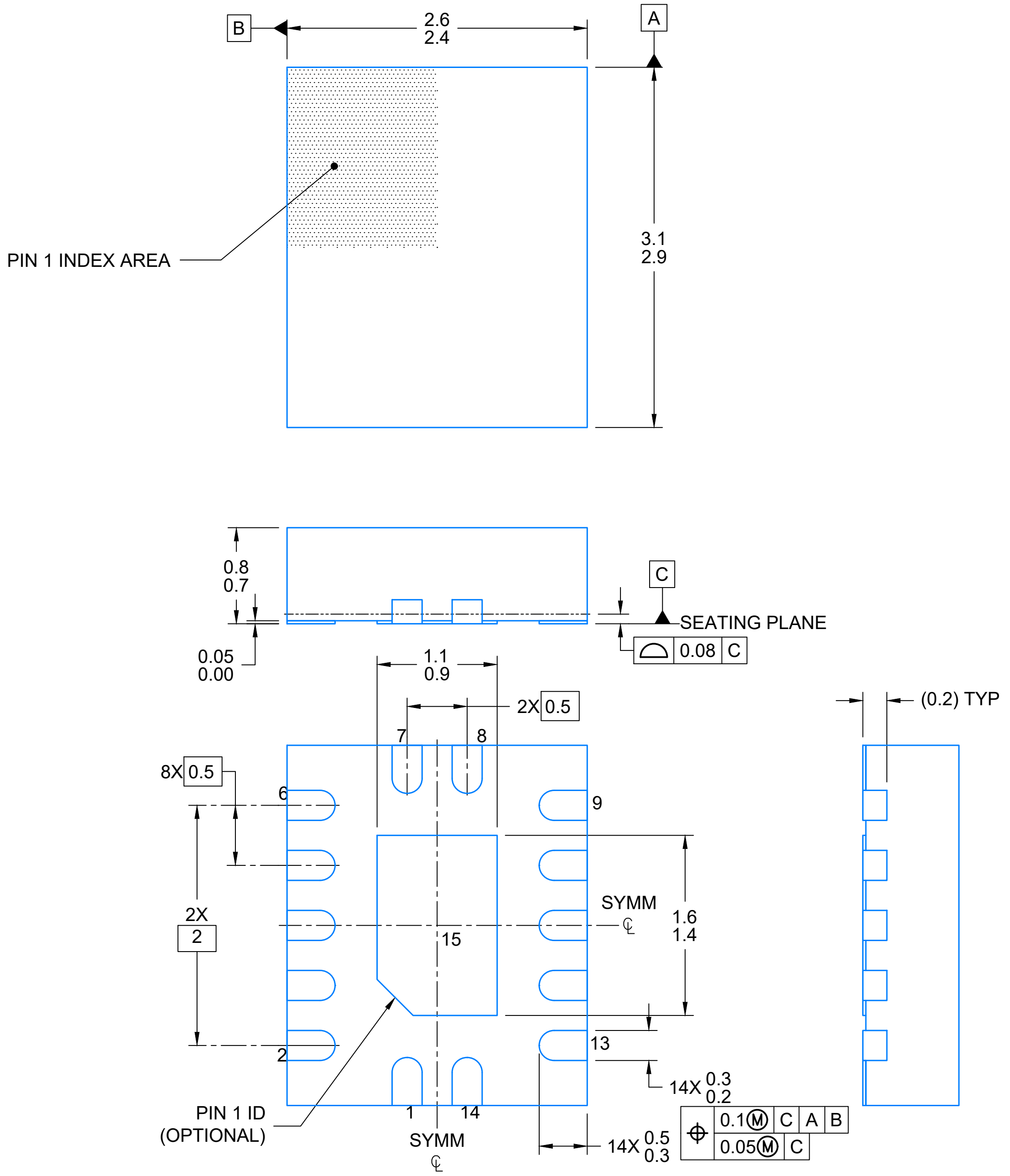


PACKAGE OUTLINE

BQA0014A

WQFN - 0.8 mm max height

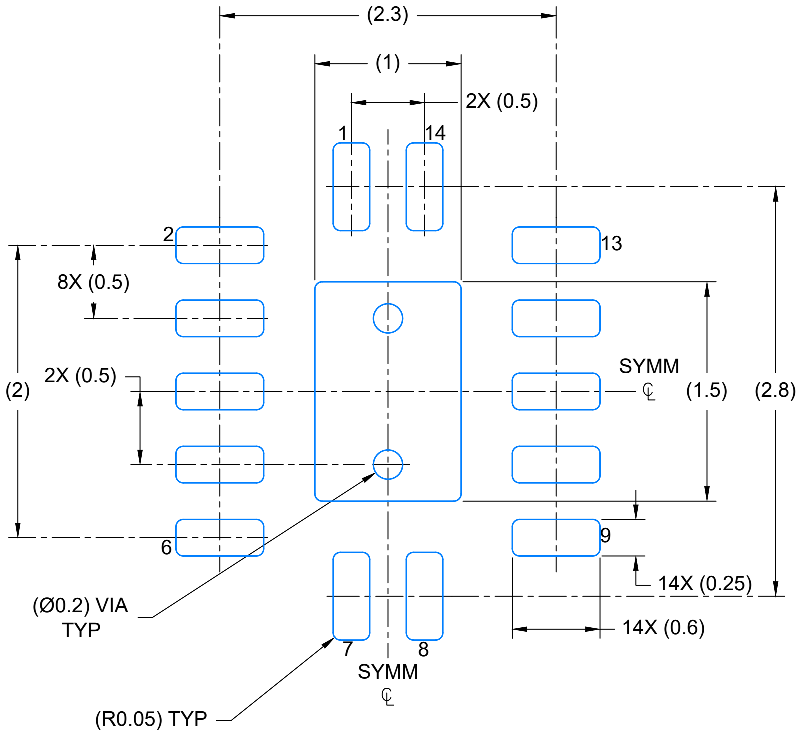
PLASTIC QUAD FLAT PACK-NO LEAD



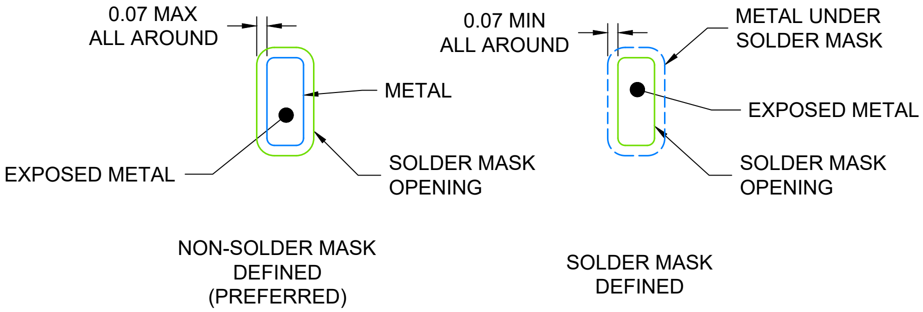
4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



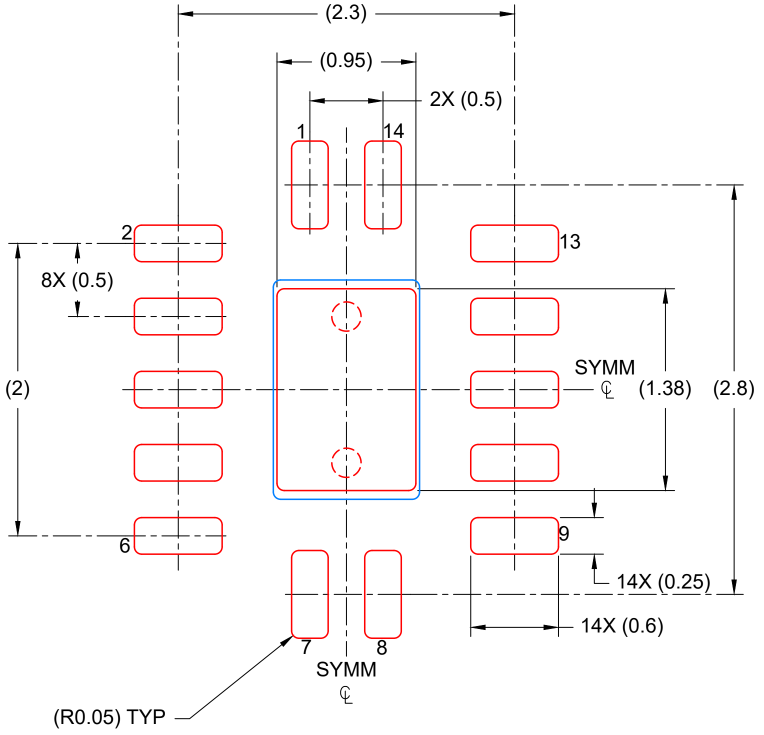
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

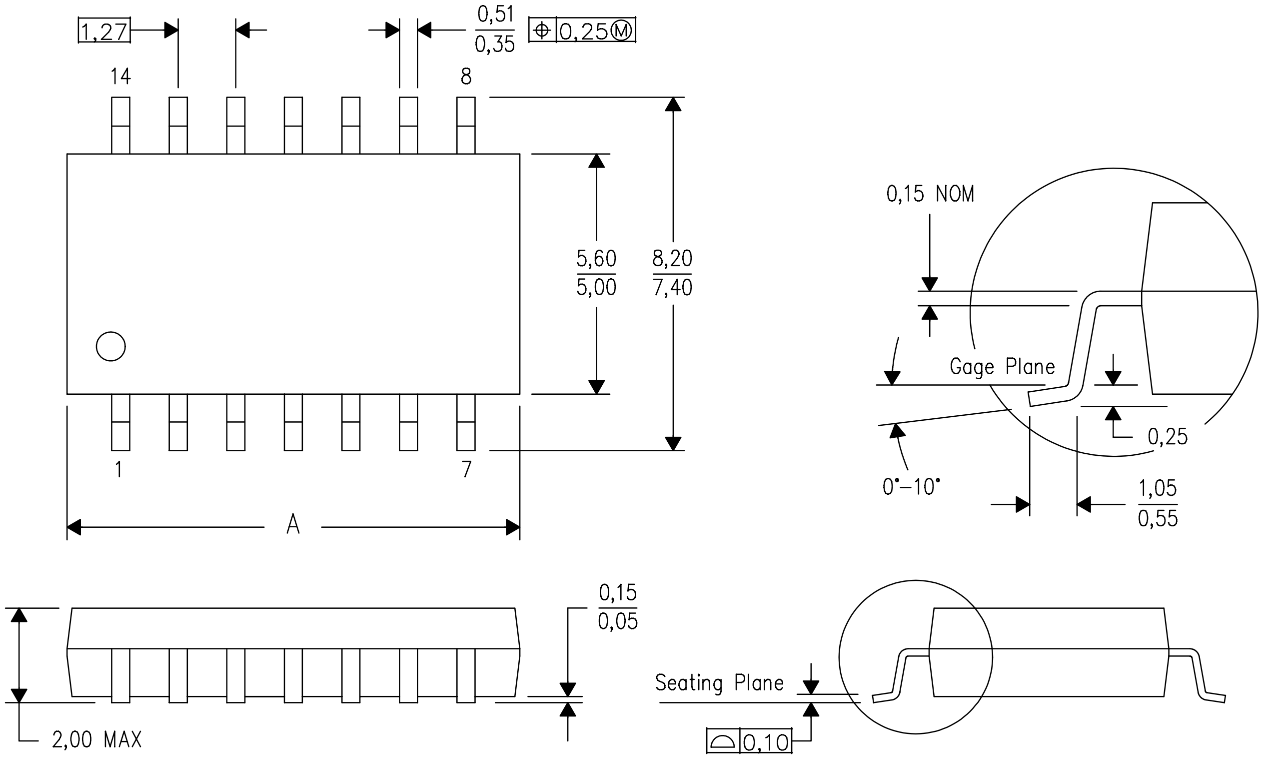
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Last updated 10/2025