- Q Devices Meet Automotive Performance Requirements
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

1A 1 14 V_{CC} 1Y 2 13 6A 2A 3 12 6Y 2Y 4 11 5A 3A 5 10 5Y 3Y 6 9 4A GND 7 8 4Y

description

The SN74AHC04Q contains six independent inverters. This device performs the Boolean function $Y = \overline{A}$.

ORDERING INFORMATION

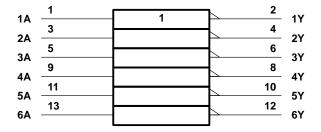
TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC - D	Tape and reel	SN74AHC04QDR	AHC04Q
-40 C to 125 C	TSSOP – PW	Tape and reel	SN74AHC04QPWR	HA04Q

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	\dots -0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
	V _{CC} = 2 V		1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage V _{CC} = 3 V			0.9	V
		V _{CC} = 5.5 V		1.65	
٧ _I	Input voltage	-	0	5.5	V
۷o	Output voltage		0	Vcc	V
		V _{CC} = 2 V		-50	μΑ
loh	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	A
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA
		V _{CC} = 2 V		50	μΑ
loL	Low-level output current $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			4	A
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		8	mA
A+/A>.	land transition rise or fell rate	V _{CC} = 3.3 V ± 0.3 V		100	20/1
Δt/Δv	Input transition rise or fall rate $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			20	ns/V
T _A	Operating free-air temperature	•	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T,	4 = 25°C	;	MIN	MAV	UNIT
PARAMETER	TEST CONDITIONS	Vcc -		TYP	MAX	IVIIIN	MAX	UNII
		2 V	1.9	2		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1		0.1	
V _{OL}		4.5 V			0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.5	
	I _{OL} = 8 mA	4.5 V			0.36		0.5	
lį	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μΑ
Ci	$V_I = V_{CC}$ or GND	5 V		2	10			pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
PARAMETER		(OUTPUT)		MIN	TYP	MAX	IVIIIN	IVIAA	ONII
^t PLH	۸	Y	C _L = 15 pF		5	8.9	1	10.5	ne
^t PHL	Α				5	8.9	1	10.5	ns
^t PLH	۸	Y	C _L = 50 pF		7.5	11.4	1	13	no
^t PHL	А				7.5	11.4	1	13	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	LOAD	T _A = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)		CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	ONII
^t PLH	۸	Y	C _L = 15 pF		3.8	5.5	1	6.5	20
t _{PHL}	А				3.8	5.5	1	6.5	ns
^t PLH	۸	V	C: 50 pF		5.3	7.5	1	8.5	no
t _{PHL}	А	Y	$C_L = 50 \text{ pF}$		5.3	7.5	1	8.5	ns

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic VOL		0.4		V
V _{OL(V)}	Quiet output, minimum dynamic VOL		-0.4		V
V _{OH(V)}	Quiet output, minimum dynamic VOH		4.8		V
VIH(D)	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

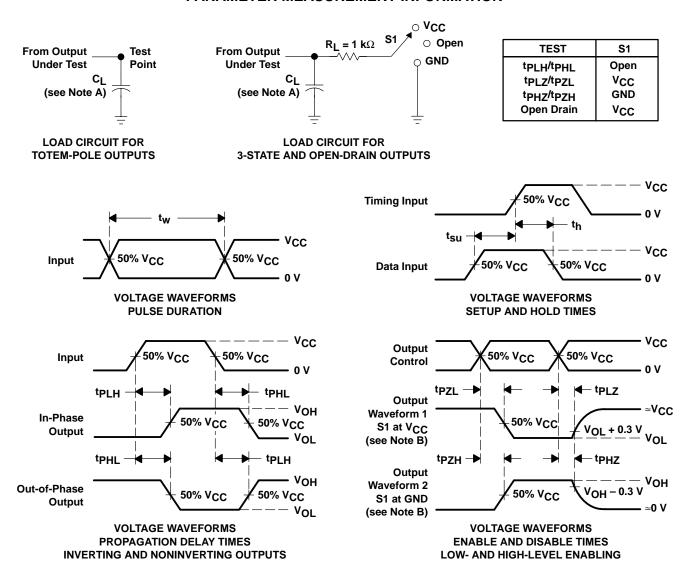
NOTE 4: Characteristics are for surface-mount packages only.



operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74AHC04QDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q
SN74AHC04QDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

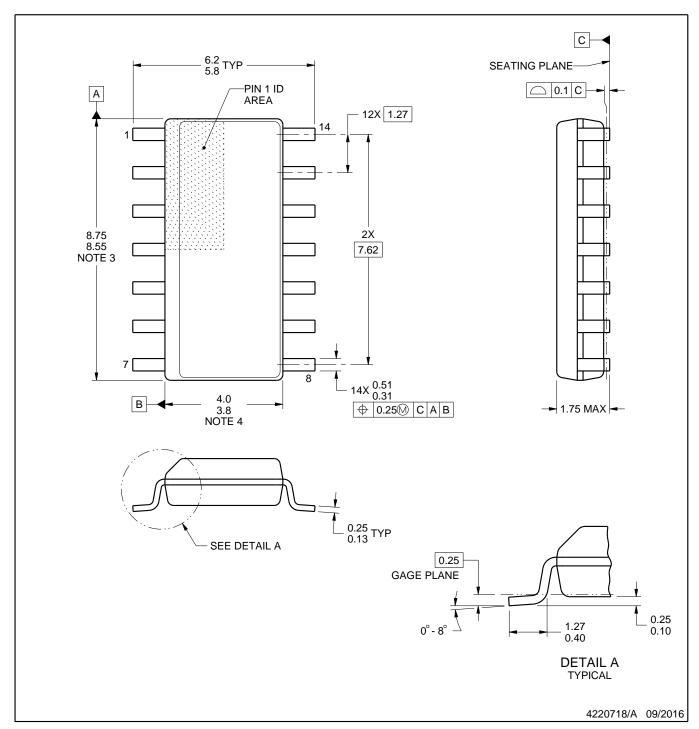
⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

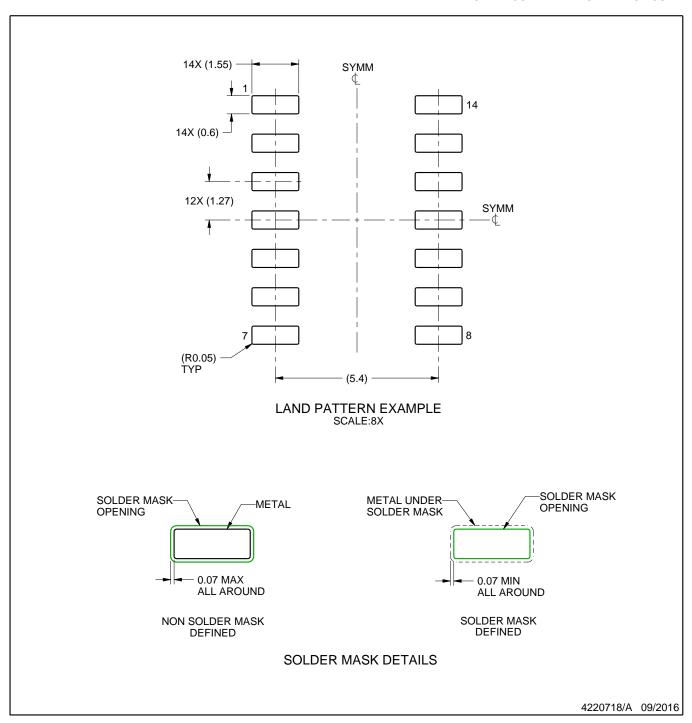
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



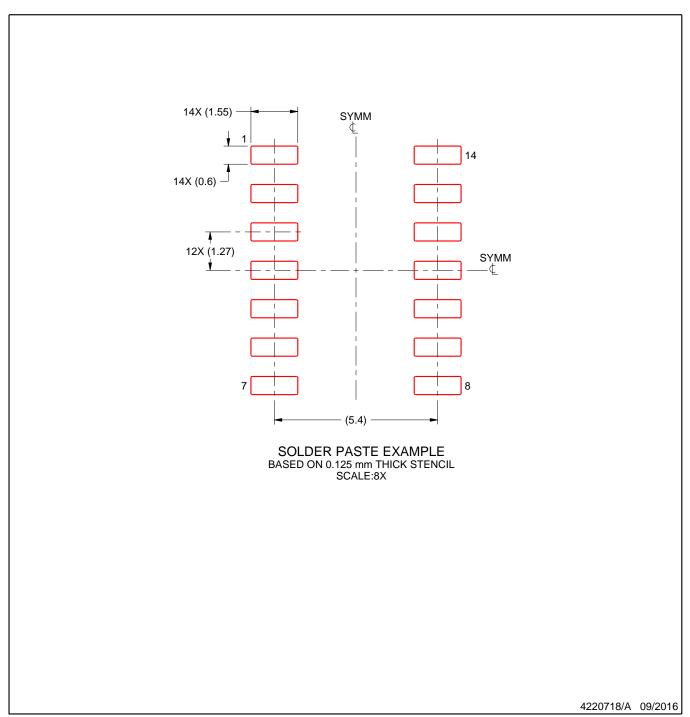
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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