







SN74AHC04-Q1

SCLS536D - AUGUST 2003 - REVISED JUNE 2023

SN74AHC04-Q1 Automotive Hex Inverter

1 Features

- Qualified for automotive applications
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Operating range of 2-V to 5.5-V V $_{\rm CC}$

2 Applications

- Synchronize inverted clock inputs
- Debounce a switch
- Invert a digital signal

3 Description

The SN74AHC04 contains six independent inverters. This device performs the Boolean function $Y = \overline{A}$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ²					
	D (SOIC, 14)	8.65 mm × 6 mm					
SN74AHC04-Q1	PW (TSSOP, 14)	5 mm × 6.4 mm					
	BQA (WQFN, 14)	3 mm × 2.5 mm					

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.





Table of Contents

1 Features1	8 Detailed Description
2 Applications1	8.1 Functional Block Diagram
3 Description1	8.2 Device Functional Modes
4 Revision History2	9 Application and Implementation
5 Pin Configuration and Functions3	9.1 Power Supply Recommendations
6 Specifications4	9.2 Layout9
6.1 Absolute Maximum Ratings4	10 Device and Documentation Support10
6.2 ESD Ratings4	10.1 Document Support (Analog)
6.3 Recommended Operating Conditions4	10.2 Receiving Notification of Documentation Updates 10
6.4 Thermal Information5	10.3 Support Resources10
6.5 Electrical Characteristics5	10.4 Trademarks10
6.6 Switching Characteristics, V _{CC} = 3.3 V ± 0.3 V5	10.5 Electrostatic Discharge Caution10
6.7 Switching Characteristics, V _{CC} = 5 V ± 0.5 V5	10.6 Glossary10
6.8 Noise Characteristics6	11 Mechanical, Packaging, and Orderable
6.9 Operating Characteristics6	Information10
7 Parameter Measurement Information7	

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cha	anges from Revision C (April 2023) to Revision D (June 2023)	Page
• A	Added BQA package to Package Information table	1
	Jpdated thermal values for PW package from RθJA = 113 to 147.7, all values in °C/W Added thermal value for RθJA: BQA = 88.3, all values in °C/W	
	anges from Revision B (April 2008) to Revision C (April 2023)	Page
• A	Added Applications, Package Information table, Pin Functions table, ESD Ratings table, Thermal table, Device Functional Modes, Application and Implementation section, Power Supply Recommissection, Layout section, Device and Documentation Support section, and Mechanical, Packaging Orderable Information section.	Information nendations , and



5 Pin Configuration and Functions

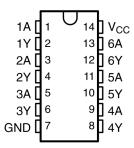


Figure 5-1. D or PW Package (Top View)

Table 5-1. Pin Functions

1	PIN	I/O	DESCRIPTION
NAME	NO.	_	DESCRIPTION
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	_	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V _{CC}	14	_	Positive Supply
Thermal Pad	1	_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

1. BQA Package only.



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)1

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I ²	Input voltage range		-0.5	7	V
V _O ²	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)		-20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM) ¹	±1500	V

⁽¹⁾ AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)¹

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		
		V _{CC} = 2 V		0.5	
V _{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V
		V _{CC} = 5.5 V		1.65	
V _I	Input voltage	·	0	5.5	V
Vo	Output voltage		0	V _{CC}	V
	High-level output current	V _{CC} = 2 V		-50	μA
I _{OH}		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	m A
		V _{CC} = 5 V ± 0.5 V		-8	mA
		V _{CC} = 2 V		50	μA
I _{OL}	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		V _{CC} = 5 V ± 0.5 V		8	IIIA
Λ+/Λ	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	no/\/
Δt/Δv	Input transition rise or fall rate	V _{CC} = 5 V ± 0.5 V		20	ns/V
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Submit Document Feedback



6.4 Thermal Information

		S	SN74AHC04-Q1			
THERMAL METRIC(1)		D (SOIC)	D (SOIC) PW BQA (WQFN)		UNIT	
		14 PINS		14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	147.7	88.3	°C/W	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			= 25°C		MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	IVIIIN	IVIAA	UNII
V _{OH}		2 V	1.9	2		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		
1 8- = HOI	I _{OH} = −8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1		0.1	
V _{OL}		4.5 V			0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.5	
	I _{OL} = 8 mA	4.5 V			0.36		0.5	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
Ci	V _I = V _{CC} or GND	5 V		2	10			pF

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	TO (OUTPUT)	LOAD CAPACITANCE	T _A	= 25°C		MIN	MAX	UNIT	
PARAMETER	(INPUT)	10 (001701)	LOAD CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	OIVII	
t _{PLH}	Δ.	V	C = 15 pE		5	8.9	1	10.5		
t _{PHL}	A	Ť	τ C _L = 15 pF	C _L = 15 pF		5	8.9	1	10.5	ns
t _{PLH}	Δ.	V	C = 50 pE		7.5	11.4	1	13		
t _{PHL}	A	Y	$C_L = 50 \text{ pF}$		7.5	11.4	1	13	ns	

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	LOAD CAPACITANCE	T _A = 25°C		MIN	MAX	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	UNII	
t _{PLH}	^	V	C ₁ = 15 pF		3.8	5.5	1	6.5	nc	
t _{PHL}		T	OL - 13 pr	υ ΟΕ - 13 μι		3.8	5.5	1	6.5	ns
t _{PLH}	۸	V	C = 50 pF		5.3	7.5	1	8.5	no	
t _{PHL}	А	Y	C _L = 50 pF		5.3	7.5	1	8.5	ns	



6.8 Noise Characteristics

 $V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}^1$

	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.4		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.4		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.8		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

6.9 Operating Characteristics

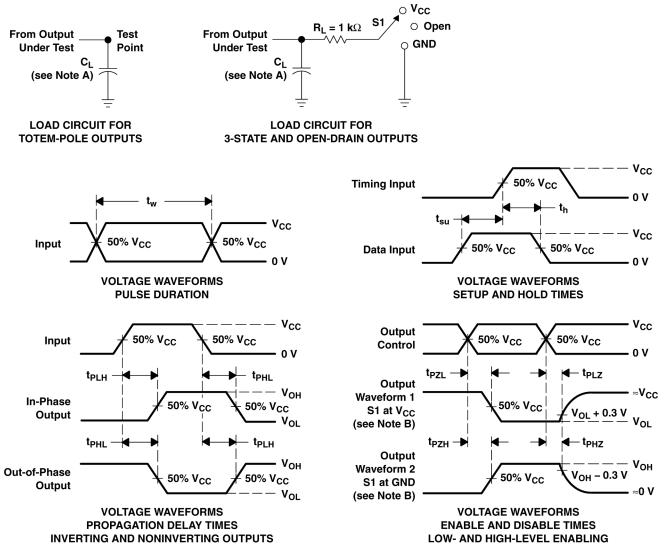
 V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

Submit Document Feedback



7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns. $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{CC}
t _{PHZ} /t _{PZH}	GND
Open Drain	V _{CC}



8 Detailed Description

8.1 Functional Block Diagram



Figure 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.2 Device Functional Modes

Table 8-1. Function Table (Each Inverter)

INPUT	OUTPUT
Α	Y
Н	L
L	Н

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Layout Diagram are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{\rm CC}$; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

9.2.1.1 Layout Example

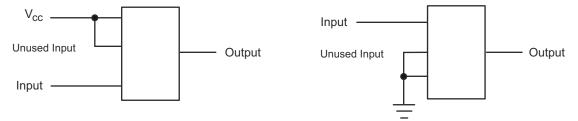


Figure 9-1. Layout Diagram

10 Device and Documentation Support

10.1 Document Support (Analog)

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN74AHC04-Q1	Click here	Click here	Click here	Click here	Click here	

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Submit Document Feedback

www.ti.com 23-May-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74AHC04QDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q1
SN74AHC04QWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q
SN74AHC04QWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC04Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

www.ti.com 23-May-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC04-Q1:

● Enhanced Product : SN74AHC04-EP

Military: SN54AHC04

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

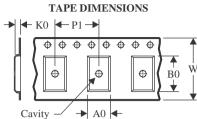
• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





	•
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

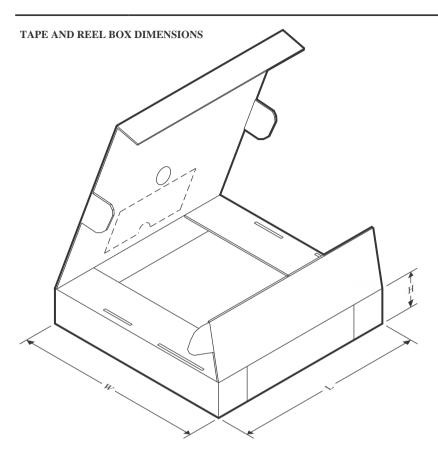


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC04QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC04QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

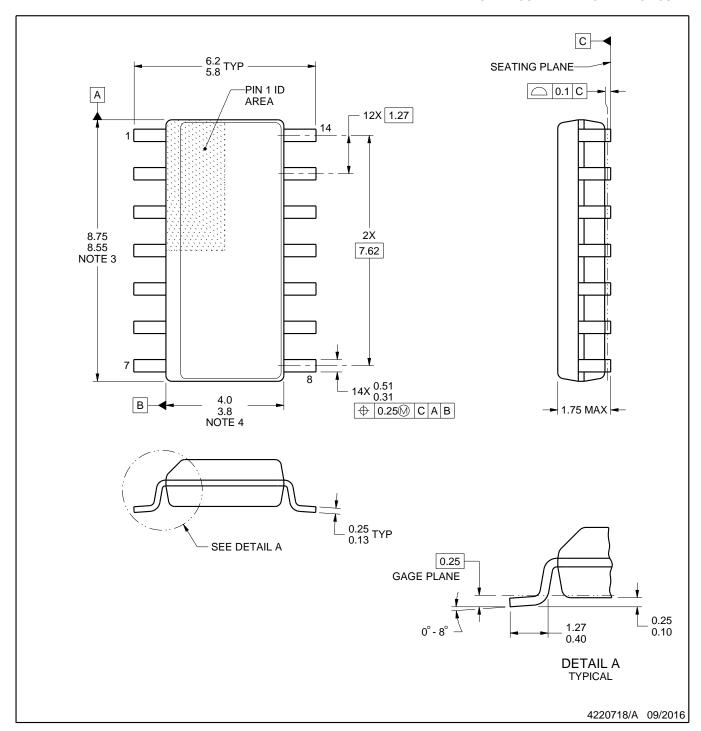


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC04QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC04QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

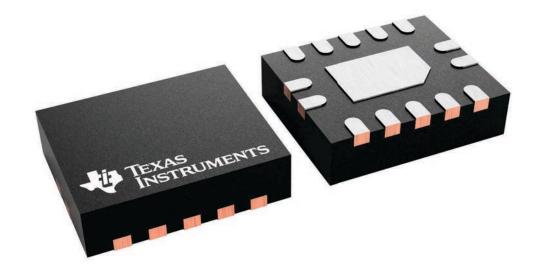
- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

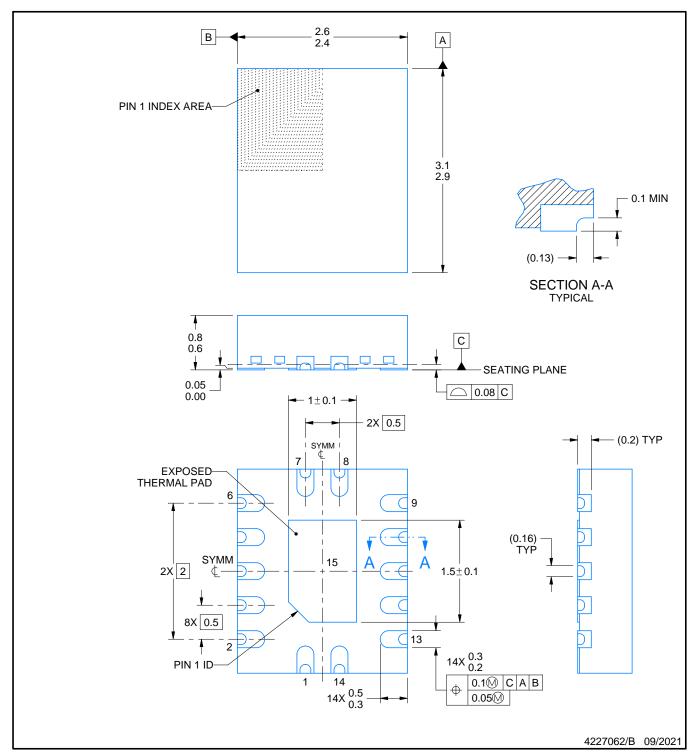
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD

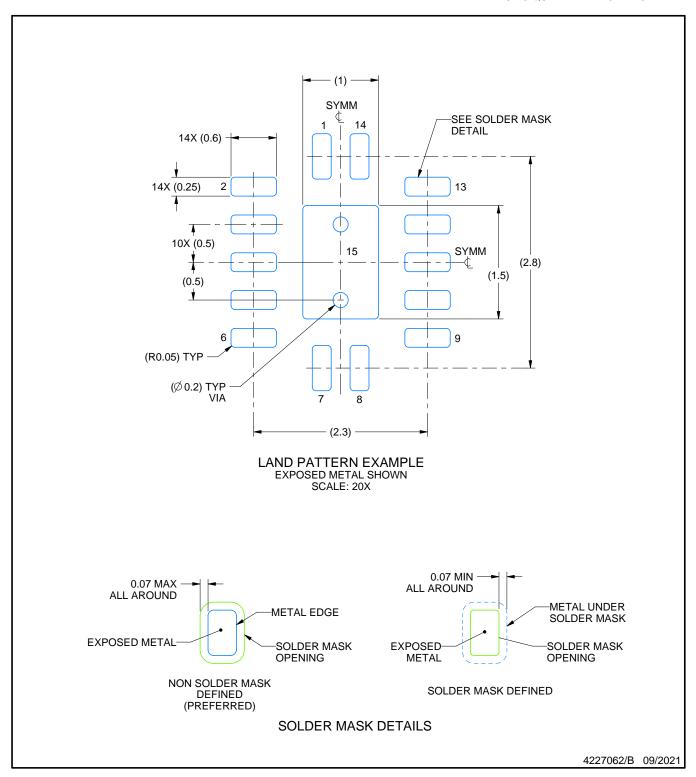


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

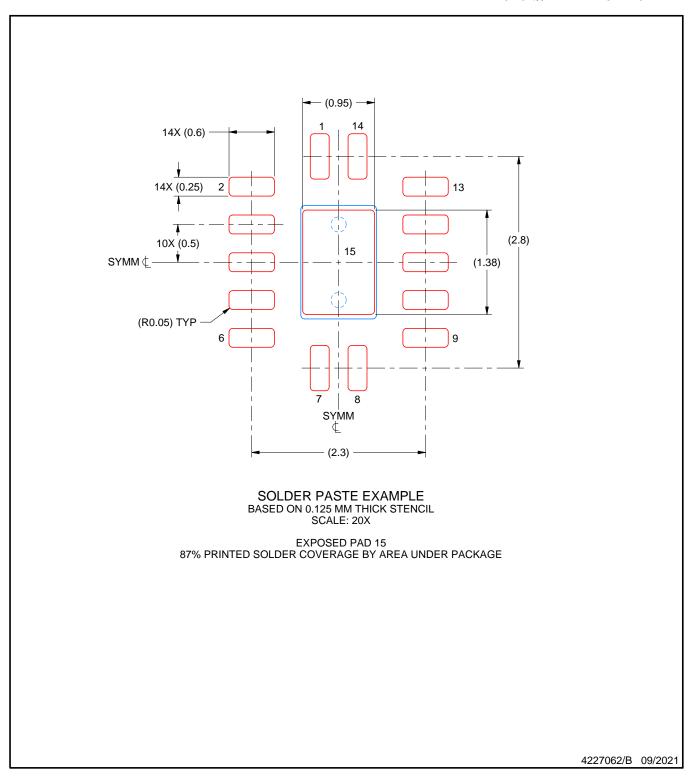


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025. Texas Instruments Incorporated