

SNx4ACT86 Quadruple 2-Input Exclusive-OR Gates

1 Features

- 4.5V to 5.5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Max t_{pd} of 10ns at 5V
- Inputs are TTL-voltage compatible

2 Description

The 'ACT86 devices are quadruple 2-input exclusive-OR gates. The devices perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

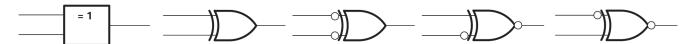
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
SNx4ACT86	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35 mm
SINAACTOO	NS (SO, 14)	10.2mm × 7.8mm	10.3mm × 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	BQA (WQFN)	3mm × 2.5mm	3mm × 2.5mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.

EXCLUSIVE-OR



Exclusive-OR Logic



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3 Pin Configuration and Functions

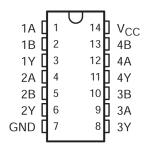


Figure 3-1. SN54ACT86 J or W Package; SN74ACT86 D, DB, N, NS, or PW Package (Top View)

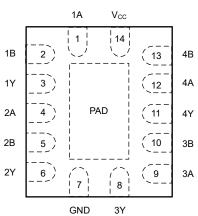
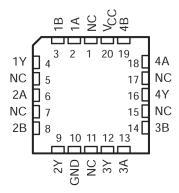


Figure 3-2. SN74ACT86 BQA Package (Transparent Top View)



NC - No internal connection

Figure 3-3. SN54ACT86 FK Package (Top View)

Table 3-1. Pin Functions

	PIN			
NAME	BQA, D, DB, N, NS, PW, J, or W	FK	Type ⁽¹⁾	DESCRIPTION
1A	1	2	I	Channel 1, Input A
1B	2	3	I	Channel 1, Input B
1Y	3	4	0	Channel 1, Output Y
2A	4	6	I	Channel 2, Input A
2B	5	8	I	Channel 2, Input B
2Y	6	9	0	Channel 2, Output Y
GND	7	10	G	Ground
3Y	8	12	0	Channel 3, Output Y
3A	9	13	I	Channel 3, Input A
3B	10	14	I	Channel 3, Input B
4Y	11	16	0	Channel 4, Output Y
4A	12	18	I	Channel 4, Input A
4B	13	19	I	Channel 4, Input B
V _{CC}	14	20	Р	Positive Supply



Table 3-1. Pin Functions (continued)

	PIN						
NAME	BQA, D, DB, N, NS, PW, J, or W	FK	Type ⁽¹⁾	DESCRIPTION			
NC	_	1, 5, 7, 11, 15, 17	_	Not internally connected			
Thermal Pac	I (2)		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply			

Signal Types: I = input, O = output, G = ground, P = power. BQA Package only. (1) (2)



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	Supply voltage range			
V _I ⁽²⁾	Input voltage range		-0.5	V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$(V_l < 0 \text{ or } V_l > V_{CC})$		±20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V _O = 0 to V _{CC})		±50	mA
	Continuous current through V _{CC} or GND	·		±200	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54ACT8	6	SN74ACT8	6	LINUT	
		MIN	MAX	MIN	MAX	UNIT	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V	
V _{IH}	High-level input voltage	2		2		V	
V _{IL}	Low-level input voltage		0.8		8.0	V	
VI	Input voltage	0	V _{CC}	0	V _{CC}	V	
Vo	Output voltage	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current		-24		-24	mA	
I _{OL}	Low-level output current		24		24	mA	
Δt/Δν	Input transition rise or fall rate		8		8	ns/V	
T _A	Operating free-air temperature	-55	125	-40	85	°C	

All unused inputs of the device must be held at V_{CC} or GND to verify proper device operation. Refer to Implications of Slow or Floating CMOS Inputs, application note.

4.3 Thermal Information

			SN74ACT86							
	THERMAL METRIC(1)	BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT		
					14 PINS					
R _{θJA}	Junction-to-ambient thermal resistance	91.3	119.9	96	80	76	145.7	°C/W		
R _{θJC(top)}	Junction-to-case (top) thermal resistance	99.4	_	_	_	_	_	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	60.0	_	_	_	_	_	°C/W		
ΨЈТ	Junction-to-top characterization parameter	14.5	_	_	_	_	_	°C/W		
ΨЈВ	Junction-to-board characterization parameter	60.8	_	_	_	_	_	°C/W		

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



		SN74ACT86						
	THERMAL METRIC(1)	BQA (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT
					14 PINS			
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	37.0	_	_	_	_	_	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CC	NDITIONS	V	Т	_A = 25 °C		SN54A	CT86	SN74A	CT86	UNIT
PARAMETER	TEST CC	MDITIONS	V _{cc}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	I - 50uA		4.5V	4.4	4.49		4.4		4.4		
	$I_{OH} = -50\mu A$		5.5V	5.4	5.49		5.4		5.4		
V	1 - 24mA		4.5V	3.86			3.7		3.76		V
V _{OH}	I _{OH} = -24mA		5.5V	4.86			4.7		4.76		v
	I _{OH} = -50mA ⁽¹⁾		5.5V				3.85				
	$I_{OH} = -75 \text{mA}^{(1)}$		5.5V						3.85		
	I - 50A		4.5V		0.001	0.1		0.1		0.1	
	$I_{OL} = 50\mu A$	5.5V		0.001	0.1		0.1		0.1		
V	1 = 24mA		4.5V			0.36		0.5		0.44	
V _{OL}	$I_{OL} = 24mA$		5.5V			0.36		0.5		0.44	V
	I _{OL} = 50mA ⁽¹⁾		5.5V					1.65	,		
	I _{OL} = 75mA ⁽¹⁾		5.5V							1.65	
I _I	V _I = V _{CC} or GND	1	5.5V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	5.5V			4		80		40	μΑ
ΔI _{CC} (2)	One input at 3.4 GND or V _{cc}	V, Other inputs at	5.5V		0.6			1.6		1.5	mA
C _i	$V_I = V_{CC}$ or GND	1	5V		2.6						pF

⁽¹⁾ Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.

4.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T,	_A = 25°C	;	SN54A	CT86	SN74AC	CT86	UNIT
PARAMETER	PROW (NAPOT)	10 (001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	V	1.5	8.5	9.5	1	10	1	10	ns
t _{PHL}	7010	1	1.5	7	9.5	1	10.5	1	10.5	115

4.6 Operating Characteristics

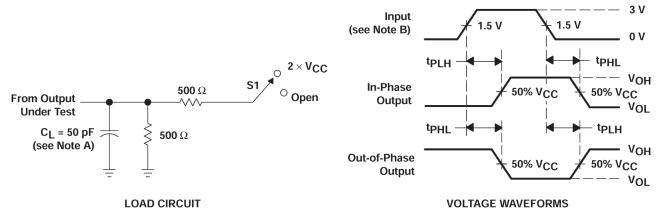
 V_{CC} = 5V, T_A = 25°C

	PARAMETER	TES	T CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C _L = 50pF	f = 1MHz	25	pF

⁽²⁾ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or V_{CC}.



5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_r v 2.5ns, t_f v 2.5ns.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S 1
t _{PLH} /t _{PHL}	Open



6 Detailed Description

6.1 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



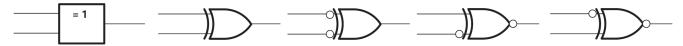
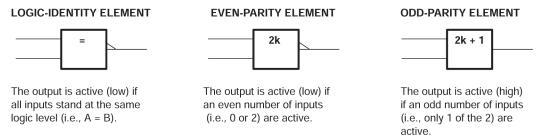


Figure 6-1. Exclusive-OR Logic

These five equivalent exclusive-OR symbols are valid for an 'ACT86 gate in positive logic; negation may be shown at any two ports.



6.2 Device Functional Modes

Table 6-1. Function Table (Each Gate)

INP	UTS	OUTPUT Y
Α	В	OUIPULT
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in Figure 7-1.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example

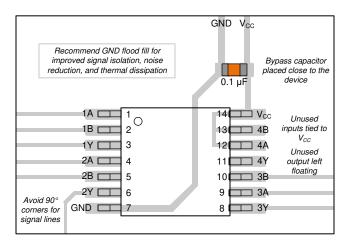


Figure 7-1. Example Layout for the SN74ACT86

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER SAMPLE & BLIY		TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN54ACT86	Click here	Click here	Click here	Click here	Click here	
SN74ACT86	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	changes from Revision D (July 2024) to Revision E (April 2025)	Page
•	Added BQA Package	3
•	Added BQA thermal information	5
_		

Changes from Revision C (October 2003) to Revision D (July 2024)

Page

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material MSL rating/ Peak reflow (4) (5)		Op temp (°C)	Part marking (6)
5962-9068701Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9068701Q2A SNJ54ACT 86FK
5962-9068701QCA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QC A SNJ54ACT86J
5962-9068701QDA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QD A SNJ54ACT86W
SN74ACT86BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	ACT86
SN74ACT86DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86DRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86DRG4.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT86N
SN74ACT86N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT86N
SN74ACT86NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT86
SN74ACT86PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	AD86
SN74ACT86PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SN74ACT86PWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD86
SNJ54ACT86FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9068701Q2A SNJ54ACT 86FK



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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54ACT86FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9068701Q2A SNJ54ACT 86FK
SNJ54ACT86J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QC A SNJ54ACT86J
SNJ54ACT86J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QC A SNJ54ACT86J
SNJ54ACT86W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QD A SNJ54ACT86W
SNJ54ACT86W.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9068701QD A SNJ54ACT86W

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT86, SN74ACT86:

Catalog: SN74ACT86

Automotive: SN74ACT86-Q1, SN74ACT86-Q1

Military: SN54ACT86

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74ACT86DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT86NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74ACT86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT86PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74ACT86DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74ACT86NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74ACT86PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT86PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9068701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9068701QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT86N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT86FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT86FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT86W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54ACT86W.A	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



www.ti.com

PLASTIC QUAD FLAT PACK-NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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