









SN74ACT8541 SCAS974 - MARCH 2024

SN74ACT8541 Octal Buffers With 3-State Outputs And Schmitt-Trigger Inputs

1 Features

- Operating voltage range of 4.5V to 5.5V
- TTL-compatible Schmitt-trigger inputs support slow and noisy input signals
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 9.6ns max ($V_{CC} = 5V$, $C_1 = 50pF$

2 Applications

- Drive an indicator LED
- Level-shift using open-drain outputs
- Control a relay

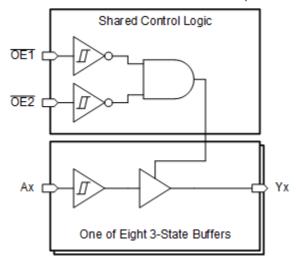
3 Description

The SN74ACT8541 contains eight independent buffers with 3-state outputs and Schmitt-trigger inputs. All channels can be simultaneously forced into the high-impedance state using either of the output enable inputs ($\overline{OE1}$ or $\overline{OE2}$).

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm
SN74ACT8541	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3mm

- For more information, see Section 10. (1)
- The package size (length × width) is a nominal value and includes pins, where applicable
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	7.1 Application Information	9
2 Applications		7.2 Typical Application	
3 Description		7.3 Design Requirements	
4 Pin Configuration and Functions	3	7.4 Detailed Design Procedure	
5 Specifications	4	7.5 Application Curves	
5.1 Absolute Maximum Ratings	4	7.6 Power Supply Recommendations	
5.2 ESD Ratings	4	7.7 Layout	. 11
5.3 Recommended Operating Conditions	4	8 Device and Documentation Support	
5.4 Thermal Information	4	8.1 Documentation Support	. 12
5.5 Electrical Characteristics	<mark>5</mark>	8.2 Receiving Notification of Documentation Updates	12
5.6 Switching Characteristics	6	8.3 Support Resources	. 12
5.7 Typical Characteristics	6	8.4 Trademarks	. 12
6 Detailed Description	7	8.5 Electrostatic Discharge Caution	12
6.1 Overview		8.6 Glossary	12
6.2 Functional Block Diagram	7	9 Revision History	. 12
6.3 Feature Description	7	10 Mechanical, Packaging, and Orderable	
6.4 Device Functional Modes	8	Information	. 12
7 Application and Implementation	9		

4 Pin Configuration and Functions

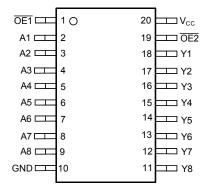


Figure 4-1. PW and DGS Package, 20-Pin TSSOP and VSSOP (Top View)

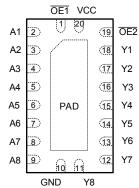


Figure 4-2. RKS Package, 20-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		- TYPE ⁽¹⁾	DESCRIPTION	
NAME	NO.	IYPE(')	DESCRIPTION	
OE1	1	ı	Output enable input 1, active low	
A1	2	ı	Input for channel 1	
A2	3	ı	Input for channel 2	
A3	4	I	Input for channel 3	
A4	5	I	Input for channel 4	
A5	6	I	Input for channel 5	
A6	7	ı	Input for channel 6	
A7	8	ı	Input for channel 7	
A8	9	I	Input for channel 8	
GND	10	G	Ground	
Y8	11	0	Output for channel 8	
Y7	12	0	Output for channel 7	
Y6	13	0	Output for channel 6	
Y5	14	0	Output for channel 5	
Y4	15	0	Output for channel 4	
Y3	16	0	Output for channel 3	
Y2	17	0	Output for channel 2	
Y1	18	0	Output for channel 1	
OE2	19	ı	Output enable input 2, active low	
V _{CC}	20	Р	Positive supply	
Thermal Pad ⁽	2)	_	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.	

⁽¹⁾ I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

⁽²⁾ RKS package only.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	V _{CC} + 0.5 V	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5 V	V
I _{IK}	Input clamp current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		±20	mA
I _{OK}	Output clamp current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$		±50	mA
Io	Continuous output current	V _O = 0 to V _{CC}		±50	mA
	Continuous output current through V _{CC} or GND			±200	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
Electrostatic	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000		
V _(ESD)	discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	V

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		4.5	5.5	V
V _I ⁽¹⁾	Input Voltage	Input Voltage		V _{CC}	V
Vo	Output Voltage	Output Voltage		V _{CC}	V
I _{OH}	High-level output current	4.5V ≤ V _{CC} ≤ 5.5V		-24	mA
I _{OL}	Low-level output current	4.5V ≤ V _{CC} ≤ 5.5V		24	mA
Δt/Δν	Input transition rise or fall rate	4.5V ≤ V _{CC} ≤ 5.5V		20	ns/V
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at a valid high or low voltage level to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating CMOS Inputs.

5.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	DGS (VSSOP)	PW (TSSOP)	RKS (VQFN)	UNIT
	THERWAL METRIC	20 PINS	20 PINS	20 PINS	ONII
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.5	126.2	67.7	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	62.1	68.7	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	77.3	40.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.8	22.3	10.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78	76.9	40.4	°C/W

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated



5.4 Thermal Information (continued)

THERMAL METRIC(1)		DGS (VSSOP)	PW (TSSOP)	RKS (VQFN)	UNIT
		20 PINS	20 PINS	20 PINS	ONII
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	24.1	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	V	TA	= 25°C		-40°C	to 125°C		UNIT
PARAMETER TES	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX	UNII
., Р		4.5V	1.2	1.5	1.9	1.2		1.9	V
V_{T+}	Positive-going input threshold voltage	5V	1.4		2	1.4		2	
	Voltago	5.5V	1.4	1.7	2.1	1.4		2.1	
		4.5V	0.5	0.9	1.2	0.5		1.2	
V _{T-}	Negative-going input threshold voltage	5V	0.8		1.3	0.8		1.3	V
	Voltage	5.5V	0.6	1	1.4	0.6		1.4	
		4.5V	0.4	0.6	1.4	0.4		1.4	
ΔV_{T}	Hysteresis (V _{T+} - V _{T-})	5V	0.4			0.4			V
		5.5V	0.4	0.6	1.5	0.4		1.5	
	I - 50A	4.5V	4.4	4.49		4.4			
	I _{OH} = -50μA	5.5V	5.4	5.49		5.4			V
	I _{OH} = -24mA	4.5V	3.94			3.7			
V _{OH}	I _{OH} = -24mA	5.5V	4.86			4.7			
	I _{OH} = -50mA	5.5V				3.85			
	I _{OH} = -75mA	5.5V				3.85			
	- FO A	4.5V		0.001	0.1	,		0.1	
	I _{OH} = 50μA	5.5V	,	0.001	0.1	,		0.1	
	I _{OH} = 24mA	4.5V			0.36			0.5	.,
V _{OL}	I _{OH} = 24mA	5.5V			0.36			0.5	V
	I _{OH} = 50mA	5.5V						1.65	
	I _{OH} = 75mA	5.5V						1.65	
I _I	V _I = 5.5V or GND	0V to 5.5V			±0.1			±1	μA
l _{oz}	V _O = V _{CC} or GND	5.5V			±0.25	,		±5	μA
I _{cc}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V			2			80	μA
ΔI _{CC}	$V_I = V_{CC} - 2.1V$; Any Input	4.5V to 5.5V		0.6	1.2			1.5	mA
Cı	V _I = V _{CC} or GND	5V		8					pF
Co	V _O = V _{CC} or GND	5V		14					pF
C _{PD} (2) (3)	C _I = 50pF, F = 1MHz	5V		19					pF

Typical value at nearest nominal voltage (1.8 V; 2.5 V; 3.3 V; 5 V)
 C_{PD} is used to determine the dynamic power consumption, per channel
 P_D= V_{CC} ²xF_IX(C_{PD}+ C_L) where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage



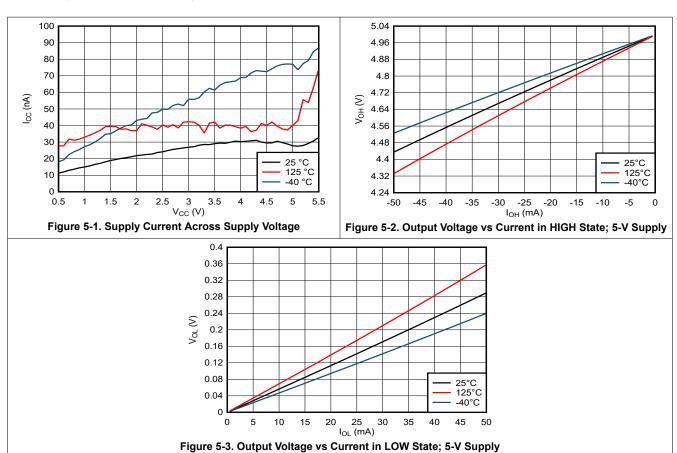
5.6 Switching Characteristics

 C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V	TA	= 25°C		-40°0	C to 125	°C	UNIT
PARAMETER	PROW (INPUT)	10 (001701)	V _{cc}	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	A	Υ	5V		4.2	5.8			7.1	ns
t _{PHL}	A	Υ	5V		5	8.1			9.6	ns
t _{PZH}	ŌĒ	Υ	5V		6.3	9.5			11.5	ns
t _{PZL}	ŌĒ	Υ	5V		6.5	10			11.9	ns
t _{PHZ}	ŌĒ	Υ	5V		5.3	6.8			7.8	ns
t _{PLZ}	ŌĒ	Υ	5V		3.8	5.2			6.3	ns

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)



Submit Document Feedback

www.ti.com

6 Detailed Description

6.1 Overview

The SN74ACT8541 contains eight buffers with 3-state outputs. The active low output enable pins (OE1 and OE2) control all eight channels, and are configured so that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driven low or high.

When the outputs are disabled, the outputs are set into the high-impedance state.

6.2 Functional Block Diagram

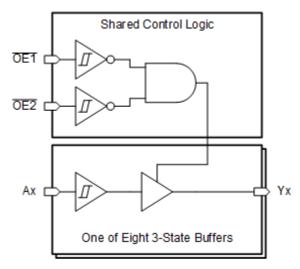


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Feature Description

6.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term balanced indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the Electrical Characteristics table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a $10k\Omega$ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

6.3.2 TTL-Compatible Schmitt-Trigger CMOS Inputs

This device includes TTL-compatible CMOS inputs with Schmitt-trigger architecture. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage thresholds.

TTL-compatible Schmitt-trigger CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated



with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a $10k\Omega$ resistor is recommended and will typically meet all requirements.

6.3.3 Clamp Diode Structure

As shown in Figure 6-2, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

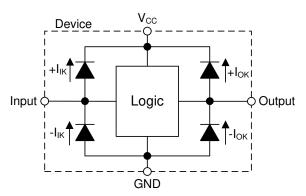


Figure 6-2. Electrical Placement of Clamping Diodes for Each Input and Output

6.4 Device Functional Modes

Table 6-1. Function Table

	OUTPUT ⁽²⁾		
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	Х	Х	Z
Х	Н	Х	Z

- (1) L = input low, H = input high, X = don't care
- (2) L = output low, H = output high, Z = high impedance

Submit Document Feedback

Copyright © 2024 Texas Instruments Incorporated

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The SN74ACT8541 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

7.2 Typical Application

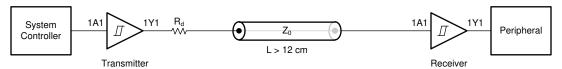


Figure 7-1. Typical Application Block Diagram

7.3 Design Requirements

7.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT8541 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT8541 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT8541 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT8541 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.



CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

7.3.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT8541 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A $10k\Omega$ resistor value is often used due to these factors.

Refer to the Feature Description section for additional information regarding the inputs for this device.

7.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

7.4 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the Layout section.
- 2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT8541 to one or more of the receiving devices.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

Product Folder Links: SN74ACT8541

7.5 Application Curves

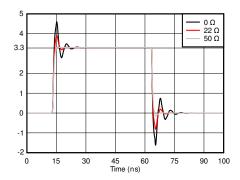


Figure 7-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

7.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.7 Layout

7.7.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.7.2 Layout Example

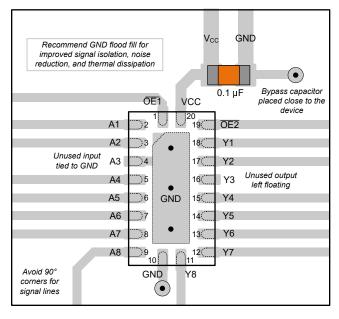


Figure 7-3. Example Layout for the SN74ACT8541 in the RKS Package



8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation
- Texas Instruments, Implications of Slow or Floating CMOS Inputs
- Texas Instruments, *Understanding Schmitt Triggers*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
March 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74ACT8541

www.ti.com 8-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74ACT8541DGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T8541
SN74ACT8541DGSR.A	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T8541
SN74ACT8541PWR	Active	Production	TSSOP (PW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD8541
SN74ACT8541PWR.A	Active	Production	TSSOP (PW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD8541
SN74ACT8541RKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT8541
SN74ACT8541RKSR.A	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT8541

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 8-Nov-2025

OTHER QUALIFIED VERSIONS OF SN74ACT8541:

Automotive: SN74ACT8541-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 7-Jul-2025

TAPE AND REEL INFORMATION





	•
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT8541DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74ACT8541PWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT8541RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

www.ti.com 7-Jul-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT8541DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74ACT8541PWR	TSSOP	PW	20	3000	353.0	353.0	32.0
SN74ACT8541RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
- 5. Features may differ or may not be present.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025