







SN54ACT573, SN74ACT573 SCAS538G - OCTOBER 1995 - REVISED MARCH 2024

# **SNx4ACT573 Octal D-Type Transparent Latches With 3-State Outputs**

#### 1 Features

- Operation of 4.5V to 5.5V V<sub>CC</sub>
- Inputs accept voltages to 5.5V
- Maximum t<sub>pd</sub> of 9.5ns at 5V
- Inputs are TTL-voltage compatible

## 2 Applications

- Parallel data storage
- Digital bus buffer

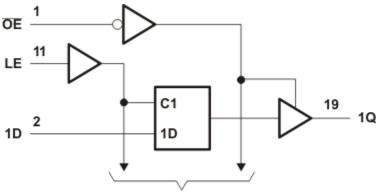
#### 3 Description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bus drivers, and working registers.

#### **Device Information**

PART NUMBER	RATING	PACKAGE <sup>(1)</sup>
		J (CDIP, 20)
SN54ACT573	Military	W (CFP, 20)
		FK (LCCC, 20)
		DB (SSOP, 20)
		DW (SOIC, 20)
SN74ACT573	Catalag	N (WQFN, 20)
SN/4AC15/3	Catalog	NS (SOP, 20)
		PW (TSSOP, 20)
		RKS (VQFN, 20)

For more information, see Section 11.



To Seven Other Channels

Logic Diagram (Positive Logic)



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#### 4 Pin Configuration and Functions

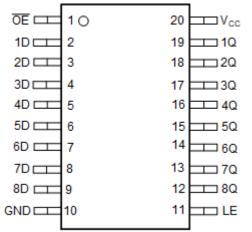


Figure 4-1. SN54ACT573 J or W Package, SN74ACT573 DB, DW, N, NS, or PW Package (Top View)

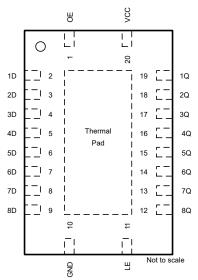


Figure 4-2. SNx4ACT573 RKS Package, 20-Pin VQFN (Top View)

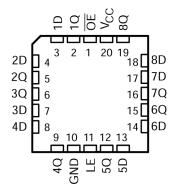


Figure 4-3. SN54ACT573 FK Package, 20-Pin LCCC (Top View)



#### **Table 4-1. Pin Functions**

	PIN	TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.	ITPE(")	DESCRIPTION
ŌĒ	1	I	Output enable
1D	2	I	1D input
2D	3	I	2D input
3D	4	I	3D input
4D	5	I	4D input
5D	6	I	5D input
6D	7	I	6D input
7D	8	I	7D input
8D	9	I	8D input
GND	10	_	Ground
LE	11	I	Latch enable input
8Q	12	0	8Q output
7Q	13	0	7Q output
6Q	14	0	6Q output
5Q	15	0	5Q output
4Q	16	0	4Q output
3Q	17	0	3Q output
2Q	18	0	2Q output
1Q	19	0	1Q output
V <sub>CC</sub>	20	_	Power pin
Thermal	Thermal Pad <sup>(2)</sup> —		The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

<sup>(1)</sup> I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

<sup>(2)</sup> For RKS package only.

#### **5 Specifications**

#### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>1</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	Supply voltage range			V
V <sub>I</sub> <sup>(2)</sup>	Input voltage range	-0.5	V <sub>CC</sub> + 0.5	V	
V <sub>O</sub> <sup>(2)</sup>	Output voltage range	-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	$(V_1 < 0 \text{ or } V_1 > V_{CC})$		±20	mA
I <sub>OK</sub>	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±50	mA
	Continuous current through, V <sub>C0</sub>	or GND		±200	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### **5.2 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)1

		SN54ACT573		SN74AC	SN74ACT573	
		MIN	MAX	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
Vo	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-24	mA
I <sub>OL</sub>	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate		8		8	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

#### 5.3 Thermal Information

	THERMAL METRIC	DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	101.2	70	69	60	126.2	67.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



#### **5.4 Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T,	<sub>λ</sub> = 25°C		SN54AC	T573	SN74ACT573		UNIT
PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49		4.4		4.4		
	10Η = =30 μΑ	5.5 V	5.4	5.49		5.4		5.4		
V	I <sub>OH</sub> = -24 mA	4.5 V	3.86			3.7		3.76		v
V <sub>OH</sub>	10H24 111A	5.5 V	4.86			4.7		4.76		·
	$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^{(1)}$	5.5 V						3.85		
	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	
	Ιοι – 30 μΑ	5.5 V			0.1		0.1		0.1	V
V	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44		0.44	
V <sub>OL</sub>	10L - 24 IIIA	5.5 V			0.36		0.44		0.44	v
	I <sub>OL</sub> = 50 mA <sup>(1)</sup>	5.5 V					1.65			
	I <sub>OL</sub> = 75 mA <sup>(1)</sup>	5.5 V							1.65	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±5		±2.5	μA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μA
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	μA
ΔI <sub>CC</sub> (2)	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		5						pF

<sup>(1)</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

#### 5.5 Timing Requirements

over operating free-air temperature range,  $V_{CC}$  = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T <sub>A</sub> = 25°	T <sub>A</sub> = 25°C SN54ACT573		SN74ACT	UNIT		
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
t <sub>w</sub>	Pulse duration, LE high	3.5		5		4		ns
t <sub>su</sub>	Setup time, data before LE↓	3		4.5		3.5		ns
t <sub>h</sub>	Hold time, data after LE↓	0		1		0		ns

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<sup>(2)</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.



#### **5.6 Switching Characteristics**

over operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	T <sub>A</sub> = 25°C			SN54AC	T573	SN74AC	T573	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
t <sub>PLH</sub>	D	Q	2.5	6	10.5	1.5	13.5	2	12	ns
t <sub>PHL</sub>	Б	Q	2.5	6	10.5	1.5	13.5	2	12	115
t <sub>PLH</sub>	LE	Q	3	6	10.5	1.5	13	2.5	12	ns
t <sub>PHL</sub>	LE	Q	2.5	5.5	9.5	1.5	12	2	10.5	115
t <sub>PZH</sub>	OE	Q	2	5.5	10	1.5	11.5	1.5	11	ns
t <sub>PZL</sub>	J OE	Q	1.5	5.5	9.5	1.5	11	1.5	10.5	115
t <sub>PHZ</sub>	ŌĒ	Q	2.5	6.5	11	1.5	13.5	1.5	12.5	ne
t <sub>PLZ</sub>	OE.	Q	1.5	5	8.5	1.5	10.5	1	9.5	ns

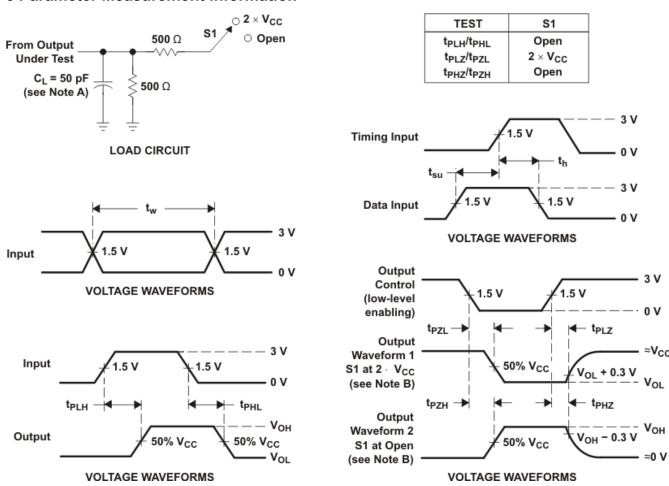
## **5.7 Operating Characteristics**

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	C <sub>L</sub> = 50 pF,	f = 1 MHz	25	pF



#### **6 Parameter Measurement Information**



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

#### 7.1 Overview

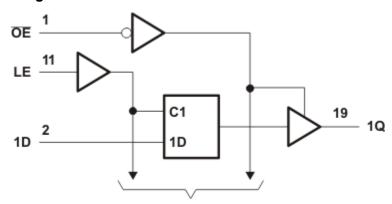
The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable  $(\overline{OE})$  input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

 $\overline{\text{OE}}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie  $\overline{\text{OE}}$  to  $V_{\text{CC}}$  through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

#### 7.2 Functional Block Diagram



To Seven Other Channels

Figure 7-1. Logic Diagram (Positive Logic)

#### 7.3 Device Functional Modes

# Function Table (Each Latch)

	OUTPUT		
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	$Q_0$
Н	X	Χ	Z



## 8 Application and Implementation

#### **Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### 8.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in Section 5.2.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1  $\mu$ F and if there are multiple  $V_{CC}$  terminals, then TI recommends .01  $\mu$ F or .022  $\mu$ F for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

#### 8.2 Layout

#### 8.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

#### 8.2.2 Layout Example

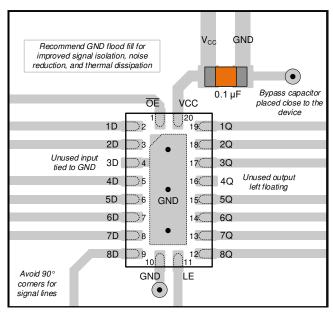


Figure 8-1. Example layout for the SNx4ACT573

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#### 9 Device and Documentation Support

#### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 9.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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#### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2023) to Revision G (March 2024)	Page
• Updated RθJA values: DW = 58 to 101.2, PW = 83 to 126.2, all values in °C/W	5
Added Application and Implementation section	10
Changes from Revision E (August 2023) to Revision F (November 2023)	Page
Added the RKS package information	
Updated the Device Information table to include rating	1

#### 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-87664012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87664012A SNJ54ACT 573FK
5962-8766401RA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8766401RA SNJ54ACT573J
5962-8766401SA	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8766401SA SNJ54ACT573W
SN74ACT573DBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD573
SN74ACT573DBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD573
SN74ACT573DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-40 to 85	ACT573
SN74ACT573DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT573
SN74ACT573DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT573
SN74ACT573N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT573N
SN74ACT573N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT573N
SN74ACT573NSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT573
SN74ACT573NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT573
SN74ACT573PW	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	AD573
SN74ACT573PWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD573
SN74ACT573PWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD573
SN74ACT573RKSR	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ACT573
SN74ACT573RKSR.A	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ACT573
SNJ54ACT573FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87664012A SNJ54ACT 573FK
SNJ54ACT573FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87664012A SNJ54ACT 573FK
SNJ54ACT573J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8766401RA SNJ54ACT573J

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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SNJ54ACT573J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8766401RA SNJ54ACT573J
SNJ54ACT573W	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8766401SA SNJ54ACT573W
SNJ54ACT573W.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8766401SA

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54ACT573, SN74ACT573:

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## PACKAGE OPTION ADDENDUM

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◆ Catalog : SN74ACT573

• Automotive : SN74ACT573-Q1, SN74ACT573-Q1

Military: SN54ACT573

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Military - QML certified for Military and Defense Applications

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 24-Jul-2025

#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT573DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74ACT573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT573NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT573RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT573DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ACT573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT573NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ACT573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT573RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

## **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87664012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8766401SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ACT573N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT573N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ACT573FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT573FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT573W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ACT573W.A	W	CFP	20	25	506.98	26.16	6220	NA





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

  D. Index point is provided on cap for terminal identification only.

  E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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