







SN54ACT244, SN74ACT244

# SCAS517G - JUNE 1995 - REVISED MARCH 2024

# **SNx4ACT244 Octal Buffers and Drivers With 3-State Outputs**

#### 1 Features

- 4.5V to 5.5V V<sub>CC</sub> operation
- Inputs accept voltages to 5.5V
- Maximum t<sub>pd</sub> of 9.5ns at 5V
- Inputs are TTL-compatible
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## 2 Applications

- LED displays
- Servers and telecommunication
- Switching networks

## 3 Description

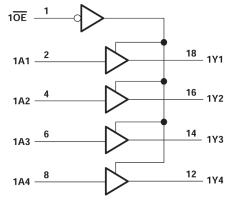
These SNx4ACT244 octal buffers and drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

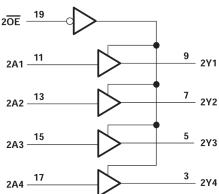
The SNx4ACT244 devices are organized as two 4bit buffers and drivers with separate output-enable (OE) inputs. When OE is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the highimpedance state.

#### **Device Information**

PART NUMBER	RATING	PACKAGE <sup>(1)</sup>
		DGS (VSSOP, 20)
		DB (SSOP, 20)
SN74ACT244		DW (SOIC, 20)
	Catalog	N (PDIP, 20)
		NS (SO, 20)
		PW (TSSOP, 20)
		RKS (VQFN, 20)
		J (CDIP, 20)
SN54ACT244	Military	W (CFP, 20)
		FK (LCCC, 20)

(1) For more information, see Section 11.





Logic Diagram (Positive Logic)



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## 4 Pin Configuration and Functions

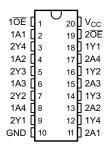


Figure 4-1. SN54ACT244: J or W Packages, 20-Pin CDIP or CFP (Top View)

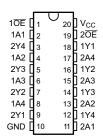


Figure 4-2. SN74ACT244: DGS, DB, DW, N, NS, or PW Packages, 20-Pin VSSOP SSOP, SOIC, PDIP, SO, or TSSOP (Top View)

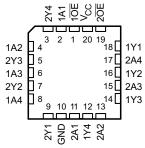


Figure 4-3. SN54ACT244: FK Package 20-Pin LCCC (Top View)

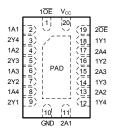


Figure 4-4. SN74ACT244: RKS Packages, 20-Pin VQFN (Top View)

**Table 4-1. Pin Functions** 

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME	I TPE	DESCRIPTION
1	1 ŌĒ	I	1 Active low Output enable
2	1A1	I	1A1 input
3	2Y4	0	2Y4 output
4	1A2	I	1A2 input
5	2Y3	0	2Y3 Output
6	1A3	I	1A3 input
7	2Y2	0	2Y2 Output
8	1A4	I	1A4 input
9	2Y1	0	2Y1 Output
10	GND	_	Ground
11	2A1	I	2A1 input
12	1Y4	0	1Y4 output
13	2A2	I	2A2 input
14	1Y3	0	1Y3 Output
15	2A3	I	2A3 input
16	1Y2	0	1Y2 Output
17	2A4	I	2A4 input
18	1Y1	0	1Y1 Output
19	2 OE	I	2 Active low Output enable
20	V <sub>CC</sub>	_	Power

(1) I = input, O = output



## **5 Specifications**

#### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
VI	Input voltage <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
Vo	Output voltage <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	$V_{l} < 0 \text{ or } V_{l} > V_{CC}$		±20	mA
I <sub>OK</sub>	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_{O} = 0$ to $V_{CC}$		±50	mA
	Continuous current through V <sub>CC</sub> or GND	·		±200	mA
T <sub>J</sub>	Absolute Maximum Junction Temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

			VALUE	UNIT				
SN74AC	CT244 in DW Package							
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000					
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±2000	V				
SN54AC	SN54ACT244 in J, W, DB, N, NS, PW, FK Packages							
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V				

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage			0.8	V
VI	Input voltage		0	V <sub>CC</sub>	V
Vo	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			-24	mA
I <sub>OL</sub>	Low-level output current			24	mA
Δt/Δν	Input transition rise or fall rate	Input transition rise or fall rate		8	ns/V
_	Operating free air temperature	SN54ACT244	-55	125	°C
T <sub>A</sub>	Operating free-air temperature SN74ACT244		-40	85	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

Product Folder Links: SN54ACT244 SN74ACT244

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



## **5.4 Thermal Information**

		SNx4ACT244							
	THERMAL METRIC(1)	DB (SSOP)	DGS (VSSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.2	123.5	101.2	48.1	106.2	126.2	67.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	76.9	62.1	68.2	34.1	72	68.7	72.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	72.1	78.5	69.7	29	71.2	77.3	40.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	43.1	7.8	44.1	19.5	42.4	22.3	10.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	71.7	78.0	69.2	28.9	70.9	76.9	40.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	24.1	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## **5.5 Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
		T <sub>A</sub> = 25°C		4.4	4.49		
		SN54ACT244	4.5 V	4.4			
	I <sub>OH</sub> = -50 μA	SN74ACT244		4.4			
	10Η30 μΑ	T <sub>A</sub> = 25°C		5.4	5.49		
		SN54ACT244	5.5 V	5.4			
		SN74ACT244		5.4			V
V	I <sub>OH</sub> = -24 mA	T <sub>A</sub> = 25°C		3.86			
V <sub>OH</sub>		SN54ACT244	4.5 V	3.7			v
		SN74ACT244		3.76			
		T <sub>A</sub> = 25°C		4.86			
		SN54ACT244	5.5 V	4.7			
		SN74ACT244		4.76			
	$I_{OH} = -50 \text{ mA}^{(1)}$	SN54ACT244	5.5 V	3.85			
	$I_{OH} = -75 \text{ mA}^{(1)}$	SN74ACT244	5.5 V	3.85			



## 5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	V <sub>CC</sub>	MIN TYP	MAX	UNIT	
		T <sub>A</sub> = 25°C		0.001	0.1		
		SN54ACT244	4.5 V		0.1		
	I - 50 A	SN74ACT244			0.1		
	I <sub>OL</sub> = 50 μA	T <sub>A</sub> = 25°C		0.001	0.1		
		SN54ACT244	5.5 V		0.1		
		SN74ACT244			0.1		
\/		T <sub>A</sub> = 25°C			0.36	V	
$V_{OL}$		SN54ACT244	4.5 V		0.5	V	
	1 = 24 m A	SN74ACT244			0.44		
	I <sub>OL</sub> = 24 mA	T <sub>A</sub> = 25°C			0.36		
		SN54ACT244	5.5 V		0.5		
		SN74ACT244			0.44		
	I <sub>OL</sub> = 50 mA <sup>(1)</sup>	SN54ACT244	5.5 V		1.65		
	I <sub>OL</sub> = 75 mA <sup>(1)</sup>	SN74ACT244	5.5 V	-	1.65		
		T <sub>A</sub> = 25°C			±0.25		
$I_{OZ}$	$V_O = V_{CC}$ or GND	SN54ACT244	5.5 V		±5	μA	
		SN74ACT244			±2.5		
		T <sub>A</sub> = 25°C		-	±0.1		
l <sub>l</sub>	$V_I = V_{CC}$ or GND	SN54ACT244	5.5 V		±1	μA	
		SN74ACT244			±1		
		T <sub>A</sub> = 25°C		-	4		
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	SN54ACT244	5.5 V		80	μA	
		SN74ACT244		-	40		
		T <sub>A</sub> = 25°C		0.6			
$\Delta_{\text{ICC}}$ (2)	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	SN54ACT244	5.5 V		1.6	mA	
	Care inpute at City of Vill	SN74ACT244			1.5		
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	T <sub>A</sub> = 25°C	5 V	2.5		pF	
C <sub>o</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	T <sub>A</sub> = 25°C	5 V	8		pF	

<sup>(1)</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 6-1)

1 3		, 60 - 1 - (			, ,	
FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	T <sub>A</sub> = 25°C	2	6.5	9		
		SN54ACT244	1		10	
	V	SN74ACT244	1.5		10	
A	Ť	T <sub>A</sub> = 25°C	2	7	9	ns
		SN54ACT244	1		10	
		SN74ACT244	1.5		10	
	FROM	FROM TO (OUTPUT)	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

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<sup>(2)</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.



## **5.6 Switching Characteristics (continued)**

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT	
			T <sub>A</sub> = 25°C	1.5	7	8.5		
t <sub>PZH</sub>			SN54ACT244	1		9.5		
	ŌĒ	Y	SN74ACT244	1		9.5	20	
	OE .	T T	T <sub>A</sub> = 25°C	2	7	9.5	ns	
t <sub>PZL</sub>			SN54ACT244	1		11		
			SN74ACT244	1.5		10.5		
			T <sub>A</sub> = 25°C	2	8	9.5		
t <sub>PHZ</sub>			SN54ACT244	1		11		
	ŌĒ		SN74ACT244	1.5		10.5		
		OE Y	T T	T <sub>A</sub> = 25°C	2.5	7.5	10	ns
t <sub>PLZ</sub>		SN54ACT244 SN74ACT244	SN54ACT244	1		11.5		
			SN74ACT244	2		10.5		

# **5.7 Operating Characteristics**

 $V_{CC}$  = 5 V,  $T_A$  = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	$C_L = 50 \text{ pF}, \qquad f = 1 \text{ MHz}$	45	pF

# **5.8 Typical Characteristics**

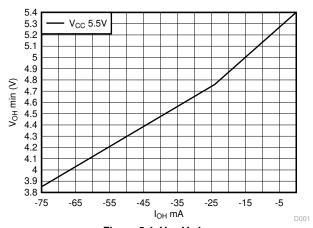
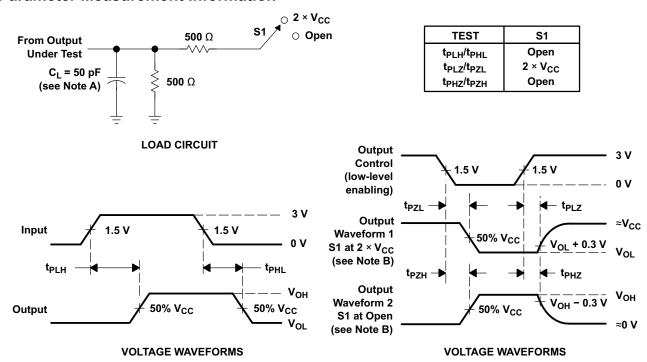


Figure 5-1.  $V_{\rm OH}$  Vs  $I_{\rm OH}$ 



## **6 Parameter Measurement Information**



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

# 7 Detailed Description

## 7.1 Overview

The SNx4ACT244 devices are buffer drivers with separate output enable inputs. The active low output enable sets the output to high impedance when a logic high is applied. For the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 7.2 Functional Block Diagram

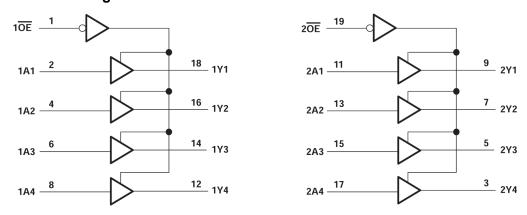


Figure 7-1. Logic Diagram (Positive Logic)

#### 7.3 Feature Description

The SNx4ACT244 devices are recommended for 4.5 V to 5.5-V  $V_{CC}$  range under normal operating conditions. The inputs are TTL compatible accepting 2-V minimum high at 5-V  $V_{CC}$ .

#### 7.4 Device Functional Modes

Table 7-1 lists the functions of the device.

Table 7-1. Function Table (Each Buffer)

INP	OUTPUT				
ŌE	ŌE A				
L	Н	Н			
L	L	L			
Н	X	Hi-Z			

## 8 Application and Implementation

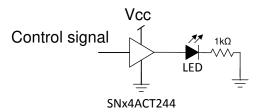
#### Note

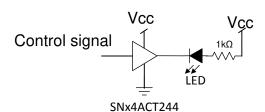
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### 8.1 Application Information

The SNx4ACT244 is high-drive buffer drivers providing 24-mA current drive per channel at nominal operating specifications. It can be used as LED driver with appropriate current-limiting resistors to ground or  $V_{CC}$  withing the device's and LEDs operating characteristics.

#### 8.2 Typical Application





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Figure 8-1. Typical LED driving application

#### 8.2.1 Design Requirements

The pullup and pull-down current limiting resistors are chosen to operate within the LED and the SNx4ACT244 device operating specifications. A 1-k $\Omega$  resistor, limits the current to less than 5 mA at 5-V V<sub>CC</sub> operation.

#### 8.2.2 Detailed Design Procedure

- 1. Recommended input conditions:
  - For the specified high and low levels See (V<sub>IH</sub> and V<sub>IL</sub>) in the Section 5.3.
  - Inputs are not overvoltage tolerant and must be limited to V<sub>CC</sub>.
- 2. Recommended output conditions:
  - Limit the output voltage to V<sub>CC</sub>.
  - Choose the current-limiting resistor for the LED to limit the output current to I<sub>O</sub> as per the Section 5.3.

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#### 8.2.3 Application Curve

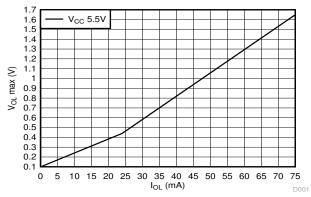


Figure 8-2. V<sub>OL</sub> vs I<sub>OL</sub>

#### 8.3 Power Supply Recommendations

The power supply may be any voltage between the MIN and MAX supply voltage rating located in the Section 5.3.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for devices with a single supply. If there are multiple  $V_{CC}$  terminals, then 0.01- $\mu$ F or 0.022- $\mu$ F capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

#### 8.4 Layout

#### 8.4.1 Layout Guidelines

Inputs should not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in the Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

#### 8.4.2 Layout Example



Figure 8-3. Layout Example



## 9 Device and Documentation Support

#### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, Implications of Slow or Floating CMOS Inputs

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision F (November 2023) to Revision G (March 2024)

Page

#### Changes from Revision E (July 2023) to Revision F (November 2023)

Page

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-8776001M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 8776001M2A SNJ54ACT 244FK
5962-8776001MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001MR A SNJ54ACT244J
5962-8776001MSA	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001MS A SNJ54ACT244W
5962-8776001SRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001SR A SNV54ACT244J
5962-8776001SRA.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001SR A SNV54ACT244J
5962-8776001SSA	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001SS A SNV54ACT244W
5962-8776001SSA.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001SS A SNV54ACT244W
SN74ACT244DBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ACT244, AD244)
SN74ACT244DBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(ACT244, AD244)
SN74ACT244DGSR	Active	Production	VSSOP (DGS)   20	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT244
SN74ACT244DGSR.A	Active	Production	VSSOP (DGS)   20	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT244
SN74ACT244DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-40 to 85	ACT244
SN74ACT244DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244DWRE4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244DWRG4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT244N
SN74ACT244N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT244N





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Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74ACT244NE4	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT244N
SN74ACT244NSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244NSRG4	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT244
SN74ACT244PW	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	AD244
SN74ACT244PWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	AD244
SN74ACT244PWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244
SN74ACT244PWRE4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244
SN74ACT244PWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244
SN74ACT244PWRG4.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD244
SN74ACT244RKSR	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-45 to 125	ACT244
SN74ACT244RKSR.A	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-45 to 125	ACT244
SNJ54ACT244FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 8776001M2A SNJ54ACT 244FK
SNJ54ACT244FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 8776001M2A SNJ54ACT 244FK
SNJ54ACT244J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001MR A SNJ54ACT244J
SNJ54ACT244J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001MR A SNJ54ACT244J
SNJ54ACT244W	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001MS A SNJ54ACT244W
SNJ54ACT244W.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776001MS A SNJ54ACT244W

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

## PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN54ACT244, SN54ACT244-SP, SN74ACT244:

Catalog: SN74ACT244, SN54ACT244

Automotive: SN74ACT244-Q1, SN74ACT244-Q1

Enhanced Product: SN74ACT244-EP, SN74ACT244-EP

Military: SN54ACT244

Space: SN54ACT244-SP

NOTE: Qualified Version Definitions:



# PACKAGE OPTION ADDENDUM

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- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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## TAPE AND REEL INFORMATION



## 

	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT244DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74ACT244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74ACT244NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT244RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT244DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ACT244DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74ACT244DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT244NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ACT244PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT244PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT244PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT244RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8776001M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8776001MSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-8776001SSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-8776001SSA.A	W	CFP	20	25	506.98	26.16	6220	NA
SN74ACT244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT244N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ACT244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ACT244FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT244FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT244W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ACT244W.A	W	CFP	20	25	506.98	26.16	6220	NA





#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# W (R-GDFP-F20)

# CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

  D. Index point is provided on cap for terminal identification only.

  E. Falls within Mil—Std 1835 GDFP2—F20







#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







#### NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. No JEDEC registration as of September 2020.
- 5. Features may differ or may not be present.





#### NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- 9. Size of metal pad may vary due to creepage requirement.
- 10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025