

SN74ACT164-Q1 8-Bit Serial-In/Parallel-Out Shift Register

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Operating voltage range of 4.5V to 5.5V
- TTL-compatible inputs
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 14.9ns at 5V

2 Applications

- Increase the number of outputs on a microcontroller
- Store up to 8 bits of data temporarily

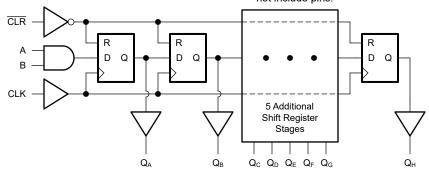
3 Description

The SN74ACT164-Q1 device contains an 8-bit shift register with AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum set-up time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
SN74ACT164-Q1	BQA (WQFN, 14)	3mm × 2.50mm	3mm × 2.50mm
3N74AC1104-Q1	PW (TSSOP, 14)	5mm x 6.4mm	5mm x 4.4mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Functional Diagram



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4 Pin Configuration and Functions

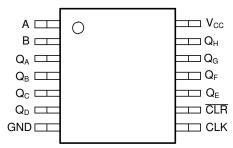


Figure 4-1. PW Package, 14-Pin TSSOP (Top View)

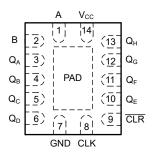


Figure 4-2. WBQA Package 14-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.	ITPE''	DESCRIPTION
A	1	I	Gated serial input A
В	2	I	Gated serial input B
Q _A	3	0	Parallel output A
Q _B	4	0	Parallel output B
Q _C	5	0	Parallel output C
Q_D	6	0	Parallel output D
GND	7	G	Ground
CLK	8	I	Clock input, rising edge triggered
CLR	9	I	Asynchronous register clear input, active low
Q _E	10	0	Parallel output E
Q _F	11	0	Parallel output F
Q_{G}	12	0	Parallel output G
Q _H	13	0	Parallel output H
V _{CC}	14	Р	Positive supply
Thermal page	(2)	_	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

⁽¹⁾ Signal Types: I = Input, O = Output, P = Power, G = Ground.

⁽²⁾ WBQA package only.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	V _{CC} + 0.5V	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5V	V
I _{IK}	Input clamp current	$V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V$		±20	mA
I _{OK}	Output clamp current	V_{O} < -0.5V or V_{O} > V_{CC} + 0.5V		±50	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±50	mA
	Continuous output current through V _{CC} or GND			±200	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000		
	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	V	

⁽¹⁾ AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-Level input voltage		0.8	V
VI	Input Voltage	0	V _{CC}	V
Vo	Output Voltage	0	V _{CC}	V
I _{OH}	High-level output current		-24	mA
I _{OL}	Low-level output current		24	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	-40	125	°C

5.4 Thermal Information

PACKAGE	PACKAGE PINS		THERMAL METRIC(1)					
FACRAGE	FINS	R _{0JA}	R _{0JC(top)}	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	R _{0JC(bot)}	UNIT
PW (TSSOP)	14	148.0	81.1	104.5	22.2	103.0	-	°C/W
BQA (WQFN)	14	105.3	106.6	74.6	18.2	74.3	51.9	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

Product Folder Links: SN74ACT164-Q1

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETIONS	V	-40°(-40°C to 125°C			
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT	
	I - 50A	4.5V	4.4				
	I _{OH} = -50μA	5.5V	5.4				
V _{OH}	I _{OH} = -24mA	4.5V	3.7			V	
	I _{OH} = -24mA	5.5V	4.7				
	$I_{OH} = -75 \text{mA}^{(3)}$	5.5V	3.85				
	I - 50A	4.5V			0.1		
	I _{OH} = 50μA	5.5V			0.1		
V _{OL}	I _{OH} = 24mA	4.5V			0.5	V	
	I _{OH} = 24mA	5.5V			0.5		
	I _{OH} = 75mA ⁽³⁾	5.5V	-		1.65		
I _I	V _I = 5.5V or GND	0V to 5.5V			±1	μA	
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V			80	μA	
ΔI_{CC}	$V_I = V_{CC} - 2.1V$; Any Input	4.5V to 5.5V			1.5	mA	
Cı	V _I = V _{CC} or GND	5V		8		pF	
Co	V _O = V _{CC} or GND	5V	-	14		pF	
C _{PD} (1) (2)	C _L = 50pF, F = 1MHz	5V		60		pF	

- (1) C_{PD} is used to determine the dynamic power consumption, per channel
 (2) P_D = V_{CC} ²xF_Ix(C_{PD}+ C_L) where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage
 (3) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V	-40°C to 125°C	UNIT
	DESCRIPTION	CONDITION	V _{CC}	MIN MAX	
f _{CLOCK}	Clock frequency		5V	120	MHz
t _W	Pulse duration	CLR low	5V	1.7	ns
t _W	Pulse duration	CLK high or low	5V	1.4	ns
t _{SU}	Setup time	Data before CLK↑	5V	0	ns
t _{SU}	Setup time	CLR inactive	5V	0	ns
t _H	Hold time	Data after CLK↑	5V	2	ns



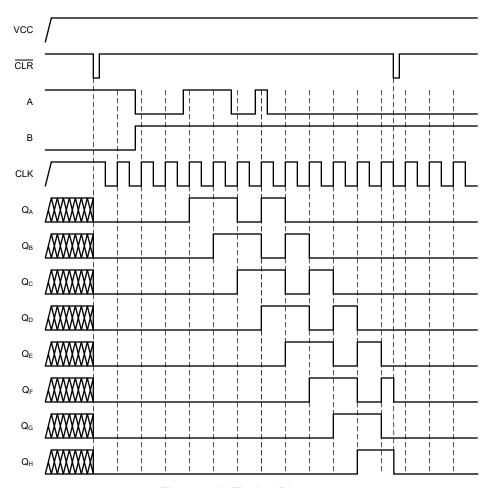


Figure 5-1. Timing Diagram

5.7 Switching Characteristics

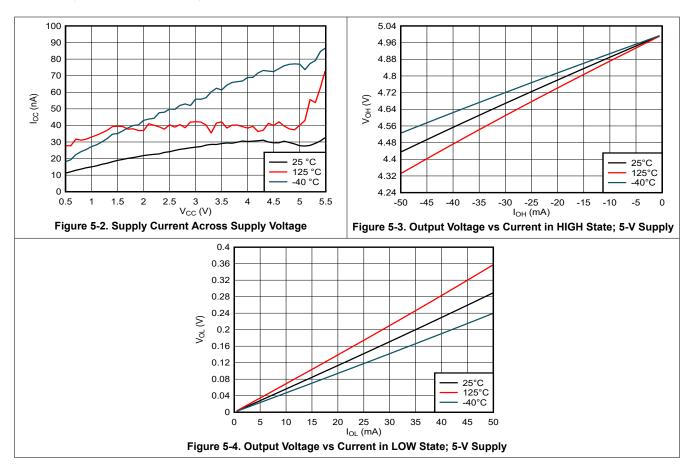
 C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

L '		1 0 7 31					,
PARAMETER	EROM (INDIT) TO (OUTDIT)		V	-40°C to 125°C			UNIT
PARAMETER	FROW (INFOT)	FROM (INPUT) TO (OUTPUT) V _{CC}	V _{CC}	MIN	TYP	MAX	ONIT
t _{PLH}	CLK	Q	5V			14.9	ns
t _{PHL}	CLK	Q	5V			14.9	ns
t _{PHL}	CLR	Q	5V			15.8	ns



5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)



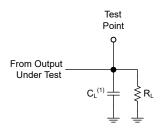


6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_t < 2.5$ ns, $V_t = 1.5$ V. For push-pull outputs, $R_L = 500\Omega$.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.



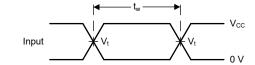


Figure 6-2. Voltage Waveforms, Pulse Duration

(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

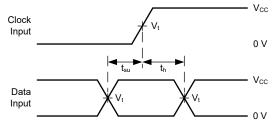
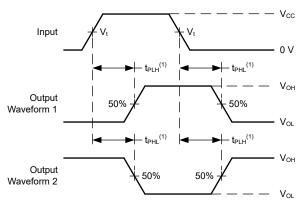
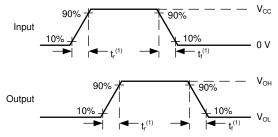


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_{r} and t_{f} is the same as t_{t} .

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

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7 Detailed Description

7.1 Overview

The SN74ACT164-Q1 is an 8-bit shift register with 2 serial inputs (A and B) connected through an AND gate, as well as an asynchronous clear (CLR). The device requires a high signal on both A and B to set the input data line high; a low signal on either input will set the input data line low. Data at A and B can be changed while CLK is high or low, provided that the minimum set-up time requirements are met.

The CLK pin of the SN74ACT164-Q1 is rising-edge triggered, activating on the transition from LOW to HIGH. Upon a positive-edge trigger, the device will store the result of the $(A \bullet B)$ input data line in the first register and propagate each register's data to the next register. The data of the last register, Q_H , will be discarded at each clock trigger. If a low signal is applied to the \overline{CLR} pin, then the SN74ACT164-Q1 will set all registers to a logical low value immediately.

7.2 Functional Block Diagram

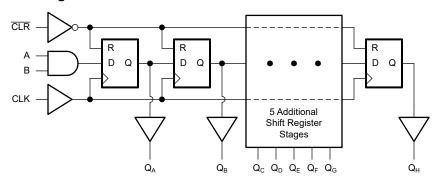


Figure 7-1. Logic Diagram (Positive Logic) for SN74ACT164-Q1

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the



maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a $10k\Omega$ resistor is recommended and typically will meet all requirements.

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

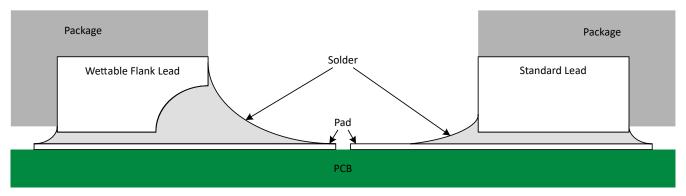


Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.5 Clamp Diode Structure

As shown in Figure 7-3, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Product Folder Links: SN74ACT164-Q1

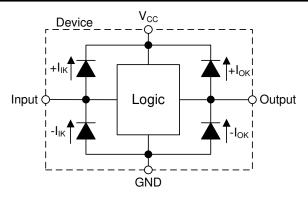


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74ACT164-Q1.

Table 7-1. Function Table

	INPL	JTS ⁽¹⁾		FUNCTION			
Α	В	CLR	CLK	FONCTION			
Х	Х	L	X	Shift register is cleared.			
L	Х	Н	1	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.			
Х	L	Н	1	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.			
Н	Н	Н	1	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.			

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74ACT164-Q1 is used to control seven-segment displays. Unlike other I/O expanders, the SN74ACT164-Q1 does not need a communication interface for control. It can easily operate with simple GPIO pins. Additional control is provided with two serial inputs that feed into an AND gate.

At power-up, the initial state of the shift registers is unknown. To give them a defined state, the shift register needs to be cleared. An RC can be connected to the $\overline{\text{CLR}}$ pin as shown in Figure 8-1 to initialize the shift register to all zeros.

8.2 Typical Application

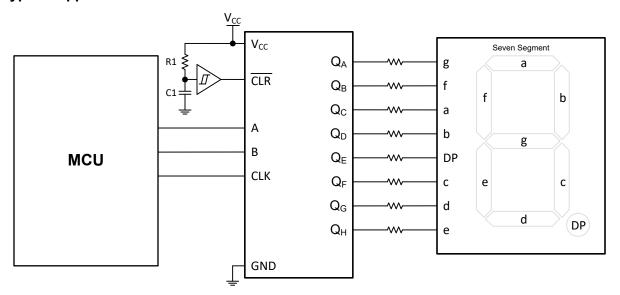


Figure 8-1. Typical Application Block Diagram

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8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT164-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT164-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT164-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT164-Q1 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear* and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT164-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A $10k\Omega$ resistor value is often used due to these factors.

The SN74ACT164-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the Feature Description section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the Feature Description section for additional information regarding the outputs for this device.

Product Folder Links: SN74ACT164-Q1

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8.2.1.4 Application Curve

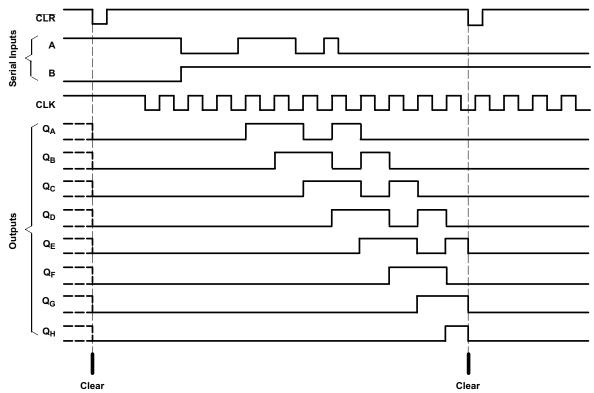


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces
 - For traces longer than 12cm
 - · Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - · Avoid branches; buffer signals that must branch separately



8.4.2 Layout Example

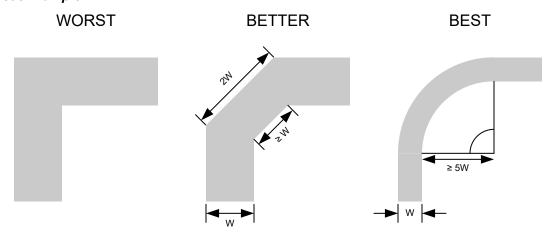


Figure 8-3. Example Trace Corners for Improved Signal Integrity

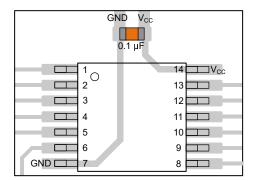


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

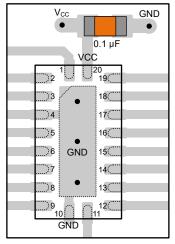


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

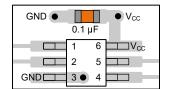


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

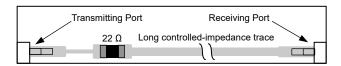


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
						(4)	(9)		
SN74ACT164PWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT164Q
SN74ACT164PWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT164Q
SN74ACT164WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD164Q
SN74ACT164WBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD164Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT164PWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT164WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT164PWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74ACT164WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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