

SN74ACT126-Q1 Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Operating voltage range of 4.5V to 5.5V
- TTL-compatible inputs
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 8.7ns

2 Applications

- Drive an indicator LED
- Redrive a digital signal
- Drive a transmission line
- Hold a signal during controller reset

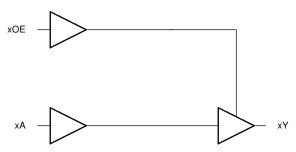
3 Description

The SN74ACT126-Q1 contains four independent 3state buffers.

Device Information

	ART MBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE(3)
SN74A		PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
Q1		BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm

- For more information, see Section 11.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



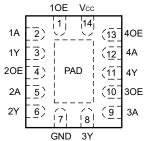
Functional Block Diagram

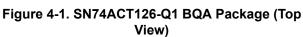


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4 Pin Configuration and Functions





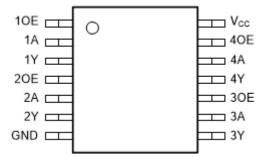


Figure 4-2. SN74ACT126-Q1 , PW Package (Top View)

Pin Functions

	PIN	TYPE ⁽¹⁾	DESCRIPTION				
NAME	NO.	1 TPE(')	DESCRIPTION				
10E	1	I	Channel 1, output enable				
1A	2	I	Channel 1, input A				
1Y	3	0	Channel 1, output Y				
20E	2OE 4 I		Channel 2, output enable				
2A	2A 5 I		Channel 2, input B				
2Y	6	0	Channel 2, output Y				
GND	7	G	Ground				
3Y	8	0	Channel 3, output Y				
3A	9	I	Channel 3, input A				
30E	10	I	Channel 3, output enable				
4Y	11	0	Channel 4, output Y				
4A	12	I	Channel 4, input A				
40E	13	I	Channel 4, output enable				
V _{CC}	14	Р	Positive supply				
Therm	nal Pad ⁽²⁾	_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.				

- (1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
- (2) BQA package only.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$V_{I} < -0.5V \text{ or } V_{I} > V_{CC} + 0.5V$		±20	mA
I _{OK}	Output clamp current	V_{O} < -0.5V or V_{O} > V_{CC} + 0.5V		±50	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±50	mA
	Continuous output current through V _{CC} or GND			±200	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
	Electrostatic	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	
V _(ESD)	discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	V

⁽¹⁾ AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-Level input voltage		0.8	V
VI	Input Voltage	0	V _{CC}	V
Vo	Output Voltage	0	V _{CC}	V
I _{OH}	High-level output current		-24	mA
I _{OL}	Low-level output current		24	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	-40	125	°C

5.4 Thermal Information

PACKAGE	PINS			THERMAL	METRIC ⁽¹⁾			UNIT
PACKAGE	FINS	R _{0JA}	R _{0JC(top)}	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	R _{0JC(bot)}	ONII
PW (TSSOP)	14	149.8	81.6	106.0	23.5	104.7	N/A	°C/W

Product Folder Links: SN74ACT126-Q1

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



PACKAGE	PINS			THERMAL	METRIC ⁽¹⁾			UNIT
PACKAGE	FINS	R _{0JA}	R _{0JC(top)}	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	R _{θJC(bot)}	UNII
BQA (WQFN)	14	95.2	106.6	64.8	19.8	64.6	40.4	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
	I - FOA	4.5V	4.4	4.49		
	$I_{OH} = -50\mu A$	5.5V	5.4	5.49		
V _{OH}	I _{OH} = -24mA	4.5V	3.7			V
	I _{OH} = -24mA	5.5V	4.7			
	$I_{OH} = -75 \text{mA}^{(1)}$	5.5V	3.85			
	I - FOA	4.5V		0.01	0.1	
	I _{OL} = 50μA	5.5V		0.01	0.1	V
V _{OL}	I _{OL} = 24mA	4.5V			0.5	
	I _{OL} = 24mA	5.5V			0.5	
	I _{OL} = 75mA ⁽¹⁾	5.5V			1.65	
I _I	V _I = 5.5V or GND	0V to 5.5V			±1	μΑ
I _{OZ}	V _O = V _{CC} or GND	5.5V			±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V		0.1	2	μA
ΔI _{CC}	$V_I = V_{CC} - 2.1V$; Any Input	4.5V to 5.5V			1.5	mA
Cı	V _I = V _{CC} or GND	5V		2		pF
Co	Output disabled, V _O = V _{CC} or GND	5V		4		pF

⁽¹⁾ Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

DADAMETED	FROM	то	V.	-40°0	C to 125°C		
PARAMETER	(INPUT)) (OUTPUT)	V _{#b#CC}	MIN	TYP	MAX	UNIT
C _L = 15pF						'	
t _{PLH}	A	Υ	4.5 V	2.3	4.2	6.6	no
t _{PHL}		Ţ	4.5 V	2.8	4.8	7.4	ns
t _{PLZ}	- OE	Υ	4.5 V	1.9	3.3	5.1	
t _{PHZ}		ĭ	4.5 V	2.8	4.8	7.4	ns
t _{PZL}	- OE	Υ	4.5 V	2.2	4.1	6.6	
t _{PZH}		ĭ	4.5 V	2.5	4.7	7.5	ns
t _r		Υ	4.5 V	0.6	1.3	2.2	
t _f		Y	4.5 V	0.6	1.2	1.8	ns
t _{sk(o)}		Υ	4.5 V		0	0.2	ns
t _{PLH}	Δ.	Υ	5.5 V	2.2	4	6.2	
t _{PHL}	A	ĭ	5.5 V	2.4	4.2	6.3	ns
t _{PLZ}	05	V	5.5 V	1.6	2.8	4.76	
t _{PHZ}	OE	Y	5.5 V	2.5	4.2	6.4	ns



over operating free-air temperature range (unless otherwise noted)

FROM	то	V	-40°C	C to 125°C		UNIT
(INPUT)	(OUTPUT)	V#b#CC	MIN	TYP	MAX	UNII
OE	V	5.5 V	2.1	3.9	6.2	ne
	'	5.5 V	2.4	4.4	6.9	ns
	V	5.5 V	0.5	1.2	2	ns
	ı	5.5 V	0.6	1.1	1.6	115
	Υ	5.5 V		0	0.2	ns
-			•			
	V	4.5 V	2.8	5.2	8.3	ne
	ľ	4.5 V	3.2	5.7	8.7	ns
OF	V	4.5 V	2.3	3.7	5.4	
JOE	Ť	4.5 V	3.6	5.8	8.7	ns
OF	V	4.5 V	2.8	5.3	8.4	20
JOE	Y	4.5 V	3.2	5.9	9.3	ns
	V	4.5 V	1.2	2.7	4.5	-
7	Ť	4.5 V	1.2	2.3	3.6	ns
1	Υ	4.5 V		0.1	0.3	ns
	V	5.5 V	2.8	4.9	7.6	
A	Y	5.5 V	2.9	5	7.5	ns
1	.,	5.5 V	2	3.2	4.92	
OE	Y	5.5 V	2.9	4.8	7	ns
		5.5 V	2.8	4.9	7.6	
OE	Y	5.5 V	3.1	5.5	8.6	ns
+		5.5 V	1.1	2.4	4	
7	Y	5.5 V	1.2	2.1	3.2	ns
	Υ					ns
		4.5 V	4	7.2	11.4	
A	Y	4.5 V	4.3	7.4	11.3	ns
OE	Υ					ns
+						
OE	Υ		_			ns
-	Y					ns
	Υ					ns
			3.7			
A	Y					ns
OE	Υ					ns
OE	Υ					ns
	Y	J.J V	2.4	3.4	9.3	ns
	'	5.5 V	2.4	4.4	6.9	110
	(INPUT) OE A OE OE A OE OE A OE A OE A OE A OE A OE A OE OE	(INPUT)	(INPUT) (OUTPUT) 5.5 V 6.5 V	OE	Company Court Co	(INPUT) (OUTPUT)



over operating free-air temperature range (unless otherwise noted)

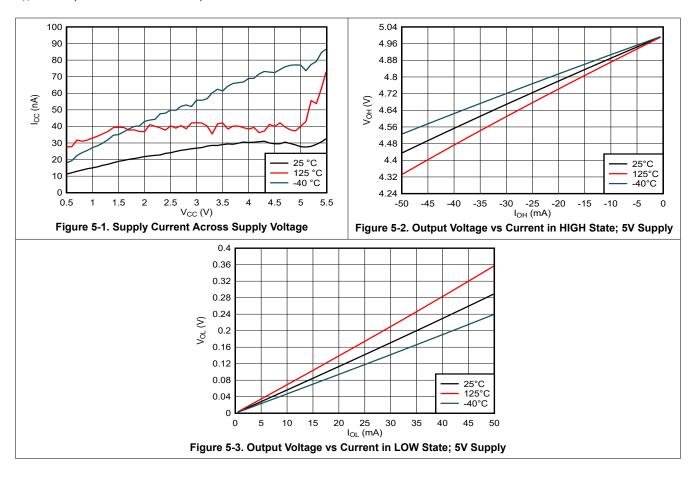
PARAMETER	FROM	то	V	-40°0	c to 125°C		UNIT	
	PARAMETER	(INPUT)	(OUTPUT)	V#b#CC	MIN TYP MA	MAX	ONII	
	C _{PD} ⁽¹⁾	Any		5V		15		pF

(1) Power dissipation capacitance is calculated using the method described in CMOS Power Consumption and Cpd Calculation.



5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

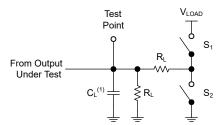


6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_t < 2.5$ ns, $V_t = 1.5$ V.

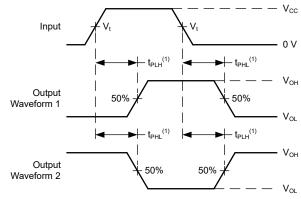
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R _L	CL	ΔV	V _{LOAD}
t _{PLH} , t _{PHL}	OPEN	OPEN	500Ω	50pF	_	_
t _{PLZ} , t _{PZL}	CLOSED	OPEN	500Ω	50pF	0.3V	2×V _{CC}
t _{PHZ} , t _{PZH}	OPEN	CLOSED	500Ω	50pF	0.3V	_



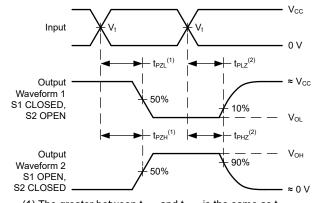
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between $t_{\textrm{PLH}}$ and $t_{\textrm{PHL}}$ is the same as $t_{\textrm{pd}}.$

Figure 6-2. Voltage Waveforms Propagation Delays



- (1) The greater between $t_{\mbox{\scriptsize PZL}}$ and $t_{\mbox{\scriptsize PZH}}$ is the same as $t_{\mbox{\scriptsize en}}.$
- (2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis} .

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

Figure 6-3. Voltage Waveforms Propagation Delays

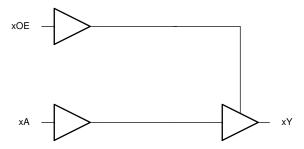


7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function Y = A in positive logic.

7.2 Functional Block Diagram



One of four channels

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7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a $10k\Omega$ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a $10k\Omega$ resistor is recommended and typically will meet all requirements.



7.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

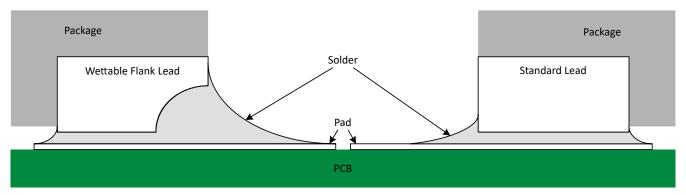


Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

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7.3.4 Clamp Diode Structure

As shown in Figure 7-2, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

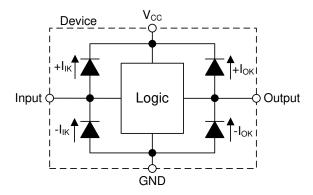


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output



7.4 Device Functional Modes

Table 7-1. Function Table

INP	UTS	OUTPUT		
OE	Α	Y		
L	Х	Z		
Н	L	L		
Н	Н	Н		

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74ACT126-Q1 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

8.2 Typical Application

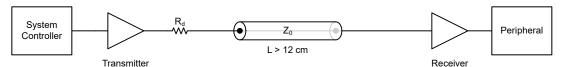


Figure 8-1. Typical Application Block Diagram



8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics of the device, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT126-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT126-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT126-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT126-Q1 can drive a load with total resistance described by $R_L \ge V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption* and *Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT126-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A $10k\Omega$ resistor value is often used due to these factors.

The SN74ACT126-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the Feature Description for additional information regarding the inputs for this device.

Product Folder Links: SN74ACT126-Q1

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.



8.2.2 Detailed Design Procedure

- Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
- 2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT126-Q1 to one or more of the receiving devices.
- 3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
- 4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the CMOS Power Consumption and Cpd Calculation application note.

8.2.3 Application Curve

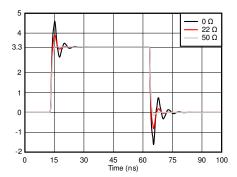


Figure 8-2. Simulated Signal Integrity at the Receiver with Different Damping Resistor (R_d) Values

Product Folder Links: SN74ACT126-Q1

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8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the $Recommended\ Operating\ Conditions$. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- · Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

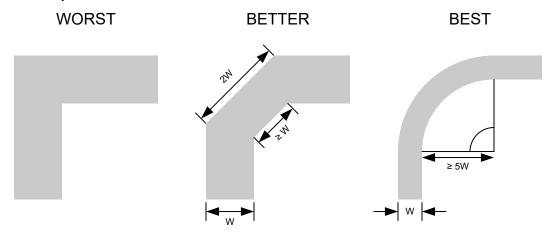


Figure 8-3. Example Trace Corners for Improved Signal Integrity

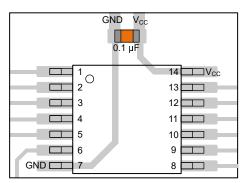


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

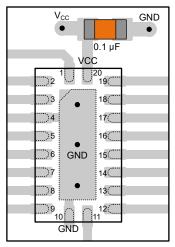


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

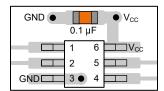


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

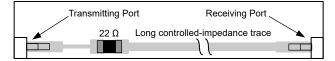


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

Submit Document Feedback

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application note
- · Texas Instruments, Designing With Logic application note
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES		
November 2025	*	Initial Release		



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74ACT126-Q1

www.ti.com 14-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74ACT126PWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	ACT126Q
SN74ACT126WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	AD126Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ACT126-Q1:

Catalog: SN74ACT126

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 14-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$ Catalog - TI's standard catalog product



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



www.ti.com



PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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