

SN74ACT00-Q1 Quadruple 2-Input Positive-NAND Gate

1 Features

- Qualified for automotive applications
- ESD protection exceeds 2000V per MIL-STD-883, Method 3015; exceeds 200V using machine model (C = 20 pF, R = 0)
- 4.5V to 5.5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 8ns at 5V
- Inputs are TTL-voltage compatible

2 Description

The SN74ACT00 contains four independent 2-input NAND gates. Each gate performs the Boolean function of $Y = \overline{A} \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

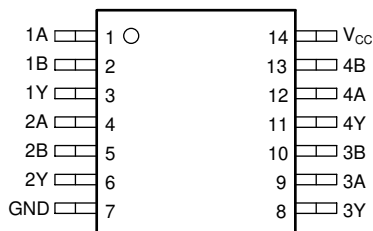
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74ACT00-Q1	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm

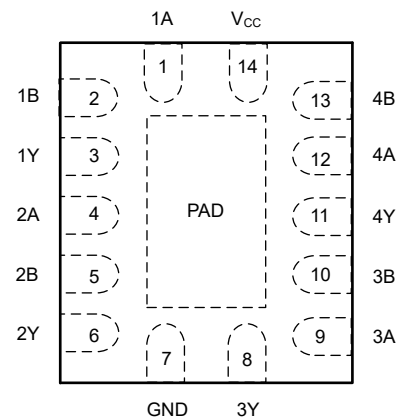
- (1) For more information, see [Section 8](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.

Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H



D or PW Package (Top View)



BQA Package (Top View)



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3 Specifications

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_I	Input voltage ⁽²⁾	–0.5	$V_{CC} + 0.5$	V
V_O	Output voltage ⁽²⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current ($V_I < 0$ or $V_I > V_{CC}$)		±20	mA
I_{OK}	Output clamp current ($V_O < 0$ or $V_O > V_{CC}$)		±20	mA
I_O	Continuous output current ($V_O = 0$ to V_{CC})		±50	mA
	Continuous current through V_{CC} or GND		±200	mA
T_{stg}	Storage temperature	–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8	ns/V
T_A	Operating free-air temperature	–40	105	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI [Implications of Slow or Floating CMOS Inputs](#) application note.

3.3 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	PW (TSSOP)	BQA (WQFN)	UNIT
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86 ⁽²⁾	145.7	91.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	76.5	99.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	102.0	61.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	—	18.8	14.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	—	100.7	60.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	37.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application note.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

3.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = –50 µA	4.5 V	4.4	4.49		4.4		V
		5.5 V	5.4	5.49		5.4		
	I _{OH} = –24 mA	4.5 V	3.86			3.7		
		5.5 V	4.86			4.7		
V _{OL}	I _{OL} = 50 µA	4.5 V		0.001	0.1		0.1	V
		5.5 V		0.001	0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5	
		5.5 V			0.36		0.5	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		40	µA
ΔI _{CC} ⁽¹⁾	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6			1.6	mA
C _i	V _I = V _{CC} or GND	5 V		2.6				pF

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

3.5 Switching Characteristics

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 4-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A or B	Y	1.5	5.5	9	1	9.5	ns
t _{PHL}	A or B	Y	1.5	4	7	1	8	ns

3.6 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{pd}	Power dissipation capacitance	CL = 50 pF, f = 1 MHz		40		pF

4 Parameter Measurement Information

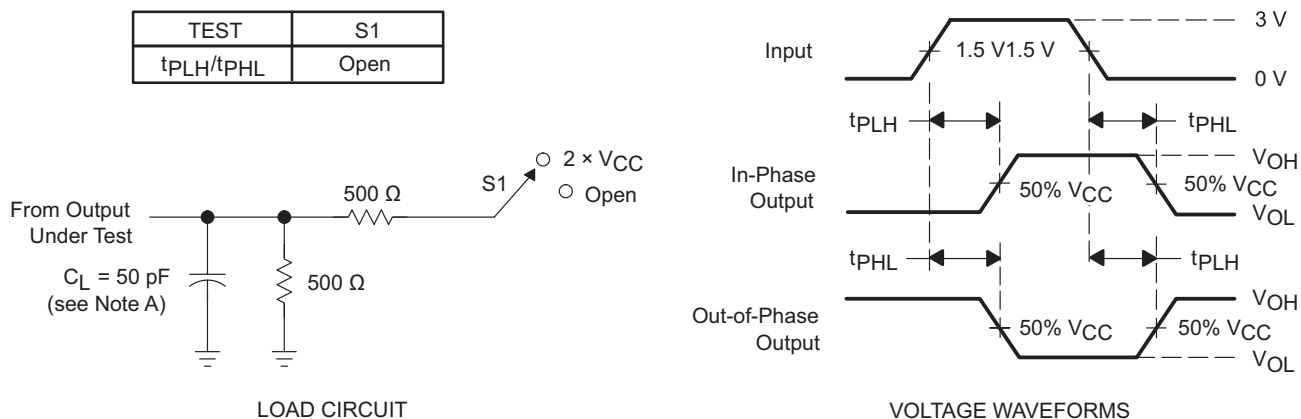


Figure 4-1. Load Circuit and Voltage Waveforms

5 Detailed Description

5.1 Functional Block Diagram



Logic Diagram, Each Gate (Positive Logic)

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

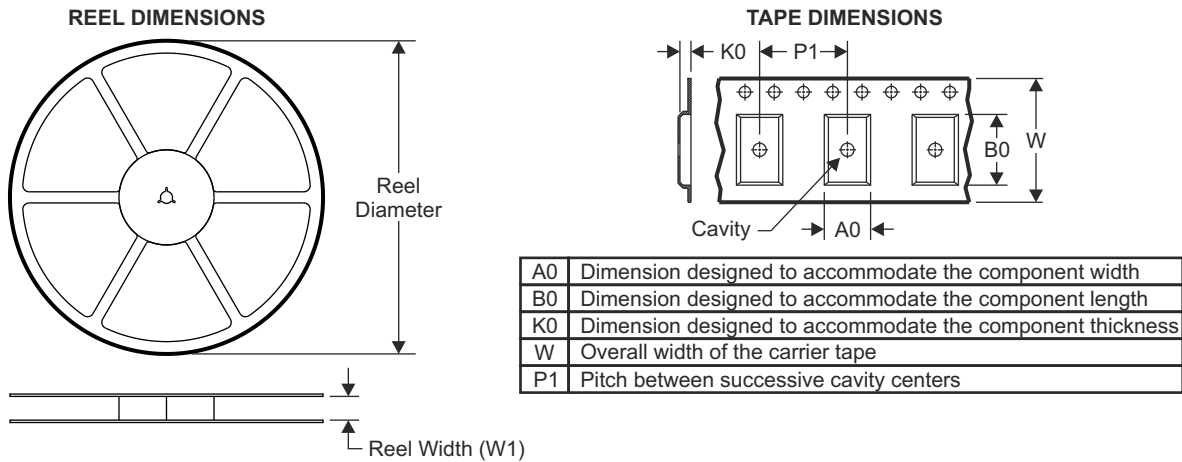
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2008) to Revision B (April 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed <i>Package Information</i> table.....	1
• Added PW and BQA packages to the data sheet.....	1
• Added <i>Thermal Information</i> table.....	3

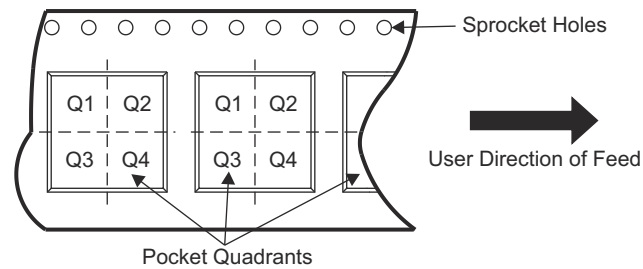
8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Tape and Reel Information

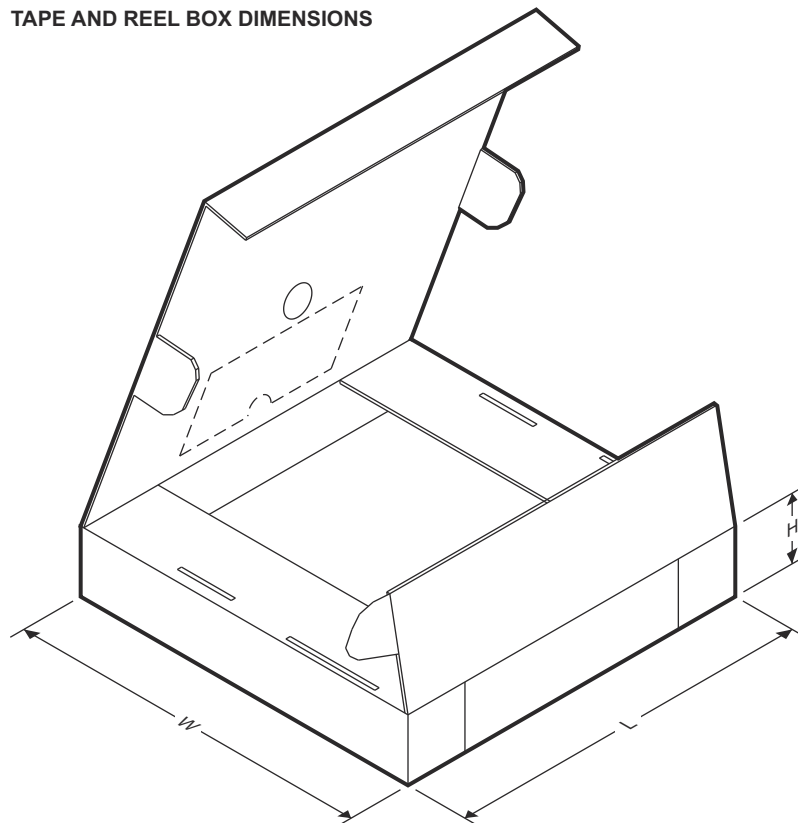


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
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8.2 Mechanical Data

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT00PWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00Q
SN74ACT00PWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00Q
SN74ACT00TDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00TQ1
SN74ACT00TDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ACT00TQ1
SN74ACT00WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AD00Q
SN74ACT00WBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	AD00Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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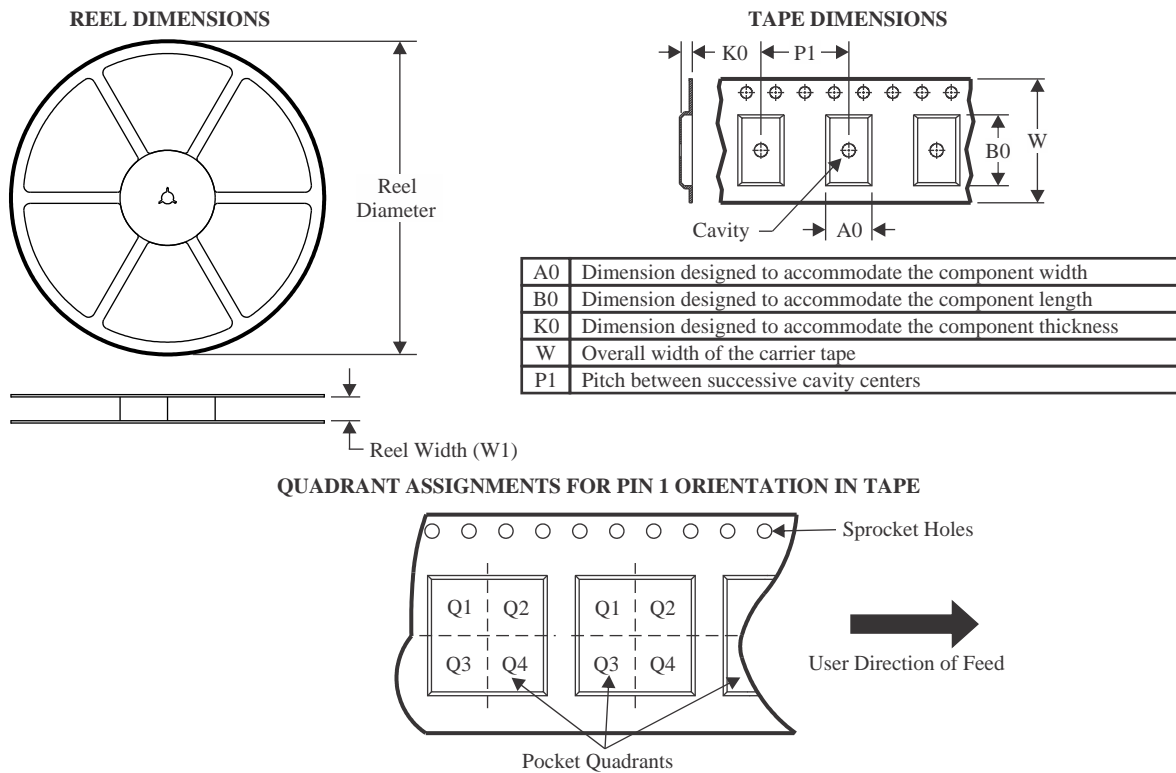
OTHER QUALIFIED VERSIONS OF SN74ACT00-Q1 :

- Catalog : [SN74ACT00](#)
- Military : [SN54ACT00](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

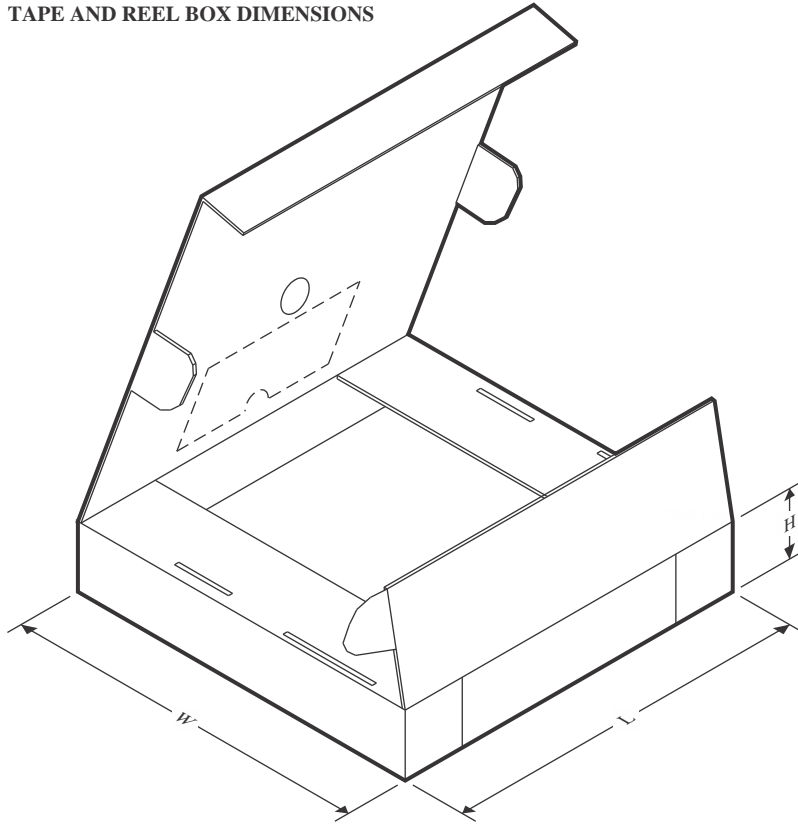
TAPE AND REEL INFORMATION



*All dimensions are nominal

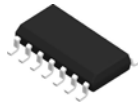
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT00PWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT00WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

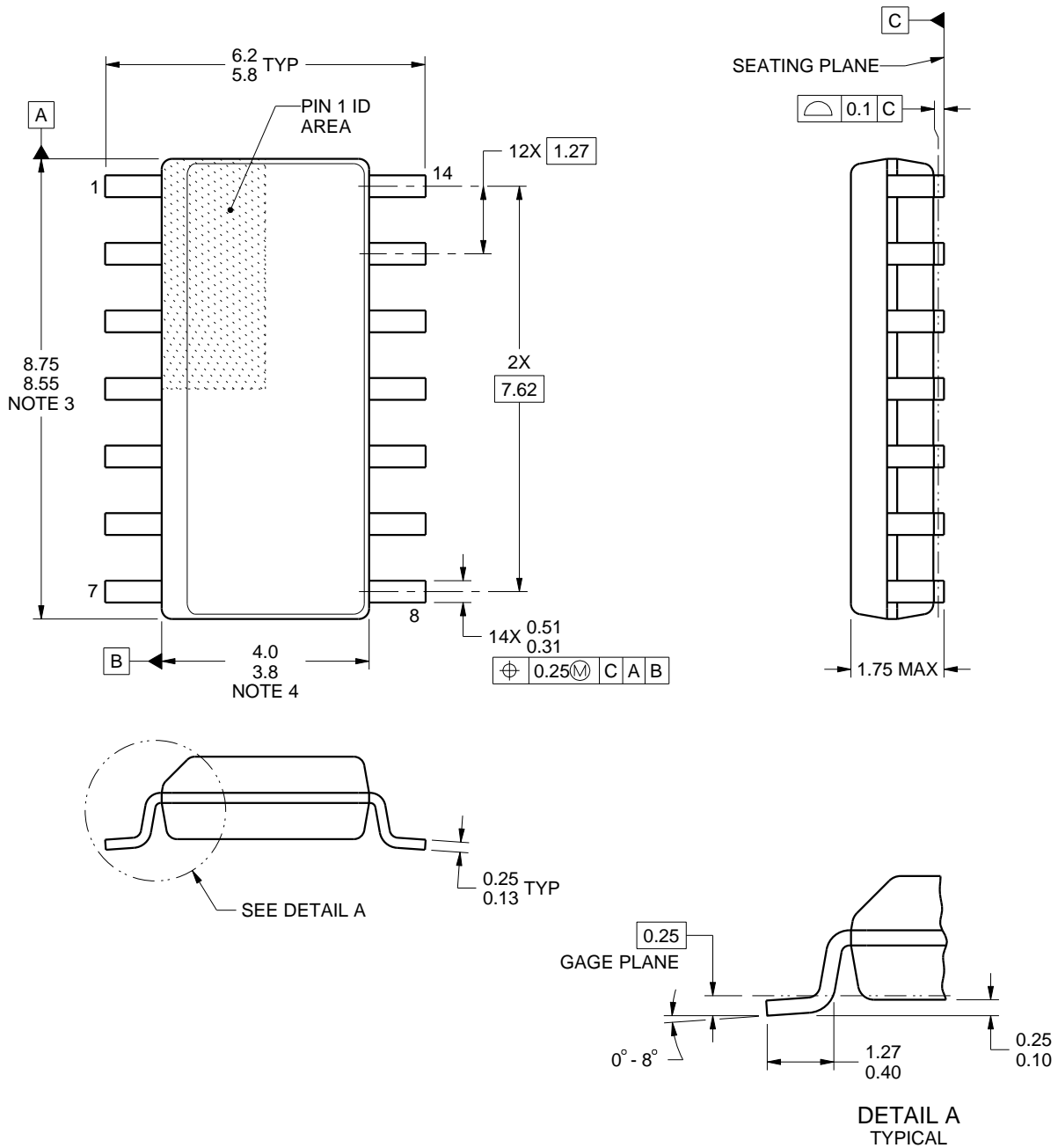


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT00PWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74ACT00WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

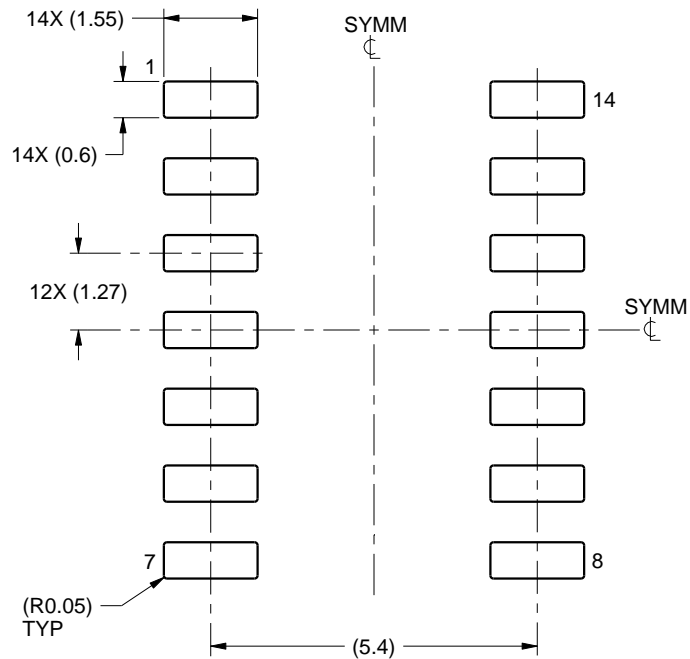
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

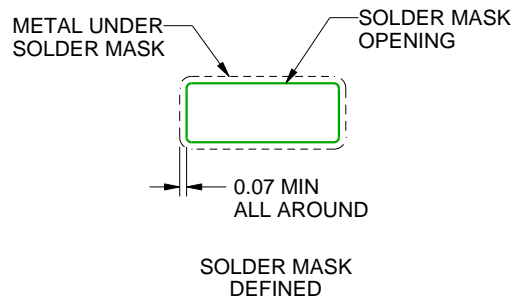
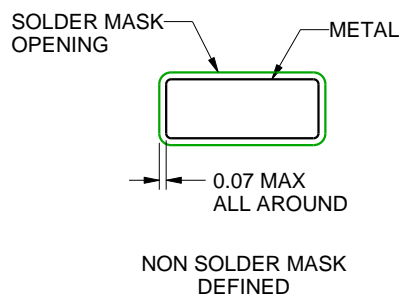
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

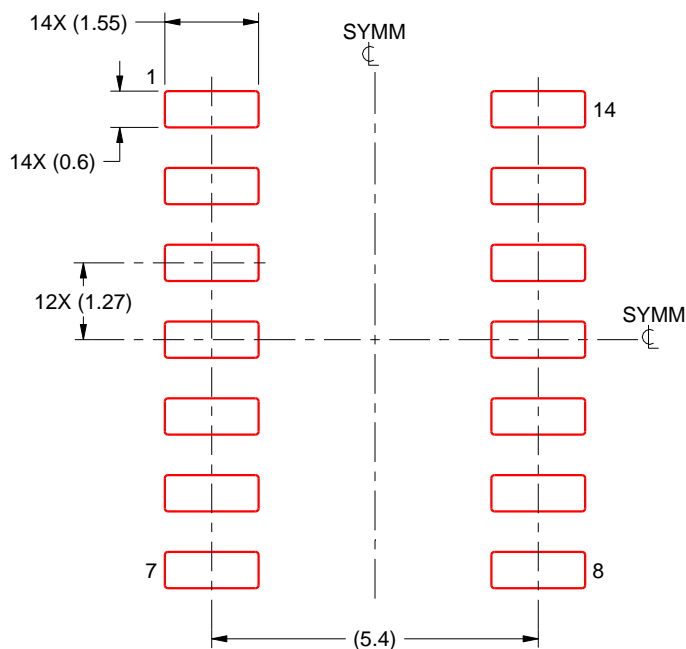
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

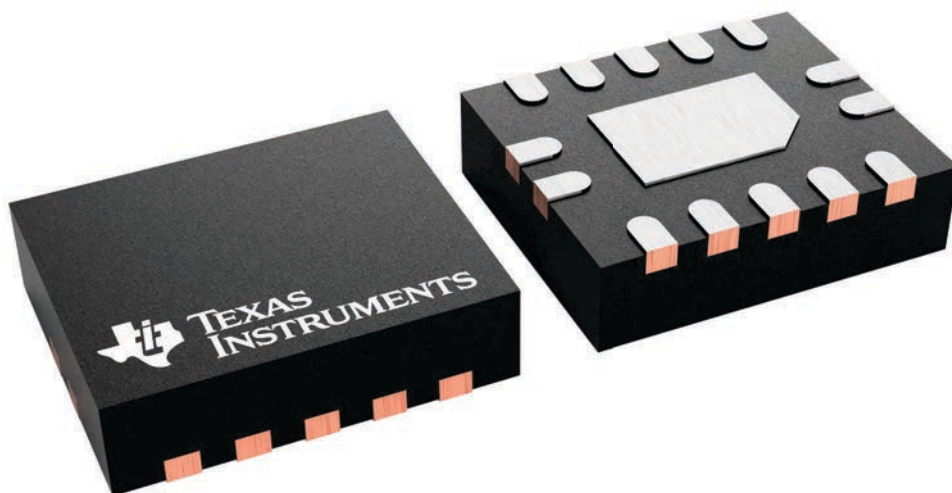
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



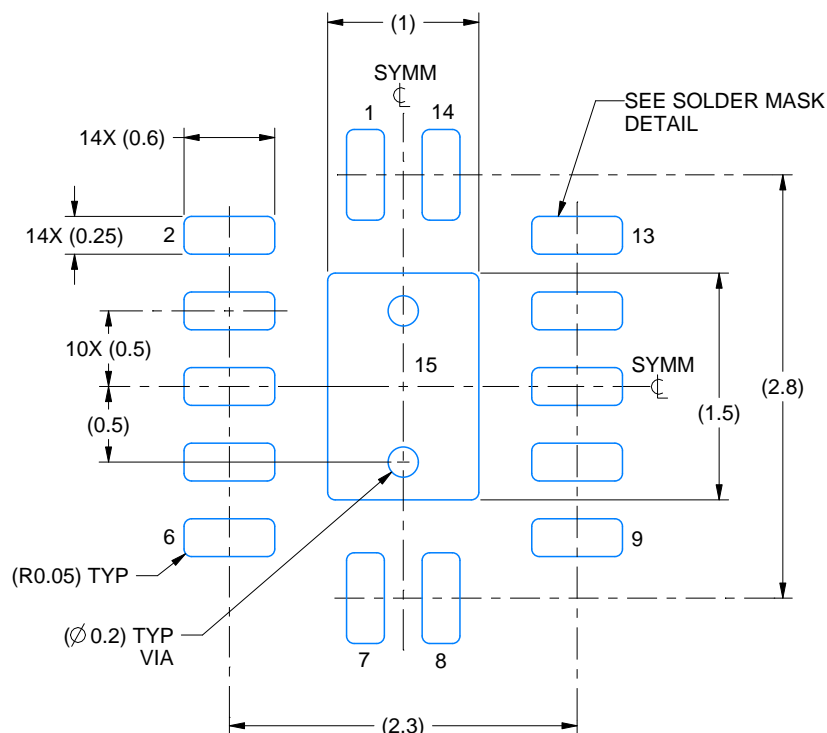
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

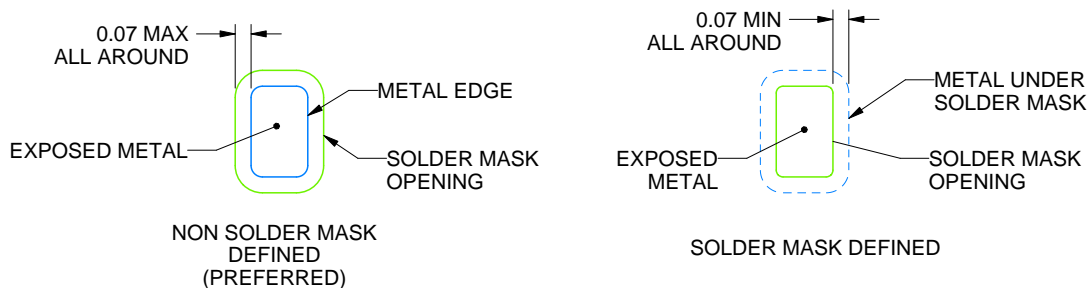
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

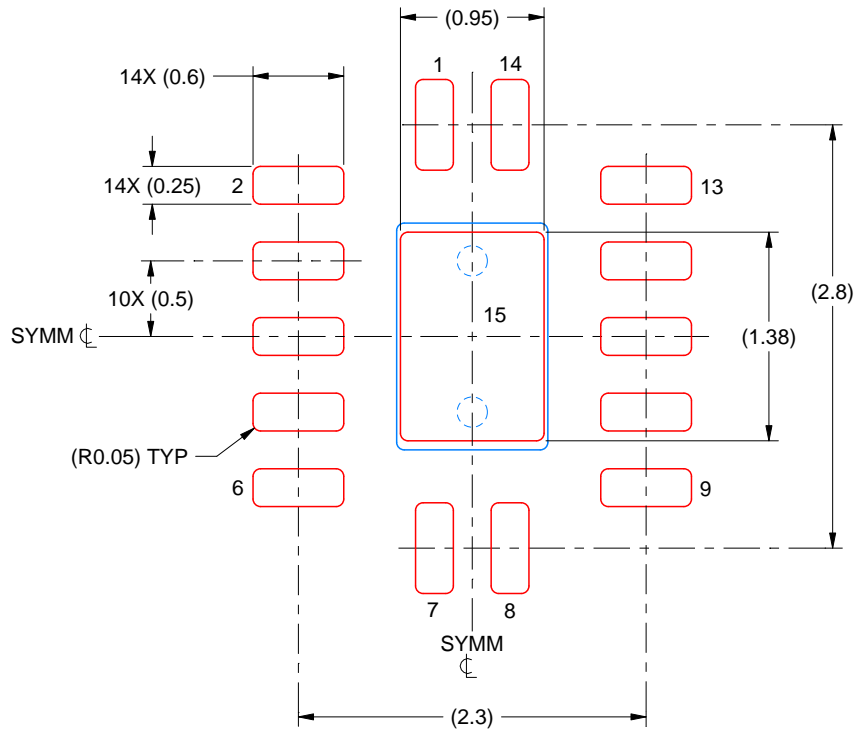
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



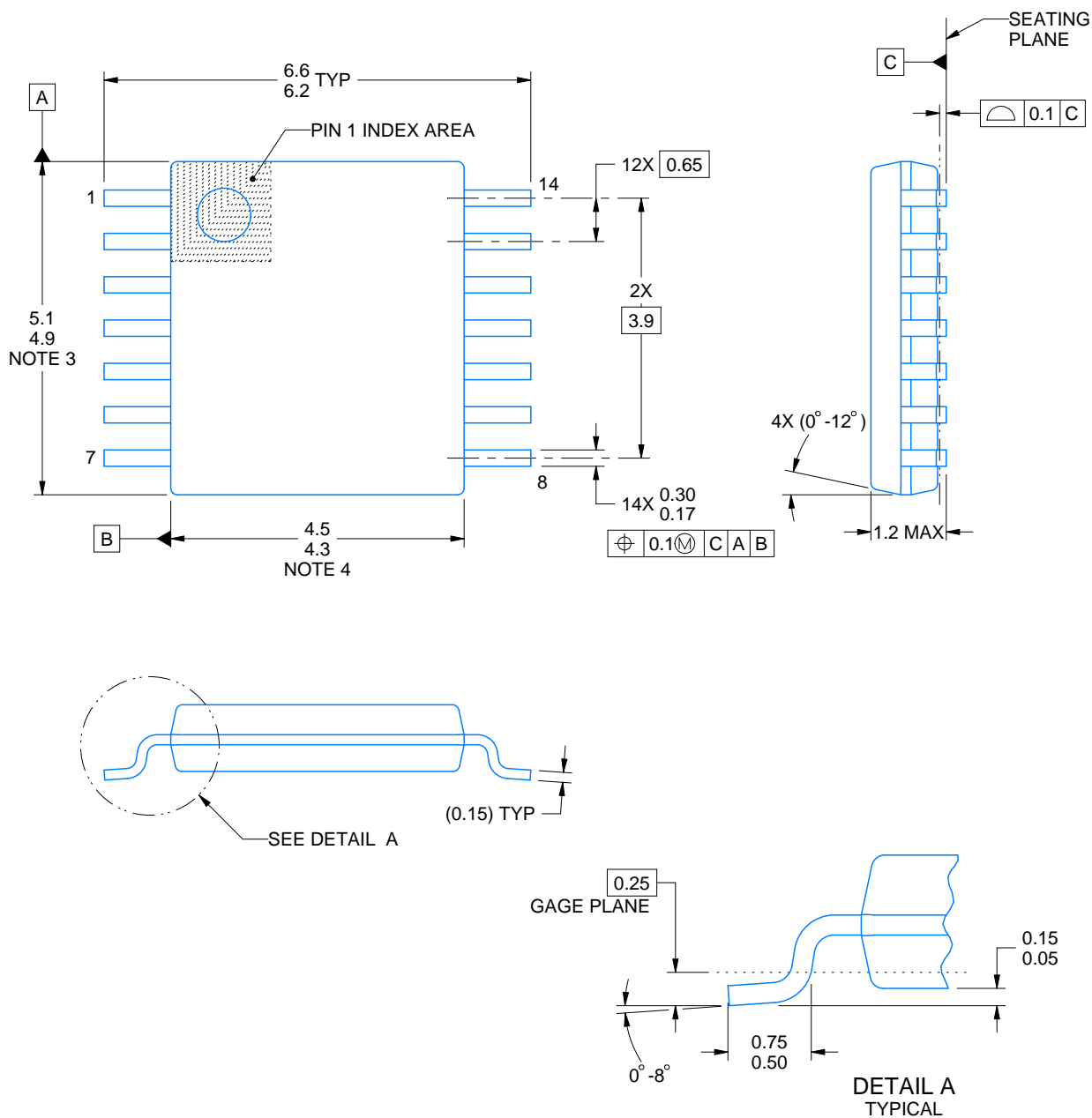
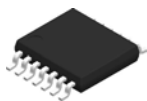
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220202/B 12/2023

NOTES:

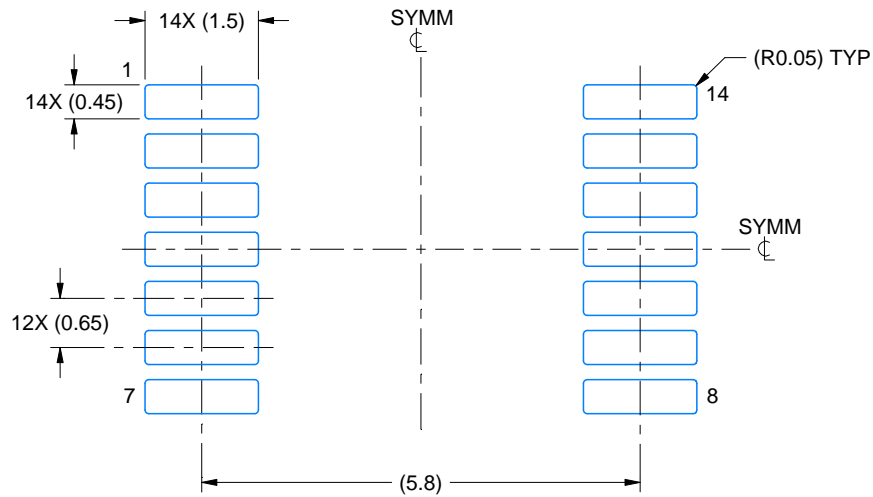
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

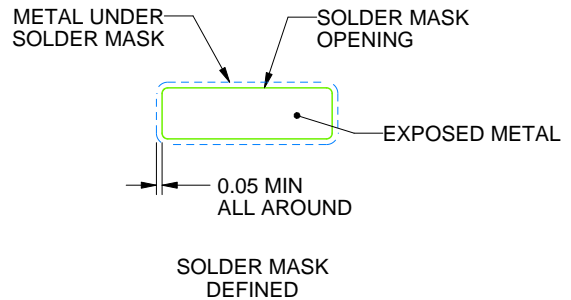
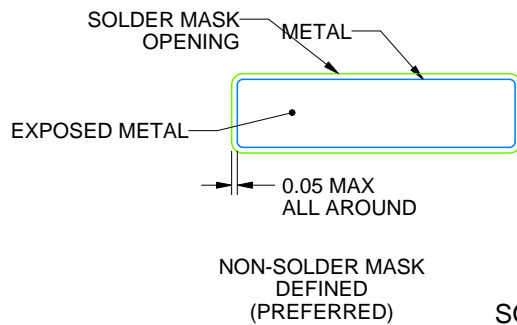
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

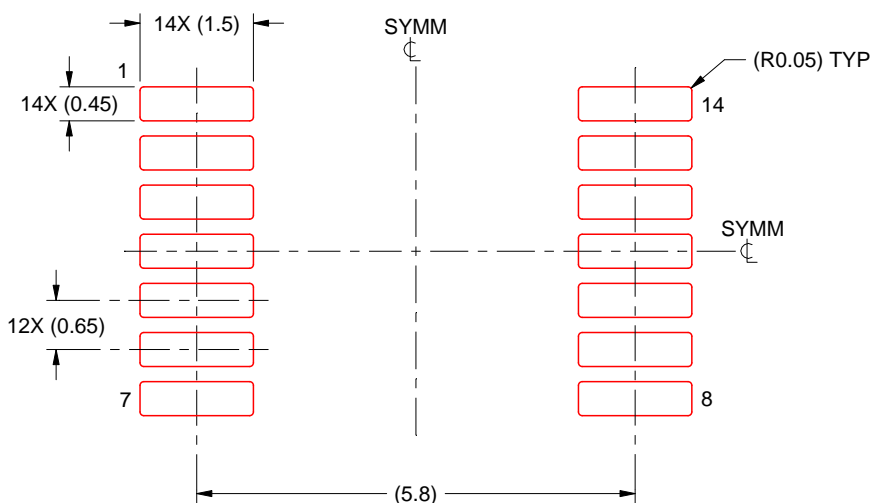
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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