









SN54AC574, SN74AC574

SCAS541G - OCTOBER 1995 - REVISED MARCH 2024

SNx4AC574 Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs

1 Features

- Operation of 2V to 6V V_{CC}
- Inputs accept voltages to 6V
- Max t_{pd} of 8.5ns at 5V
- 3-state outputs drive bus lines directly

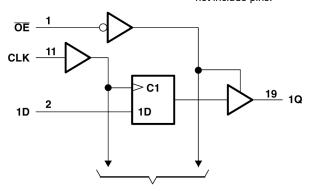
2 Description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
SNx4AC574	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DW (SOIC, 20)	12.8mm × 10.3mm	12.80mm × 7.50mm
SINX4AC574	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.50mm × 4.40mm

- For more information, see Section 10. (1)
- (2)The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



To Seven Other Channels Logic Diagram (Positive Logic)

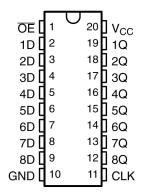


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3 Pin Configuration and Functions



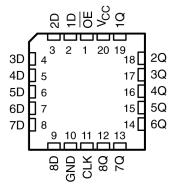


Figure 3-1. SN54AC574 J or W Package; SN74AC574 DB, DW, N, NS, or PW Package (Top View)

Figure 3-2. SN54AC574 FK Package (Top View)

Table 3-1. Pin Functions

P	PIN	I/O	DESCRIPTION				
NAME	NO.	1/0	DESCRIPTION				
ŌĒ	1	Input	Output enable for all channels, active low				
D1	2	Input	Input for channel 1				
D2	3	Input	Input for channel 2				
D3	4	Input	Input for channel 3				
D4	5	Input	Input for channel 4				
D5	6	Input	Input for channel 5				
D6	7	Input	Input for channel 6				
D7	8	Input	Input for channel 7				
D8	9	Input	Input for channel 8				
GND	10	_	Ground				
CLK	11	Input	Clock input for all channels, rising edge triggered				
Q8	12	Output	Output for channel 8				
Q7	13	Output	Output for channel 7				
Q6	14	Output	Output for channel 6				
Q5	15	Output	Output for channel 5				
Q4	16	Output	Output for channel 4				
Q3	17	Output	Output for channel 3				
Q2	18	Output	Output for channel 2				
Q1	19	Output	Output for channel 1				
V _{CC}	20	_	Postive supply				
Thermal Pad —		_	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.				



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I ⁽²⁾	Input voltage range		-0.5	V _{CC} + 0.5	V
V _O (2)	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC)}$		±20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC)}$		±20	mA
I _O	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50	mA
	Continuous current through V _{CC} or GND			±200	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			SN54AC57	SN54AC574		SN74AC574		
			MIN	MAX	MIN	MAX	UNIT	
V _{CC}	Supply voltage		2	6	2	6	V	
		V _{CC} = 3 V	2.1		2.1			
V _{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15		3.15		V	
		V _{CC} = 5.5 V	3.85		3.85			
		V _{CC} = 3 V		0.9		0.9		
V _{IL}	V _{IL} Low-level input voltage	V _{CC} = 4.5V		1.35		1.35	V	
		V _{CC} = 5.5 V		1.65		1.65		
VI	Input voltage		0	V _{CC}	0	V _{CC}	V	
Vo	Output voltage		0	V _{CC}	0	V _{CC}	V	
		V _{CC} = 3 V		-12		-12		
I _{OH}	High-level output current	V _{CC} = 4.5 V		-24		-24	mA	
		V _{CC} = 5.5 V		-24		-24		
		V _{CC} = 3 V		12		12		
I _{OL}	Low-level output current	V _{CC} = 4.5 V		24		24	mA	
		V _{CC} = 5.5 V		24		24		
Δt/Δν	Input transition rise or fall rate	·		8		8	ns/V	
T _A	Operating free-air temperature		-55	125	-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Product Folder Links: SN54AC574 SN74AC574

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



4.3 Thermal Information

		SNx4AC574					
	THERMAL METRIC(1)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	-	
				20 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	101.2	69	60	126.2	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T,	A = 25°C	SN54AC574	SN74AC574	UNIT
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP MAX	MIN MAX	MIN MAX	UNII
		3 V	2.9		2.9	2.9	
	I _{OH} = -50μA	4.5 V	4.4		4.4	4.4	
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		5.5 V	5.4		5.4	5.4	V
V _{OH}	I _{OH} = −12 mA	3 V	2.56		2.4	2.46	v
	I _{OH} = -24 mA	4.5 V	3.94		3.7	3.76	
	10H24 MA	5.5 V	4.94		4.7	4.76	
		3 V		0.1	0.1	0.1	
	I _{OL} = 50μA	4.5 V		0.1	0.1	0.1	
V		5.5 V		0.1	0.1	0.1	v
V _{OL}	I _{OL} = 12 mA	3 V		0.36	0.5	0.44	
	I = 24 mA	4.5 V		0.36	0.5	0.44	
	I _{OL} = 24 mA	5.5 V		0.36	0.5	0.44	
lı	V _I = V _{CC} or GND	5.5 V		±0.1	±1	±1	μΑ
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5	±5	±2.5	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4	80	40	μΑ
C _i	V _I = V _{CC} or GND	5 V		4.5			pF

4.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T _A = 25°C		SN54AC574		SN74AC574		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	UNII	
f _{clock}	Clock frequency		75		55		60	MHz	
t _w	Pulse duration, CLK high or low	6		7.5		7		ns	
t _{su}	Setup time, data before CLK↑	2.5		6.5		3		ns	
t _h	Hold time, data after CLK↑	1.5		2.5		1.5		ns	



4.6 Timing Requirements, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T _A = 25°C		SN54AC574		SN74AC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
f _{clock}	Clock frequency		95		85		85	MHz
t _w	Pulse duration, CLK high or low	4		5		5		ns
t _{su}	Setup time, data before CLK↑	1.5		3.5		2		ns
t _h	Hold time, data after CLK↑	1.5		2.5		1.5		ns

4.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54AC574		SN74AC574		UNIT
PARAMETER			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
f _{max}			75	112		55		60		MHz
t _{PLH}	CLK	CIV	3.5	8.5	13.5	1	16.5	3.5	15	no
t _{PHL}		Q	3.5	7.5	12	1	15	3.5	13.5	ns
t _{PZH}	- OE	Q	2.5	7	11	1	13	2.5	12	200
t _{PZL}			3	6.5	10.5	1	12.5	3	11.5	ns
t _{PHZ}	ŌĒ	OF O	3.5	7.5	12	1	14	2.5	13	no
t _{PLZ}		Q	2	5.5	9	1	10.5	1.5	10	ns

4.8 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	TO (INPUT)	TO (OUTPUT)	T	T _A = 25°C			SN54AC574		SN74AC574	
PARAMETER			MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}			95	153		85		85		MHz
t _{PLH}	CLK	0	2	6	9.5	1.5	11.5	2	11	no
t _{PHL}	CLK	Q	2	5.5	8.5	1.5	10.5	2	9.5	ns
t _{PZH}	- OE	Q	2	5	8.5	1.5	9.5	2	9	no
t _{PZL}			2	5	8	1.5	9.5	1.5	9	ns
t _{PHZ}	ŌĒ	0	2	6	9.5	1.5	11.5	1.5	10.5	no
t _{PLZ}	UE	Q	1	4.5	7.5	1.5	9	1	8.5	ns

4.9 Operating Characteristics

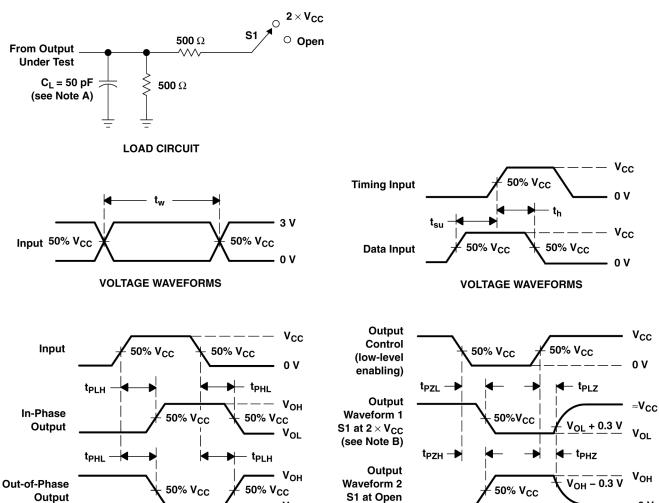
 V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF}, f = 1 \text{ MHz}$	40	pF

Product Folder Links: SN54AC574 SN74AC574



5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

(see Note B)

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

 V_{OL}

D. The outputs are measured one at a time with one input transition per measurement.

VOLTAGE WAVEFORMS

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	Open

VOLTAGE WAVEFORMS

≈0 V

6 Detailed Description

6.1 Overview

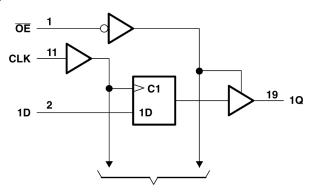
The eight flip-flops of the 'AC574 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

 $\overline{\text{OE}}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For the specified high-impedance state during power up or power down, \overline{OE} must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram



To Seven Other Channels

Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table (Each Flip-flop)

	INPUTS	OUTPUT Q	
ŌĒ	CLK	D	OUTFUT Q
L	1	Н	Н
L	1	L	L
L	H or L	Х	Q_0
Н	X	Х	Z

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μ F capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μ F or 0.022 μ F capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μ F and 1.0 μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in layout example are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.1.1 Layout Example

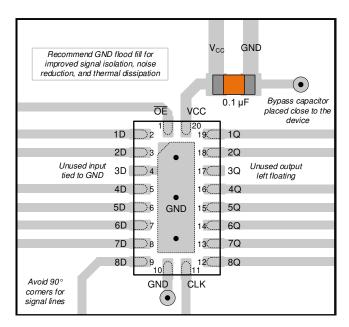


Figure 7-1. Layout example for the SNx4AC574



8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

(Changes from Revision F (August 2023) to Revision G (March 2024)	Page
•	Updated RθJA values: DW = 58 to 101.2, PW = 83 to 126.2, all values in °C/W	5
•	Added Application and Implementation section	9

Changes from Revision E (October 2003) to Revision F (August 2023)

Page

Added Device Information table, Pin Functions table, Thermal Information table, Device Functional Modes,
 Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN54AC574 SN74AC574

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9677301Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9677301Q2A SNJ54AC 574FK
5962-9677301QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J
5962-9677301QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W
SN74AC574DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SN74AC574DBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SN74AC574DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SN74AC574DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SN74AC574N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC574N
SN74AC574N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC574N
SN74AC574PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	AC574
SN74AC574PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SN74AC574PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SN74AC574PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574
SNJ54AC574FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9677301Q2A SNJ54AC 574FK
SNJ54AC574FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9677301Q2A SNJ54AC 574FK
SNJ54AC574J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J



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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	(3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54AC574J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J
SNJ54AC574W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W
SNJ54AC574W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN54AC574, SN74AC574:

• Military : SN54AC574

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC574DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC574DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AC574DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC574DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC574PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

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Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)	
5962-9677301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA	
5962-9677301QSA	W	CFP	20	25	506.98	26.16	6220	NA	
SN74AC574N	N	PDIP	20	20	506	13.97	11230	4.32	
SN74AC574N.A	N	PDIP	20	20	506	13.97	11230	4.32	
SNJ54AC574FK	FK	LCCC	20	55	506.98	12.06	2030	NA	
SNJ54AC574FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA	
SNJ54AC574W	W	CFP	20	25	506.98	26.16	6220	NA	
SNJ54AC574W.A	W	CFP	20	25	506.98	26.16	6220	NA	

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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