







SN54AC14, SN74AC14

SCAS522I - AUGUST 1995 - REVISED JULY 2024

SNx4AC14 Hex Schmitt-Trigger Inverters

1 Features

- V_{CC} operation of 2V to 6V
- · Inputs accept voltages to 6V
- Max t_{pd} of 9.5ns at 5V

2 Applications

- · Synchronize inverted clock inputs
- Debounce a switch
- · Invert a digital signal

3 Description

These Schmitt-trigger devices contain six independent inverters.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)	
	BQA (WQFN, 14)	3.00mm × 2.50mm	3.00mm × 2.50mm	
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm	
SNx4AC14	DB (SSOP, 14)	6.2mm x 7.8mm	6.2mm x 5.3mm	
SINX4AC 14	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35mm	
	NS (SOP, 14)	10.2mm x 7.8mm	10.3mm x 5.3mm	
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm	

- (1) For more information, see Section 11.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.

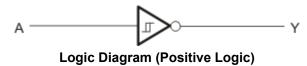


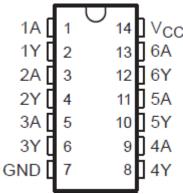


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4 Pin Configuration and Functions



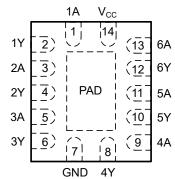
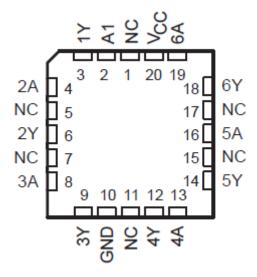


Figure 4-2. SN54AC14 BQA Package, 14-Pin WQFN (Top View)

Figure 4-1. SN54AC14 J or W Package; SN74AC14 D, DB, N, NS, or PW Package; 14-Pin CDIP, CFP, SSOP, SOIC, PDIP, SOP, or TSSOP (Top View)



NC - No internal connection

Figure 4-3. SN54AC14 FK Package, 20-Pin LCCC (Top View)

Table 4-1. Pin Functions

	PIN							
NAME	D, DB, N, NS, PW, BQA, J, or W	FK	I/O	DESCRIPTION				
1A	1	2	Input	Channel 1, Input A				
1Y	2	3	Output	Channel 1, Output Y				
2A	3	4	Input	Channel 2, Input A				
2Y	4	6	Output	Channel 2, Output Y				
3A	5	8	Input	Channel 3, Input A				
3Y	6	9	Output	Channel 3, Output Y				
GND	7	10	_	Ground				
4Y	8	12	Output	Channel 4, Output Y				
4A	9	13	Input	Channel 4, Input A				



Table 4-1. Pin Functions (continued)

	PIN			
NAME	D, DB, N, NS, PW, BQA, J, or W	FK	1/0	DESCRIPTION
5Y	10	14	Output	Channel 5, Output Y
5A	11	16	Input	Channel 5, Input A
6Y	12	18	Output	Channel 6, Output Y
6A	13	19	Input	Channel 6, Input A
V _{CC}	14	20	_	Positive Supply
NC		1, 5, 7, 11, 15, 17	_	Not internally connected
Thermal Pag	d (1)		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) BQA package only.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5V	7	V
V _I (2)	Input voltage range		-0.5V	V _{CC} + 0.5	V
V _O (2)	Output voltage range		-0.5V	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		±20	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50	mA
	Continuous current through V _{CC} or GND			±200	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±4000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommend Operating Conditions

			SN54A	SN54AC14		SN74AC14		
			MIN	MAX	MIN	MAX	UNIT	
V _{CC}	Supply voltage		2	6	2	6	V	
VI	Input voltage		0	V _{CC}	0	V _{CC}	V	
Vo	Output voltage		0	V _{CC}	0	V _{CC}	V	
		V _{CC} = 3 V		-12		-12		
I _{OH}	High-level output current	V _{CC} = 4.5 V		-24		-24	mA	
		V _{CC} = 5.5 V		-24		-24		
		V _{CC} = 3 V		12		12		
I_{OL}	Low-level output current	V _{CC} = 4.5 V		24		24	mA	
		V _{CC} = 5.5 V		24		24		
T _A	Operating free-air temperature	<u>'</u>	-55	125	-40	85	°C	

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾			SN74AC14						
		BQA (WQFN)	I D (SOIC) N (PDIP) NS (SO)						
				14	PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.4	89.9	96	72.1	92.4	148	°C/W	

For more information about traditional and new thermal metrics, see the <u>Semiconductor and IC Package Thermal Metrics</u> application report.

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⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T	₄ = 25°C		SN54A	C14	SN74AC14		UNIT	
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
V _{T+}		3 V	0.8	1.8	2.2	0.8	2.2	0.8	2.2		
Positive-going		4.5 V	1.5	2.6	3.2	1.5	3.2	1.5	3.2	V	
threshold		5.5 V	1.6	3.2	3.9	1.6	3.9	1.6	3.9		
V _{T-}		3 V	0.5	0.8	1	0.5	1.2	0.5	1		
Negative-going		4.5 V	0.9	1.4	1.8	0.9	1.8	0.9	1.8	V	
threshold		5.5 V	1.1	1.8	2.3	1.1	2.3	1.1	2.3		
ΔV_{T}		3 V	0.3	1	1.2	0.3	1.2	0.3	1.2		
Hysteresis		4.5 V	0.4	1.2	1.4	0.4	1.4	0.4	1.4	V	
(V _{T+} - V _{T-})		5.5 V	0.5	1.4	1.6	0.5	1.6	0.5	1.6		
		3 V	2.9			2.9		2.9			
	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		V	
		5.5 V	5.4			5.4		5.4			
	I _{OH} = -12 mA	3 V	2.56			2.4		2.48			
V _{OH}	I _{OH} = -24 mA	4.5 V	3.86			3.7		3.8			
	10H24 IIIA	5.5 V	4.86			4.7		4.8			
	$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V				3.85					
	$I_{OH} = -75 \text{ mA}^{(1)}$	3.5 V						3.85			
		3 V			0.1		0.1		0.1		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1		
		5.5 V			0.1		0.1		0.1		
V _{OL}	I _{OL} = 12 mA	3 V			0.36		0.44		0.44	V	
V OL	I _{OL} = 24 mA	4.5 V			0.36		0.44		0.44	V	
	IOL - 24 IIIA	5.5 V			0.36		0.44		0.44		
	I _{OL} = 50 mA ⁽¹⁾	5.5 V					1.65			1	
	$I_{OL} = 75 \text{ mA}^{(1)}$	3.5 V							1.65		
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ	
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40		20	μΑ	
C _i	V _I = V _{CC} or GND	5 V		4.5						pF	

⁽¹⁾ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	TA	= 25°C		SN54A	C14	SN74	AC14	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
t _{PLH}	۸	V	1.5	6	13.5	1	1 16	1.5	15	20
t _{PHL}	А	, ,	1.5	6	11.5	1	14	1.5	13	ns

Product Folder Links: SN54AC14 SN74AC14



5.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM	то	TA	= 25°C		SN54A	C14	SN74A	C14	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
t _{PLH}	А	Υ _	1.5	5	10	1.5	12	1.5	11	ns
t _{PHL}			1.5	5	8.5	1.5	10	1.5	9.5	

5.8 Operating Characteristics

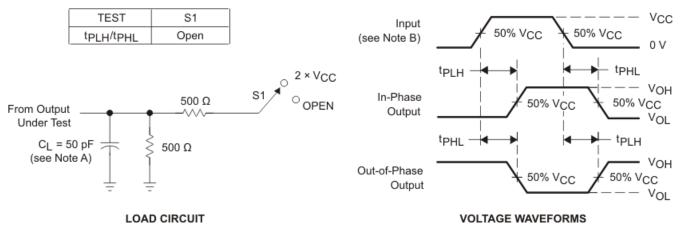
 V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CO	TYP	UNIT	
C_{pd}	Power dissipation capacitance	C _L = 50 pF,	f = 1 MHz	25	pF



6 Parameter Measurement Information

6.1



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

These 'AC14 devices perform the Boolean function $Y = \overline{A}$. Because of the Schmitt action, they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

7.2 Functional Block Diagram



7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
 - Inputs accept V_{IH} levels of 2 V
- · Slow edge rates minimize output ringing
- · Inputs are TTL-Voltage compatible

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.



7.3.2 Clamp Diode Structure

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clampcurrent ratings are observed.

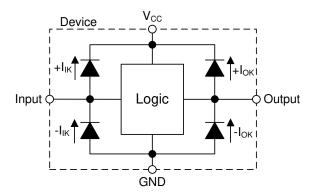


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUT	OUTPUT
Α	Y
Н	L
L	Н

Product Folder Links: SN54AC14 SN74AC14

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SNx4AC14 device is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC} . This feature makes it Ideal for translating down to the V_{CC} level. Switching Characteristics Comparison shows the reduction in ringing compared to higher drive parts such as AC.

8.2 Typical Application

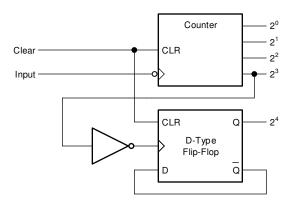


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

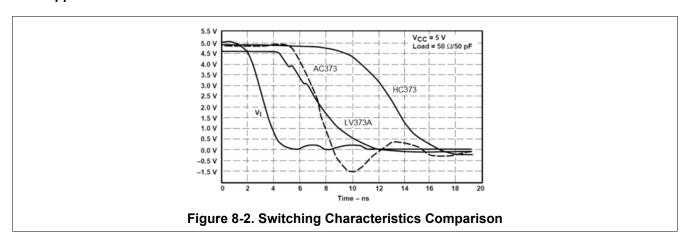
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the Section 5.3 table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the Section 5.3 table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- 2. Recommend Output Conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC}.



8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 5.3.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

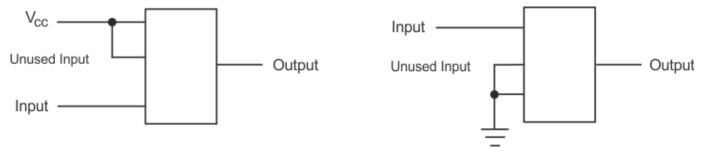


Figure 8-3. Layout Diagram



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AC14	Click here	Click here	Click here	Click here	Click here
SN74AC14	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2023) to Revision I (July 2024) Added BQA package size to Package Information table, Pin Configuration and Functions section, and Thermal Information table......1 Updated R0JA values: D = 86 to 89.9, DB = 96 to 101.2, N = 80 to 72.1, NS = 76 to 92.4, PW = 113 to 148, all values in °C/W......5

Changes from Revision G (August 2008) to Revision H (January 2023)

Page

Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and

Product Folder Links: SN54AC14 SN74AC14



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-87624012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87624012A SNJ54AC 14FK
5962-8762401CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J
5962-8762401DA	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W
SN74AC14BQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14
SN74AC14BQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14
SN74AC14D	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	AC14
SN74AC14DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC14N
SN74AC14N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC14N
SN74AC14NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14NSRG4	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	AC14
SN74AC14PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC14
SN74AC14PWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14
SNJ54AC14FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87624012A SNJ54AC 14FK



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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54AC14FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87624012A SNJ54AC 14FK
SNJ54AC14J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J
SNJ54AC14J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401CA SNJ54AC14J
SNJ54AC14W	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W
SNJ54AC14W.A	Active	Production	CFP (W) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8762401DA SNJ54AC14W

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.





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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AC14, SN74AC14:

Catalog : SN74AC14

Automotive: SN74AC14-Q1, SN74AC14-Q1

Military: SN54AC14

Space : SN54AC14-SP

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Military - QML certified for Military and Defense Applications

• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC14BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AC14DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC14NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74AC14NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AC14PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC14PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC14BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AC14DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AC14DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AC14DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC14NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AC14NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AC14PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC14PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0



PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87624012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8762401DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AC14N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC14N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC14N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC14N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AC14FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC14FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC14W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AC14W.A	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025