

SN74AC11-Q1 Automotive Triple 3-Input Positive-AND Gate

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous 24mA output drive at 5V
- Supports up to 75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Maximum t_{pd} of 7.5ns at 5V, 50pF load

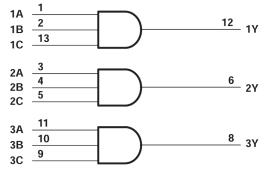
2 Description

The SN74AC11-Q1 device contains three independent 3-input AND gates. This device performs the Boolean function $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic

Package Information

	•		
PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	WQFN (BQA, 14)	3mm x 2.5mm	3mm x 2.5mm
SN74AC11-Q1	D (SOIC, 14)	8.65mm x 6mm	8.65mm x 3.9mm
	PW (TSSOP, 14)	5mm x 6.4mm	5mm x 4.4mm

- For all available packages, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Gate (Positive Logic)



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3 Pin Configuration and Functions

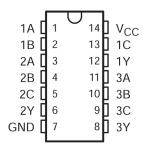


Figure 3-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

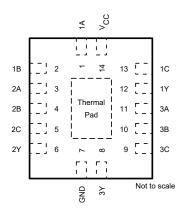


Figure 3-2. BQA Package, 14-Pin WQFN (Top View)

Table 3-1. Pin Functions

P	PIN	I/O ⁽¹⁾	DESCRIPTION
NAME	NO.	1/0(1/	DESCRIPTION
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	_	Ground
3Y	8	Output	Channel 3, Output Y
3C	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3A	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V _{CC}	14	_	Positive Supply
Thermal Pad ⁽²)	_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

- (1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
- (2) BQA package only



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		·	MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I (2)	Input voltage range		-0.5	V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50	mA
	Continuous current through V_{CC} GND	or		±200	mA
T _{stg}	Storage temperature range		-65	150	°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-0021	±2000	V

1. AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74AC11	SN74AC11-Q1	
			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	6	V
		V _{CC} = 3V	2.1		
V _{IH}	High-level input voltage	V _{CC} = 4.5V	3.15		V
		V _{CC} = 5.5V	3.85		
		V _{CC} = 3V		0.9	
V _{IL}	Low-level input voltage	V _{CC} = 4.5V		1.35	V
		V _{CC} = 5.5V		1.65	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 3V		-12	
I _{OH}	High-level output current	V _{CC} = 4.5V		-24	mA
		V _{CC} = 5.5V		-24	
		V _{CC} = 3V		12	
I _{OL}	Low-level output current	V _{CC} = 4.5V		24	mA
		V _{CC} = 5.5V		24	
Δt/Δν	Input transition rise or fall rate			8	ns/V
T _A	Operating free-air temperature		-40	85	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Product Folder Links: SN74AC11-Q1

The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.4 Thermal Information

			SN74AC11-Q1		
THERMAL METRIC(1)		BQA (WQFN)	BQA (WQFN) D (SOIC) PW (TSSOP)		
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.3	119.9	145.7	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	TEST SOMBITIONS			A = 25°C		SN74AC1	11-Q1	LINIT	
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNIT	
		3V	2.9	2.99		2.9			
	$I_{OH} = -50 \mu A$	4.5V	4.4	4.49		4.4			
		5.5V	5.4	5.49		5.4			
\\\	I _{OH} = -12mA	3V	2.56			2.46		V	
V _{OH}	I _{OH} = -24mA	4.5V	3.86			3.76		V	
	10H24IIIA	5.5V	4.86			4.76			
	$I_{OH} = -50 \text{mA}^{(1)}$	5.5V							
	$I_{OH} = -75 \text{mA}^{(1)}$	5.5V				3.85			
	I _{OL} = 50μA	3V 0.002 0.1		0.1					
		4.5V		0.001	0.1		0.1		
		5.5V		0.001	0.1		0.1		
V _{OL}	I _{OL} = 12mA	3V			0.36		0.44	V	
VOL	1 - 24mA	4.5V			0.36		0.44	V	
	I _{OL} = 24mA	5.5V			0.36		0.44		
	I _{OL} = 50mA ⁽¹⁾	5.5V							
	I _{OL} = 75mA ⁽¹⁾	5.5V					1.65		
I _I	V _I = V _{CC} or GND	5.5V			±0.1		±1	μA	
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V	-		2		20	μA	
C _i	V _I = V _{CC} or GND	5V		2.6				pF	

⁽¹⁾ Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.

4.6 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	EDOM (INIDIIT)	TO (OUTPUT)	Т	A = 25°C		SN74AC	11-Q1	UNIT
PARAMETER	TER FROM (INPUT)	10 (001701)	MIN	TYP	MAX	MIN	MAX	UNII
t _{PLH}	A, B, or C	2 or C	1.5	5.5	9.5	1	10	ne
t _{PHL}	A, B, or C	'	1.5	5.5	8.5	1	9.5	ns

4.7 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT) TO (OUTPUT)	Т	T _A = 25°C			SN74AC11-Q1		
PARAMETER		10 (001701)	MIN	TYP	MAX	MIN	MAX	UNIT
t _{PLH}	A B or C	A, B, or C Y	1.5	4	8	1	8.5	ne
t _{PHL}	А, В, ОГС		1.5	4	7	1	7.5	ns

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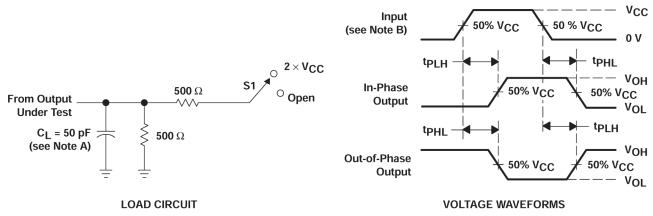


4.8 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50pF,	f = 1 MHz	20	pF

5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- 3. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open

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6 Detailed Description

6.1 Functional Block Diagram

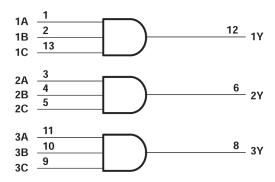


Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

6.2 Feature Description

6.2.1 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law $(R = V \div I)$.

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a $10k\Omega$ resistor, however, is recommended and will typically meet all requirements.

6.3 Device Functional Modes

Table 6-1. Function Table (Each Gate)

	INPUTS	OUTPUT			
Α	В	С	Υ		
Н	Н	Н	Н		
L	Х	Х	L		
Х	L	Х	L		
Х	Х	L	L		



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

- · Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - · Avoid branches; buffer signals that must branch separately

7.2.2 Layout Example

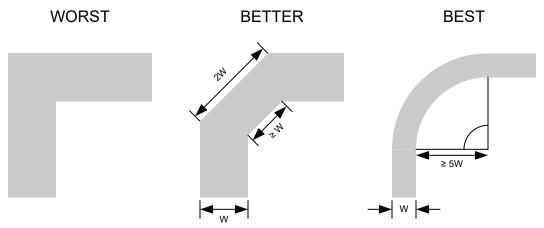


Figure 7-1. Example Trace Corners for Improved Signal Integrity

Product Folder Links: SN74AC11-Q1

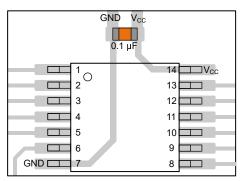


Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages

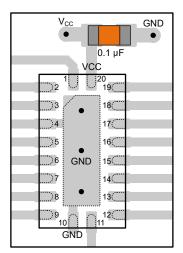


Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages

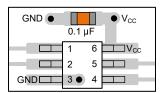


Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

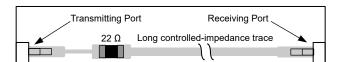


Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity



8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, CMOS Power Consumption and Cpd Calculation application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2008) to Revision B (February 2025)

Page

- Added BQA package to Package Information table, Pin Configuration and Functions section, and Thermal
 Information table
- Added Package Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Device
 Functional Modes, Application and Implementation section, Device and Documentation Support section, and
 Mechanical, Packaging, and Orderable Information section

Product Folder Links: SN74AC11-Q1



10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AC11IDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11IQ1
SN74AC11IDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11IQ1
SN74AC11IPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11IQ1
SN74AC11IPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11IQ1
SN74AC11WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11Q
SN74AC11WBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN74AC11-Q1:

■ Catalog : SN74AC11

• Enhanced Product : SN74AC11-EP

Military : SN54AC11

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

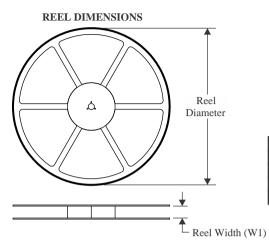
• Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

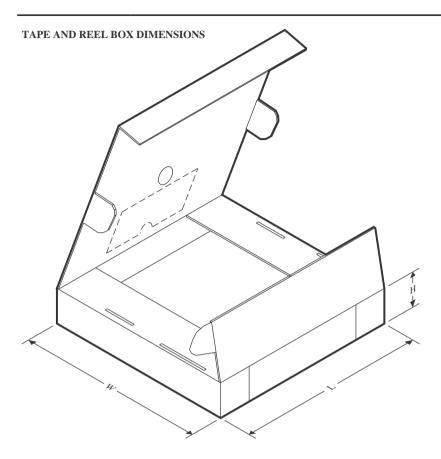


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC11IPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC11WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC11IPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC11WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

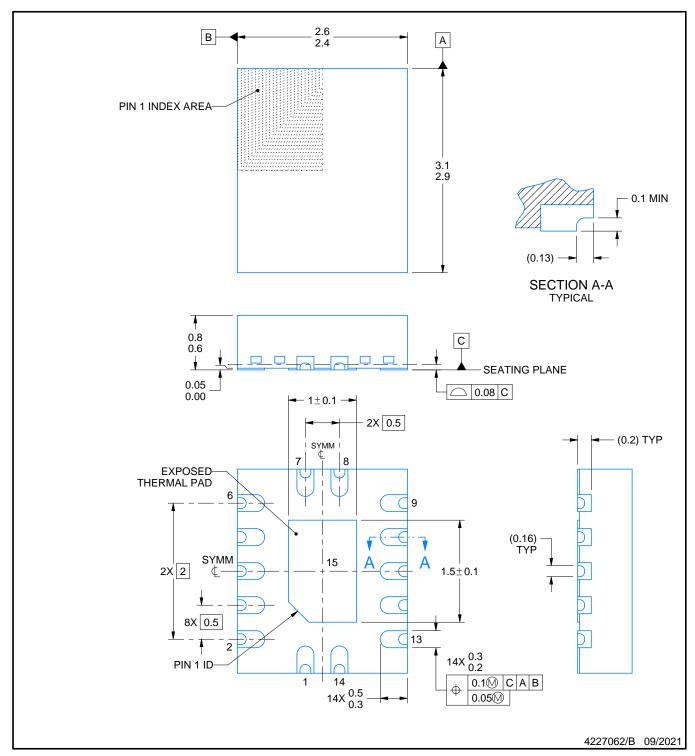
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD

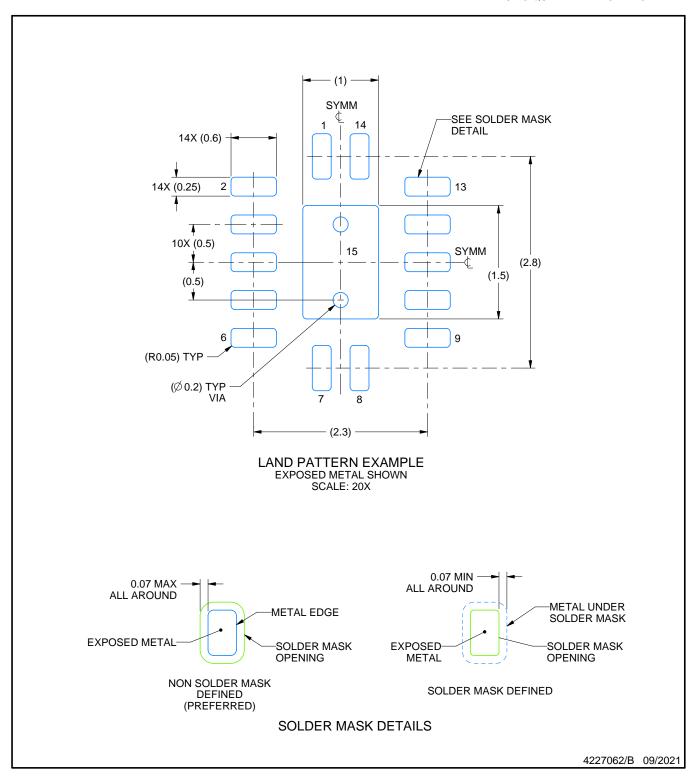


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

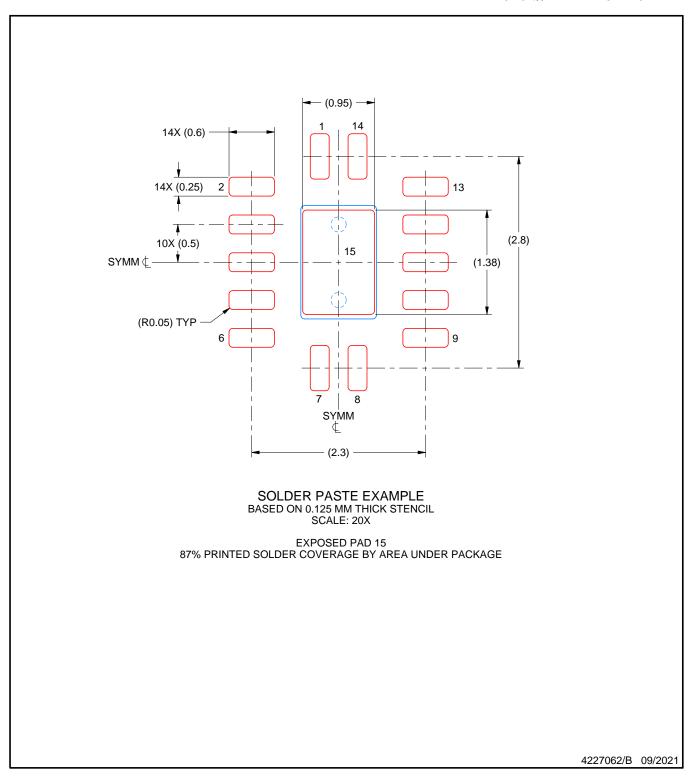


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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