

SN74AC08-Q1 Automotive Quadruple 2-Input Positive-and Gate

1 Features

- Qualified for automotive applications
- 2V to 6V V_{CC} operation
- Inputs accept voltages to 6V
- Max t_{pd} of 7.5ns at 5V

2 Description

The SN74AC08 device is a quadruple 2-input positive-AND gate. This device performs the Boolean function $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)	BODY SIZE(3)
	BQA (WQFN, 14)	3mm x 2.5mm	3mm x 2.5mm
SN74AC08-Q1	D (SOIC, 14)	8.65 mm × 6mm	8.65 mm × 3.9mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.

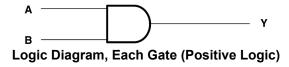




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3 Pin Configuration and Functions

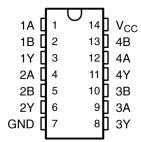


Figure 3-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

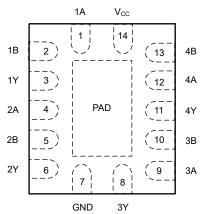


Figure 3-2. BQA Package, 14-Pin WQFN (Top View)

Table 3-1. Pin Functions

	PIN		
NAME	NO.	TYPE ⁽¹⁾	DESCRIPTION
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	_	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V _{CC}	14	_	Positive Supply
Thermal pad ⁽²⁾		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

⁽¹⁾ I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

⁽²⁾ BQA package only.



4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		·	MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I ⁽²⁾	Input voltage range			V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		±20	mA
I _{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±20	mA
Io	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50	mA
	Continuous current through V _{CC} or G		±200	mA	
T _{stg}	Storage temperature range			150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1))

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	6	V
		V _{CC} = 3V	2.1		
V_{IH}	High-level input voltage	V _{CC} = 4.5V	3.15		V
		V _{CC} = 5.5V	3.85		
		V _{CC} = 3V		0.9	
V_{IL}	Low-level input voltage	V _{CC} = 4.5V		1.35	V
		V _{CC} = 5.5V		1.65	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 3V		-12	
I _{OH}	High-level output current	V _{CC} = 4.5V		-24	mA
		V _{CC} = 5.5V		-24	
		V _{CC} = 3V		12	
I _{OL}	Low-level output current	V _{CC} = 4.5V		24	mA
		V _{CC} = 5.5V		24	
Δt/Δν	Input transition rise or fall rate	,		8	ns/V
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.3 Thermal Information

			SN74AC08-Q1				
THERMAL METRIC(1)		BQA (WQFN)	1 D (SOIC)		UNIT		
		14 PINS	14 PINS	14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.3	119.9	145.7	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics.

Product Folder Links: SN74AC08-Q1

²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{cc}	T,	₄ = 25°C		T _A = −40° 125°0		T _A = -		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
			3V	2.9			2.9		2.9		
	$I_{OH} = -50 \mu A$		4.5V	4.4			4.4		4.4		
V			5.5V	5.4			5.4		5.4		V
V _{OH}	I _{OH} = −12mA		3V	2.56			2.4		2.46		v
	I _{OH} = -24mA		4.5V	3.86			3.7		3.76		
	1 _{OH} 24111A		5.5V	4.86			4.7		4.76		
			3V		0.002	0.1		0.1		0.1	
	I _{OL} = 50μA		4.5V		0.001	0.1		0.1		0.1	
V			5.5V		0.001	0.1		0.1		0.1	V
V _{OL}	I _{OL} = 12mA		3V			0.36		0.5		0.44	v
	I = 24m A		4.5V			0.36		0.5		0.44	
	$I_{OL} = 24mA$		5.5V			0.36		0.5		0.44	
I _I A or B ports	V _I = V _{CC} or GND		5.5V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	5.5V			2		40		20	μA
C _i	$V_I = V_{CC}$ or GND		5V		4.5						pF

4.5 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C		T _A = 25°C		T _A = -40°C TO 125°C		T _A = -40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH}	A or B	V	1.5	7.5	9.5	1	12.5	1	10	no	
t _{PHL}		ľ	1.5	7	8.5	1	11.5	1	9	ns	

4.6 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C				10°C TO 5°C	T _A = -40 85°		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	V	1.5	5.5	7.5	1	9	1	8.5	ns
t _{PHL}	AUID	•	1.5	7	8.5	1	11.5	1	9	115

4.7 Operating Characteristics

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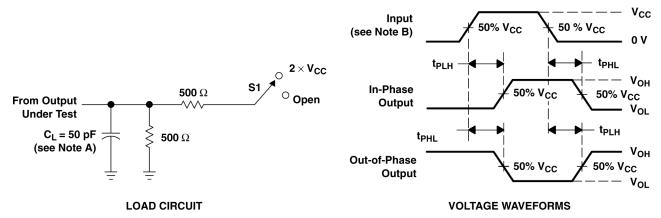
 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYF	UNIT
C _{pd}	Power dissipation capacitance	$C_L = 50pF,$ $f = 1$	1 MHz 20) pF

Product Folder Links: SN74AC08-Q1



5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r v 2.5 ns, t_f v 2.5 ns.
- C. The outputs are measured one at a time, with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t _{PLH} /t _{PHL}	Open

Product Folder Links: SN74AC08-Q1

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6 Detailed Description

6.1 Functional Block Diagram



Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

6.2 Device Functional Modes

Table 6-1. Function Table (Each Gate)

INPUT	S	OUTPUT Y
Α	В	OUIPULT
Н	Н	Н
L	X	L
X	L	L



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended. If there are multiple V_{CC} pins, 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Section 7.2.2 shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

7.2.2 Layout Example

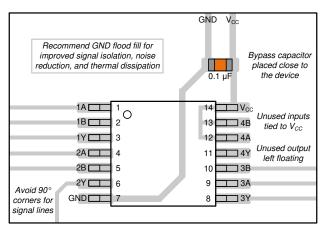


Figure 7-1. Example Layout for the SN74AC08-Q1

Product Folder Links: SN74AC08-Q1

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN74AC08-Q1	Click here	Click here	Click here	Click here	Click here	

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2024) to Revision C (February 2025)

Page

Added BQA package to Package Information table, Pin Configuration and Functions section, and Thermal
 Information table

Changes from Revision A (January 2008) to Revision B (July 2024)

Page

 Added Package Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Device Functional Modes, Application and Implementation section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section



10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74AC08-Q1

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
SN74AC08QDRG4Q1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08QDRG4Q1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08QPWRG4Q1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08QPWRG4Q1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08QPWRQ1	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08QPWRQ1.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08WBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q
SN74AC08WBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC08Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AC08-Q1:

● Enhanced Product : SN74AC08-EP

Military: SN54AC08

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

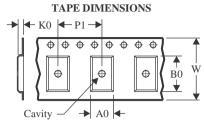
• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

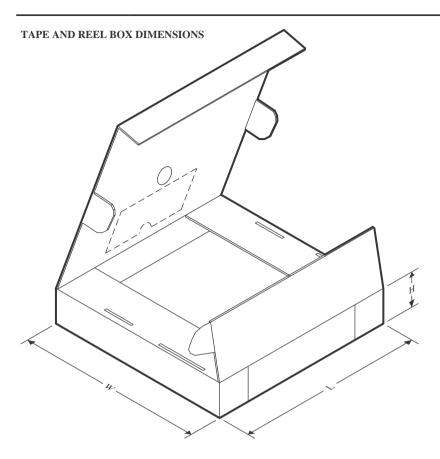


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC08QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC08QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC08WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC08QPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC08QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC08WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

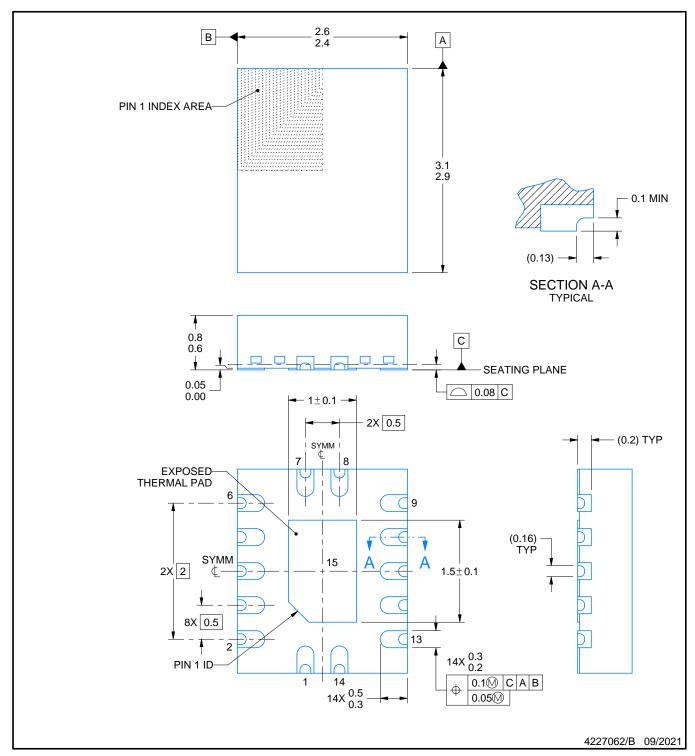
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD

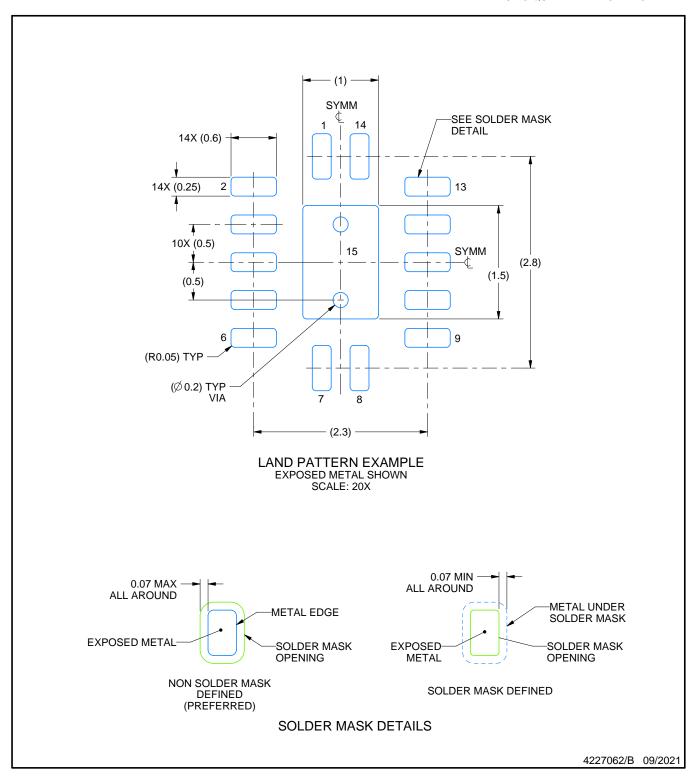


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

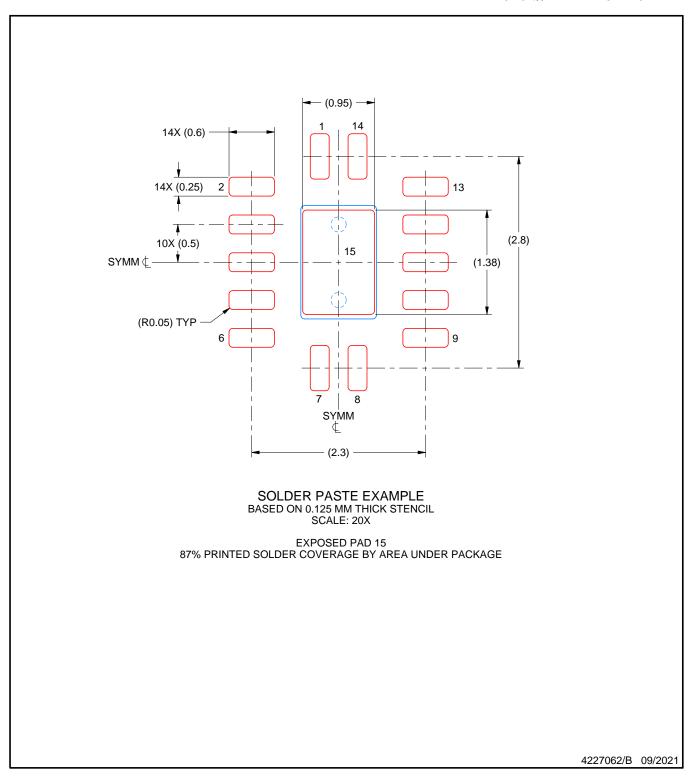


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

^{6.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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