







SN54AC04, SN74AC04

SCAS519G - JULY 1995 - REVISED JULY 2024

# **SNx4AC04 Hex Inverters**

#### 1 Features

- V<sub>CC</sub> operation of 2V to 6V
- Inputs accept voltages to 6V
- Max t<sub>pd</sub> of 7ns at 5V

# 2 Applications

- Synchronize inverted clock inputs
- Debounce a switch
- Invert a digital signal

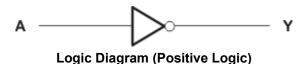
# 3 Description

The 'AC04 devices contain six independent inverters. The devices perform the Boolean function  $Y = \overline{A}$ .

#### **Device Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)	BODY SIZE(3)
	BQA (WQFN, 14)	3mm x 2.5mm	3mm x 2.5mm
	DB (SSOP, 14)	6.2mm x 7.8mm	6.2mm x 5.3mm
SNx4AC04	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	NS (SOP, 14)	10.2mm x 7.8mm	10.3mm x 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- For more information, see Mechanical, Packaging, and Orderable Information.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.





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# 4 Pin Configuration and Functions

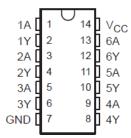


Figure 4-1. SN54AC04 J or W Package; SN74AC04 D, DB, N, NS, or PW Package; 14-Pin CDIP, CFP, SOIC, SSOP, PDIP, SOP, and TSSOP (Top View)

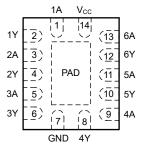


Figure 4-2. SN74AC04 BQA Package, 14-Pin WQFN (Top View)

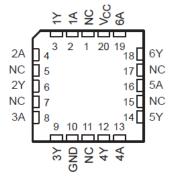


Figure 4-3. SN54AC04 FK Package, 20-Pin LCCC (Top View)

	PIN			
NAME	D, DB, N, NS, PW, J, W, or BQA	FK	I/O	DESCRIPTION
1A	1	2	Input	Channel 1, Input A
1Y	2	3	Output	Channel 1, Output Y
2A	3	4	Input	Channel 2, Input A
2Y	4	6	Output	Channel 2, Output Y
3A	5	8	Input	Channel 3, Input A
3Y	6	9	Output	Channel 3, Output Y
GND	7	10	_	Ground
4Y	8	12	Output	Channel 4, Output Y
4A	9	13	Input	Channel 4, Input A
5Y	10	14	Output	Channel 5, Output Y
5A	11	16	Input	Channel 5, Input A
6Y	12	18	Output	Channel 6, Output Y
6A	13	19	Input	Channel 6, Input A
V <sub>CC</sub>	14	20	_	Positive Supply
NC		1, 5, 7, 11, 15, 17	_	Not internally connected
Thermal P	ad <sup>(1)</sup>		_	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) BQA package only.



# **5 Specifications**

#### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
VI	Input voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
Vo	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I <sub>OK</sub>	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to $V_{CC}$		±50	mA
	Continuous current through V <sub>CC</sub> or GND	·		±200	mA
T <sub>stg</sub>	Storage temperature range		-60	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 5.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## **5.3 Recommended Operating Conditions**

over recommended operating free-air temperature range (unless otherwise noted)(1)

			SN54A	SN54AC04		C04	UNIT
			MIN	MAX	MIN MAX		UNII
V <sub>CC</sub>	Supply voltage		2	6	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		2.1		V
		V <sub>CC</sub> = 4.5 V	3.15		3.15		
		V <sub>CC</sub> = 5.5 V	3.85		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9		0.9	V
		V <sub>CC</sub> = 4.5 V		1.35		1.35	
		V <sub>CC</sub> = 5.5 V		1.65		1.65	
VI	Input voltage	'	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
Vo	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		-12		-12	mA
		V <sub>CC</sub> = 4.5 V		-24		-24	
		V <sub>CC</sub> = 5.5 V		-24		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12		12	mA
		V <sub>CC</sub> = 4.5 V		24		24	
		V <sub>CC</sub> = 5.5 V		24		24	
Δt/Δν	Input transition rise or fall rate	1		8		8	ns/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Product Folder Links: SN54AC04 SN74AC04

<sup>(2)</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### **5.4 Thermal Information**

		SN74AC04						
	THERMAL METRIC <sup>(1)</sup>		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	UNIT
				14 P	INS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.4	89.9	96	80	92.4	148	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

#### 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		Т,	<sub>A</sub> = 25°C		SN54A	C04	SN74A	C04	UNIT
PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9	2.99		2.9		2.9		
	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49		4.4		4.4		
		5.5 V	5.4	5.49		5.4		5.4		
V	I <sub>OH</sub> = −12 mA	3 V	2.56			2.4		2.46		V
V <sub>OH</sub>	I <sub>OH</sub> = -24 mA	4.5 V	3.86			3.7		3.76		v
	10H24 IIIA	5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V				3.85				
	$I_{OH} = -75 \text{ mA}^{(1)}$	5.5 V						3.85		
	Ι <sub>ΟL</sub> = 50 μΑ	3 V		0.002	0.1		0.1		0.1	
		4.5 V		0.001	0.1		0.1		0.1	
		5.5 V		0.001	0.1		0.1		0.1	
V	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5		0.44	v
V <sub>OL</sub>	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5		0.44	v
	1 <sub>OL</sub> - 24 IIIA	5.5 V		-	0.36		0.5		0.44	
	I <sub>OL</sub> = 50 mA <sup>(1)</sup>	5.5 V					1.65			
	I <sub>OL</sub> = 75 mA <sup>(1)</sup>	5.5 V							1.65	
Iı	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40		20	μA
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND			2.8						pF

<sup>(1)</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

# 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC}$  = 3.3 V  $\pm$  0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms )

PARAMETER FROM		FROM TO		T <sub>A</sub> = 25°C		SN54AC04		SN74AC04		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
t <sub>PLH</sub>	^	V	1.5	4.5	9	1	11	1	10	no
t <sub>PHL</sub>	A	T	1.5	4.5	8.5	1	10	1	9.5	ns

# **5.7 Operating Characteristics**

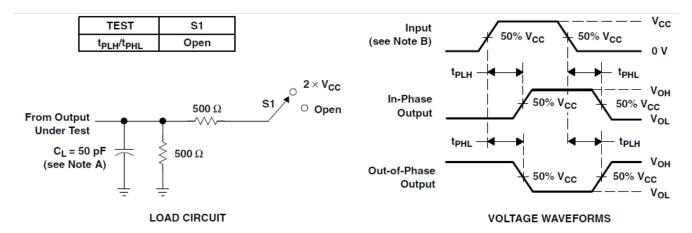
 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF	f = 1 MHz	45	pF



#### **6 Parameter Measurement Information**

#### **Load Circuit and Voltage Waveforms**



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.

C. The outputs are measured one at a time with one input transition per measurement.

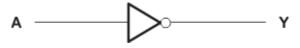


# 7 Detailed Description

#### 7.1 Overview

The 'AC04 devices contain six independent inverters. The devices perform the Boolean function  $Y = \overline{A}$ .

#### 7.2 Functional Block Diagram



**Logic Diagram (Positive Logic)** 

# 7.3 Feature Description

The SNx4AC04 devices have an operating  $V_{CC}$  range from 2 V to 6 V.

#### 7.4 Device Functional Modes

Function Table lists the function modes of the SNx4ACT04.

Function Table (Each Inverter)

INPUT	OUTPUT
Α	Υ
Н	L
L	Н

# 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### 8.1 Application Information

The SNx4ACT04 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

#### 8.2 Typical Application

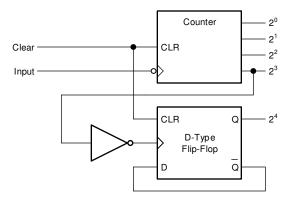


Figure 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions
  - Rise time and fall time specs: See (Δt/ΔV) in the Section 5.3.
  - Specified high and low levels: See (V<sub>IH</sub> and V<sub>IL</sub>) in the Section 5.3.
- 2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above V<sub>CC</sub>.



# 8.2.3 Application Curve

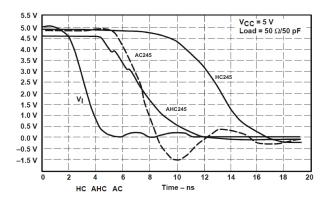


Figure 8-2. Switching Characteristics Comparison

#### 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Section 5.3.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and a 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

#### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Section 8.4.1.1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

#### 8.4.1.1 Layout Example

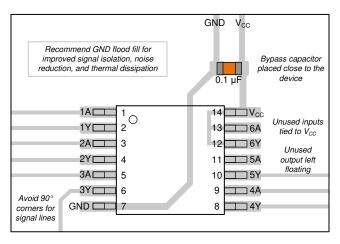


Figure 8-3. Example Layout of the SN74AC04

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## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 9.1 Device and Documentation Support

#### 9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AC04	Click here	Click here	Click here	Click here	Click here
SN74AC04	Click here	Click here	Click here	Click here	Click here

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

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#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### 

Updated Layout Example image......10



#### Changes from Revision E (July 1995) to Revision F (January 2023)

Page

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN54AC04 SN74AC04

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# **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	3.1		Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-87609012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87609012A SNJ54AC 04FK
5962-8760901CA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8760901CA SNJ54AC04J
5962-8760901DA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8760901DA SNJ54AC04W
SN74AC04BQAR	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04
SN74AC04BQAR.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04
SN74AC04D	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	AC04
SN74AC04DBR	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04DBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04DR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04DR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04DRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04
SN74AC04DRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04
SN74AC04N	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC04N
SN74AC04N.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC04N
SN74AC04NE4	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC04N
SN74AC04NSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04NSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04PW	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	AC04
SN74AC04PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04PWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC04
SN74AC04PWRG4.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04
SNJ54AC04FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87609012A SNJ54AC 04FK





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Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SNJ54AC04FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 87609012A SNJ54AC 04FK
SNJ54AC04J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8760901CA SNJ54AC04J
SNJ54AC04J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8760901CA SNJ54AC04J
SNJ54AC04W	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8760901DA SNJ54AC04W
SNJ54AC04W.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8760901DA SNJ54AC04W

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.





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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54AC04, SN74AC04:

Catalog: SN74AC04

Automotive: SN74AC04-Q1, SN74AC04-Q1

● Enhanced Product : SN74AC04-EP, SN74AC04-EP

Military: SN54AC04

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications



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#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC04BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AC04DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AC04DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AC04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC04DRG4	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AC04NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AC04NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74AC04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC04PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC04BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AC04DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74AC04DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AC04DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC04DRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74AC04NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AC04NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AC04PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC04PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

# **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87609012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8760901DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AC04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC04N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AC04FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC04FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC04W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54AC04W.A	W	CFP	14	25	506.98	26.16	6220	NA



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLAT PACK-NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# W (R-GDFP-F14)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-150.





NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
   Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
   Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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