SCBS159E - JANUARY 1991 - REVISED APRIL 2005

- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

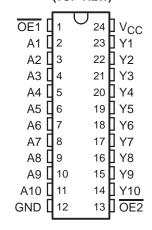
description

These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

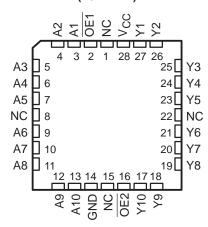
The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable $(\overline{OE1} \text{ or } \overline{OE2})$ input is high, all ten outputs are in the high-impedance state. The 'ABT827 provides true data at the outputs.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT827 . . . JT PACKAGE SN74ABT827 . . . DB, DW, NT, OR PW PACKAGE (TOP VIEW)



SN54ABT827 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN54ABT827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Χ	Н	Χ	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

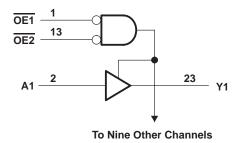
EPIC-IIB is a trademark of Texas Instruments.



logic symbol[†]

& OE1 ΕN 13 OE2 23 Υ1 **A1** 3 22 **Y2** A2 4 21 Υ3 Α3 5 20 Α4 **Y4** 6 19 Α5 Y5 7 18 Α6 **Y6** 8 17 **A7 Y7** 9 16 **Y8 A8** 10 15 Α9 Υ9 11 14 Y10 A10

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		-0.5 V to 7 V
Input voltage range, V _I (see Note 1)		-0.5 V to 7 V
Voltage range applied to any output in the high or	r power-off state, VO	. $-0.5\ V$ to $5.5\ V$
Current into any output in the low state, IO: SN54	4ÅBT827	96 mA
SN74	4ABT827	128 mA
Input clamp current, I _{IK} (V _I < 0)		–18 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Package thermal impedance, θ _{JA} (see Note 2): D		
D	DW package	81°C/W
N	NT package	67°C/W
Р	PW package	120°C/W
Storage temperature range, T _{stg}		-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 3)

		SN54A	BT827	SN74A	BT827	
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	VCC	0	VCC	V
IOH	High-level output current		-24		-32	mA
loL	Low-level output current		48		64	mA
Δt/Δν	Input transition rise or fall rate		5		5	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

SN54ABT827, SN74ABT827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS159E - JANUARY 1991 - REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			1	A = 25°	C	SN54A	MAX -1.2 0.55 ±1 ±10 ±10 -10 -225 250 40 250 1.5 50 1.5	SN74A	BT827	
PARAMETER	TEST CONDIT	IONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2		-1.2		-1.2	V
	V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.5			2.5		2.5		
.,,	V _{CC} = 5 V,	IOH = -3 mA	3			3		3		V
VOH	V 45V	I _{OH} = -24 mA	2			2				V
	V _{CC} = 4.5 V	I _{OH} = -32 mA	2*					2		
V	V 45V	I _{OL} = 48 mA			0.55		0.55			V
VOL	V _{CC} = 4.5 V	I _{OL} = 64 mA			0.55*				0.55	V
V _{hys}				100						mV
l _l	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±1		±1		±1	μΑ
lozpu [‡]	$V_{CC} = 0$ to 2.1 V, $V_{O} = 0.5$ V	to 2.7 V, OE = X			±50		±10		±50	μΑ
IOZPD [‡]	$V_{CC} = 2.1 \text{ V to } 0, V_{O} = 0.5 \text{ V}$	to 2.7 V, OE = X			±50		±10		±50	μΑ
lozh	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}, V_{O} = 2.7 \text{ V}$	7 V, OE ≥ 2 V			10§		10		10§	μΑ
lozL	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V}, V_{O} = 0.5 \text{ V}$	5 V, OE ≥ 2 V			-10§		-10		-10§	μΑ
l _{off}	$V_{CC} = 0$,	V_I or $V_O \le 5.5 \text{ V}$			±100				±100	μΑ
ICEX	$V_{CC} = 5.5 \text{ V}, V_{O} = 5.5 \text{ V}$	Outputs high			50		50		50	μΑ
IO¶	V _{CC} = 5.5 V,	V _O = 2.5 V	-50	-140	-225§	-50	-225§	-50	-225§	mA
	.,,	Outputs high		80	250		250		250	μΑ
ICC	$V_{CC} = 5.5 \text{ V}, I_{O} = 0,$ $V_{I} = V_{CC} \text{ or GND}$	Outputs low		35	40\$		40§		40§	mA
	V1 = V00 01 0115	Outputs disabled		80	250		250		250	μΑ
	V _{CC} = 5.5 V,	Outputs enabled			1.5		1.5		1.5	mA
∆lcc#	One input at 3.4 V,	Outputs disabled			50		50		50	μΑ
	Other inputs at V _{CC} or GND	Control inputs			1.5		1.5		1.5	mA
Ci	V _I = 2.5 V or 0.5 V			4						pF
Co	V _O = 2.5 V or 0.5 V			8						pF

 $[\]buildrel{\complex}^{\star}$ On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V _C	C = 5 V \ = 25°C	<u>'</u> ,	SN54A	BT827	SN74A	BT827	UNIT
	(INPUT)	PUT) (OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}		Υ	1.1	2.6	4.4	1.1	4.9	1.1	4.8	
t _{PHL}	А		1.1	2.3	4.1	1.1	4.8	1.1	4.7	ns
^t PZH		V	1§	3.2	5.1	1	6	1§	5.9	
tpZL	ŌĒ	Y	1§	3.3	5.9	1	7.1	1§	6.9	ns
t _{PHZ}	ŌĒ	V	2	4.9	6.3	2	7	2	6.8	20
tPLZ	OE .	Y	1.3§	4.2	6.6	1.3	7.9	1.3§	6.9	ns

[§] This data sheet limit may vary among suppliers.



[†] All typical values are at $V_{CC} = 5 \text{ V}$.

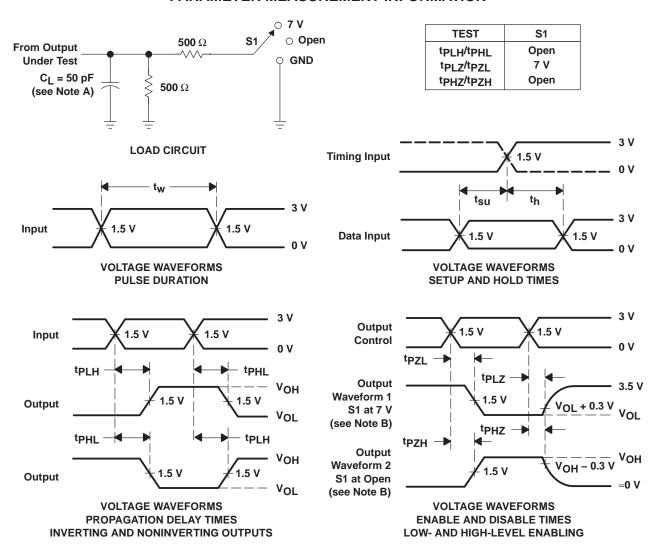
[‡]This parameter is characterized, but not production tested.

[§] This data sheet limit may vary among suppliers.

[¶] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[#]This is the increase in supply current for each input that is at the specified TTL voltage level, rather than VCC or GND.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

www.ti.com

11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
5962-9450901QKA	Active	Production	CFP (W) 24	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9450901QK A SNJ54ABT827W
5962-9450901QLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9450901QL A SNJ54ABT827JT
SN74ABT827DBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827DBR.B	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT827
SN74ABT827DW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT827
SN74ABT827DWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT827
SN74ABT827DWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT827
SN74ABT827PW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827PW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827PWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827PWRG4	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SN74ABT827PWRG4.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB827
SNJ54ABT827JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9450901QL A SNJ54ABT827JT
SNJ54ABT827W	Active	Production	CFP (W) 24	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9450901QK A SNJ54ABT827W

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ABT827, SN74ABT827:

Catalog: SN74ABT827

Military: SN54ABT827

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 9-Oct-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT827DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT827DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT827PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74ABT827PWRG4	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

www.ti.com 9-Oct-2025



*All dimensions are nominal

7 til dillionorio di o mominar							
Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT827DBR	SSOP	DB	24	2000	353.0	353.0	32.0
SN74ABT827DWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74ABT827PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74ABT827PWRG4	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 9-Oct-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9450901QKA	W	CFP	24	25	506.98	26.16	6220	NA
SN74ABT827DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT827DW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT827PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74ABT827PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
SNJ54ABT827W	W	CFP	24	25	506.98	26.16	6220	NA

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



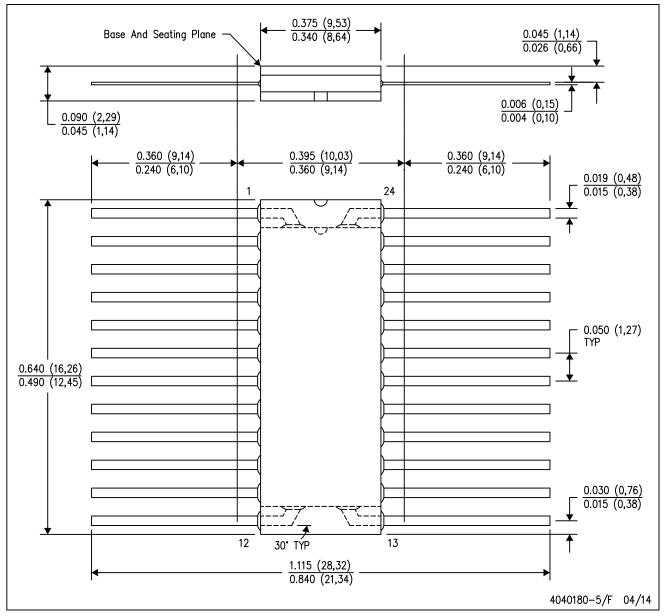
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only. E. Falls within Mil—Std 1835 GDFP2—F20



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025